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SST 28LF040 3.0V-only 4 Megabit SuperFlash EEPROM

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Data Sheet



Features:

Single 3.0-Volt Read and Write Operations				
CMOS SuperFlash EEPRO	M Technology			
Endurance: 100,000 Cycl	les (typical)			
Greater than 100 years D	Data Retention			
Memory Organization:	512K x 8			
Sector Erase Capability:	256 bytes per Sector			
Low Power Consumption:				
Active Current:	10 mA (typical)			
Standby Current:	5 µA (typical)			
Fast Sector Erase/Byte Pre	ogram Operation			
Byte Program Time:	35 µs (typical)			
Sector Erase Time:	2 ms (typical)			
Complete Memory Rewrit	te: 20 sec (typical)			
Fast Access Time: 200 and 250 ns				

Latched Address and Data Hardware and Software Data Protection 7-Read-Cycle-Sequence Software Data Protection End of Write Detection Toggle Bit Data# Polling TTL I/O Compatibility Packages Available 40-Pin TSOP (10 mm x 20 mm) 32-Pin TSOP (8 mm x 20 mm) 32-Pin PLCC 32-Pin PDIP

Product Description

The 28LF040 is a 512K x 8 (bits) CMOS sector erase, byte program EEPROM. The 28LF040 is manufactured using SST's proprietary, high peformance CMOS SuperFlash EEPROM Technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternative approaches. The 28LF040 erases and programs with a 3.0 volt only power supply. (V_{cc}: 3.0V to 3.6V) The 28LF040 conforms to JEDEC standard pinouts for byte wide memories and is compatible with existing industry standard EPROM, flash EPROM and EEPROM pinouts.

Featuring high performance programming, the 28LF040 typically byte programs in 35 μ s. The 28LF040 typically sector erases in 2 ms. Both program and erase times can be optimized using interface features such as Toggle bit or Data# Polling to indicate the completion of the write φ -cle. To protect against an inadvertent write, the 28LF040 has on chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the 28LF040 is offered with a guaranteed sector endurance of 10⁴ and 10³ cycles. Data retention is rated greater than 100 years.

The 28LF040 is best suited for applications that require reprogrammable nonvolatile mass storage of program, configuration, or data memory. For all system applications, the 28LF040 significantly improves performance and reliability, while lowering power consumption when compared with floppy diskettes or EPROM approaches. EEPROM technology makes possible convenient and economical updating of codes and control pograms on-line. The 28LF040 improves flexibility, while lowering the cost of program and configuation storage application.

Figure 1 shows the functional blocks of the 28LF040. Figures 2A, 2B, and 3 show the pin assignments for the 40 pin TSOP, 32 pin TSOP, 32 pin PDIP, and 32 pin PLCC packages. Pin description and operation modes are described in Tables 1 through 4.

Device Operation

Commands are used to initiate the memory φ eration functions of the device. Commands are written to the device using standard microprocesor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first. Note, during the software data protection sequence the address are latched on the rising edge of OE# or CE#, which-ever occurs first.

Command Definitions

Table 3 contains a command list and a brief summary of the commands. The following is a detailed description of the operations initiated by each command.



Sector_Erase Operation

The Sector_Erase operation erases all bytes within a sector and is initiated by a setup command and an execute command. A sector contains 256 bytes. This sector erasability enhances the flexibility and usefulness of the 28LF040, since most applications only need to change a small number of bytes or sectors, not the entire chip.

The setup command is performed by writing 20H to the device. The execute command is performed by writing D0H to the device. The erase operation begins with the rising edge of the WE# or CE#, whichever occurs first and terminates automaically by using an internal timer. The end of Erase can be determined using either Data# Polling, Toggle Bit, or Successive Reads detection mehods. See Figure 9 for timing waveforms.

The two-step sequence of setup command folowed by an execute command ensures that only memory contents within the addressed sector are erased and other sectors are not inadvertently erased.

Sector_Erase Flowchart Description

Fast and reliable erasing of the memory contents within a sector is accomplished by following the sector erase flowchart as shown in Figure 18. The entire procedure consists of the execution of two commands. The Sector_Erase operation will terminate after a maximum of 4 ms. A Reset command can be executed to terminate the erase operation; however, if the erase operation is terminated prior to the 4 ms time-out, the sector may not be fully erased. An erase command can be reissued as many times as necessary to complete the erase operation. The 28LF040 cannot be "overerased".

Chip_Erase Operation

The Chip_Erase operation is initiated by a setup command (30H) and an execute command (30H). The Chip_Erase operation allows the entire array of the 28LF040 to erase in one operation, as φ -posed to 2048 sector erase operations. Using the Chip_Erase operation will minimize the time to rewrite the entire memory array. The Chip_Erase operation will terminate after a maximum of 20 ms. A Reset command can be executed to termi-

nate the erase operation; however, if the erase operation is terminated prior to the 20 ms timeout, the Chip may not be completely erased. If an erase error occurs an erase command can be **e**issued as many times as necessary to complete the erase operation. The 28LF040 cannot be "overerased". (See Figure 8)

Byte_Program Operation

The Byte_Program operation is initiated by writing the setup command (10H). Once the program setup is performed, programming is executed by the next WE# pulse. See Figures 5 and 6 for tining waveforms. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first, and begins the program operation. The program operation is terminated automatically by an internal timer. See Figure 16 for the programming flowchart.

The two-step sequence of a setup command folowed by an execute command ensures that only the addressed byte is programmed and other bytes are not inadvertently programmed.

The Byte_Program Flowchart Description

Programming data into the 28LF040 is accomplished by following the Byte_Program flowchart shown in Figure 16. The Byte_Program command sets up the byte for programming. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first and begins the program operation. The end of program can be detected using either the Data# Polling, Toggle bit, or Successive reads.

Reset Operation

The Reset command is provided as a means to safely abort the erase or program command sequences. Following either setup commands (erase or program) with a write of FFH will safely abort the operation. Memory contents will not be altered. After the Reset command, the device eturns to the read mode. The Reset command does not enable software data protection. See Figure 7 for timing waveforms.

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Read

The Read operation is initiated by setting CE#, and OE# to logic low and setting WE# to logic high (See Table 2). See Figure 4 for read memory timing waveform. The read operation from the host retrieves data from the array. The device emains enabled for read until another operation mode is accessed. During initial power-up, the device is in the read mode and is software data protected. The device must be unprotected to execute a write command.

The read operation of the 28LF040 is controlled by OE# and CE# at logic low. When CE # is high, the chip is deselected and only standby power will be consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when CE# and OE# are high.

Read_ID operation

The Read_ID operation is initiated by writing a single command (90H). A read of address 0000H will output the manufacturer's code (BFH). A read of address 0001H will output the device code (04H). Any other valid command will terminate this operation.

Data Protection

In order to protect the integrity of nonvolatile data storage, the 28LF040 provides both hardware and software features to prevent inadvertent writes to the device, for example, during system power-up or power-down. Such provisions are described below.

Hardware Data Protection

The 28LF040 is designed with hardware features to prevent inadvertent writes. This is done in the following ways:

- 1. Write Inhibit Mode: OE# low, CE#, or WE# high will inhibit the write opeation.
- 2. Noise/Glitch Protection: A WE# pulse width of less than 15 ns will not initiate a write cycle.
- 3. V_{CC} Power Up/Down Detection: The write ϕ eration is inhibited when V_{CC} is less than 2.5V.

4. After power-up the device is in the read mode and the device is in the software data protect state.

Software Data Protection (SDP)

The 28LF040 has software methods to further prevent inadvertent writes. In order to perform an erase or program operation, a two-step command sequence consisting of a set-up command followed by an execute command avoids inadvertent erasing and programming of the device.

The 28LF040 will default to software data protection after power up. A sequence of seven consecutive reads at specific addresses will unprotect the device The address sequence is 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 041AH. The address bus is latched on the rising edge of OE# or CE#, whichever occurs first. A similar seven read sequence of 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 040AH will protect the device. Also refer to Figures 10 and 11 for the 7 read cycle sequence Software Data Protection. The I/O pins can be in any state (i.e., high, low, or tristate).

Write Operation Status Detection

The 28LF040 provides three means to detect the completion of a write cycle, in order to optimize the system write cycle time. The end of a write cycle (erase or program) can be detected by three means: 1) monitoring the Data# Polling bit; 2) monitoring the Toggle bit; or 3) by two successive read of the same data. These three detection mechanisms are described below.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simulaneous with the completion of the write cycle. If this occurs, the system may possibly get an eroneous result, i.e., valid data may appear to conflict with the DQ used. In order to prevent spurious rejection, if an erroneous result occurs, the sofware routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

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Data# Polling (DQ₇)

The 28LF040 features Data# Polling to indicate the write operation status. During a write opeation, any attempt to read the last byte loaded during the byte-load cycle will receive the complement of the true data on DQr. Once the write cycle is completed, DQr will show true data. The device is then ready for the next operation. See Figure 12 for Data Polling timing waveforms. In order for Data# Polling to function correctly, the byte being polled must be erased prior to pogramming.

Toggle Bit (DQ₆)

An alternative means for determining the write operation status is by monitoring the Toggle Bit, DQ_6 . During a write operation, consecutive attempts to read data from the device will result in DQ_6 toggling between logic 0 (low) and logic 1 (high). When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 13 for Toggle Bit timing waveforms.

Successive Reads

An Alternative means for determining an end of a write cycle is by reading the same address for two consecutive data matches.

Product Identification

The Product Identification mode identifies the device as 28LF040 and the manufacturer as SST. This mode may be accessed by hardware and software operations. The hardware operation is typically used by an external programmer to identify the correct algorithm for the 28LF040. Users may wish to use the software operation to identify the device (i.e., using the device code). For details see Table 2 for the hardware operation and Figure 19 for the software operation. The manufacturer and device codes are the same for both operations.

Product Identification Table

	Byte	Data
Manufacturer Code	0000 H	BF H
Device Code	0001 H	04 H





Figure 1: Functional Block Diagram of SST 28LF040



Figure 2A: Standard Pin Assignments for 4 0-pin TSOP Packages

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Figure 2B: Standard Pin Assignments for 32-pin TSOP Packages



Figure 3: Pin Assignments for 32-pin Plastic DIPs and 32-pin PLCCs



Table 1: P	in Description	
Symbol	Pin Name	Functions
A ₁₈ -A ₈	Row Address Inputs	To provide memory addresses. Row addresses define a sector.
$A_7 - A_0$	Column Address Inputs	Selects the byte within the sector.
DQ_7 - DQ_0	Data Input/Output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE#, CE # is high.
CE#	Chip Enable	To activate the device when CE # is low. ⁽¹⁾
OE#	Output Enable	To gate the data output buffers. ⁽¹⁾
WE#	Write Enable	To control the write operations. ⁽¹⁾
Vcc	Power Supply	To provide 3.3-volt supply (± 0.3 V)
Vss	Ground	

Note: ⁽¹⁾This pin is considered an input for the purposes of the DC Operation Characteristics Table.

Mode	CE#	OE#	WE#	DQ	Address
Read	VIL	VIL	V _{IH}	D _{OUT}	A _{IN}
Byte Program	V _{IL}	VIH	VIL	D _{IN}	A _{IN,} See Table 3
Sector Erase	V _{IL}	V _{IH}	VIL	D _{IN}	A _{IN,} See Table 3
Standby	VIH	Х	Х	High Z	X
Write Inhibit	Х	V _{IL}	Х	High Z/ D _{OUT}	X
Write Inhibit	Х	Х	V _{IH}	High Z/ D _{OUT}	X
Software Chip Erase	VIL	VIH	VIL	D _{IN}	See Table 3
Product Identification					
Hardware Mode	V _{IL}	V _{IL}	V _{IH}	Manufacturer Code (BF)	$A_{18}-A_1=V_{1L}, A_9=V_H, A_0=V_{1L}$
				Device Code (04)	$A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IH}$
Software Mode	VIL	VIH	VIL		See Table 3
SDP Enable & Disable Mode	VIL	VIH	VIL		See Table 3
Reset	V _{IL}	VIH	VIL		See Table 3

Table 2: Operation Modes Selection



Table 3: Software Command Summary

Command Su mmary	Required	Setup Command Cycle			Execute Command C y- cle			SDP ⁽⁵⁾
	Cycle(s)	Type ⁽¹⁾	Addr ^{(2,3}	Data ⁽⁴⁾	Type ⁽¹⁾	Addr ^{(2,3}	Data ⁽⁴⁾	
Sector_Erase	2	W	Х	20H	W	SA	D0H	Ν
Byte_Program	2	W	Х	10H	W	PA	PD	Ν
Chip_Erase	2	W	Х	30H	W	Х	30H	Ν
Reset	1	W	Х	FFH				Y
Read_ID	3	W	Х	90H	R	(8)	(8)	Y
Software_Data_Protect	7	R	(6)					
Software_Data_Unprotect	7	R	(7)					

Notes:

- 1. Type definition: W = Write, R = Read, X= don't care
- Addr (Address) definition: SA = Sector Address = A₈ A₈, sector size = 256 bytes; A₇ A₀ = X for this command.
- 3. Addr (Address) definition: $PA = Program Address = A_8 A_0$.
- 4. Data definition: PD = Program Data, H = number in hex.
- 5. SDP = Software Data Protect mode using 7 Read CycleSequence.
 - a) Y = the operation can be executed with protection enabled
 - b) N = the operation cannot be executed with protection enabled
- 6. Refer to Figure 11 for the 7 Read Cycle sequence for Software_Data_Protect.
- 7. Refer to Figure 10 for the 7 Read Cycle sequence for Software_Data_Unprotect.
- 8. Address 0000H retrieves the manufacturer' code of BFH and address 0001H retrieves the device code of 04H.

Table 4: Memory Array Detail

Sector Select	Byte Select
A ₁₈ - A ₈	A ₇ - A ₀



Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the pertainal sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias	55°C to +125°C
Storage Temperature	65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential	0.5V to $V_{\text{CC}}\text{+}~0.5\text{V}$
Transient Voltage (<20 ns) on Any Pin to Ground Potential	1.0V to V_{CC} + 1.0V
Voltage on A9 Pin to Ground Potential	0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C)	1.0W
Through Soldering Temperature (10 Seconds)	300°C
Surface Mount Lead Soldering Temperature (3 Seconds)	.240°C
Output Short Circuit Current ¹⁾	100 mA
(1)	

Note: ⁽¹⁾ Outputs shorted for no more than one second. No more than one output shorted at a time.

Table 5: Operating Range

Range	Ambient Temp	V _{CC}
Commercial	0 °C to +70 °C	3.0V to 3.6V
Industrial	-40 °C to +85 °C	3.0V to 3.6V

Table 6: AC Conditions of Test

Input Rise/Fall Time	10 ns
Output Load	1 TTL Gate and $C_L = 100 \text{ pF}$
See Figures 14 and 15	

Table 7:	DC Operating Characteristics
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Symbo	Parameter	Limits		Units	Test Conditions
		Min	Мах	-	
I _{cc}	Power Supply Current				CE# = OE# =V _{IL} , WE# =V _{IH} , all I/Os open
	Read		10	mA	Address input = V_{IL}/V_{IH} , at f=1/T _{RC} Min. $V_{CC} = V_{CC}$ Max
	Program and Erase		25	mA	CE# =WE# =V _{IL} , OE# =V _{IH} V _{CC} =V _{CC} Max.
I _{SB1}	Standby V _{cc} Current (TTL in- put)		1	mA	$CE\# = OE\# = WE\# = V_{IH}, V_{CC} = V_{CC}$ Max
I _{SB2}	Standby V _{CC} Current (CMOS input)		20	μA	$CE\# = OE\# = WE\# = V_{CC} - 0.3V,$ $V_{CC}=V_{CC} Max$
ILI	Input Leakage Current		1	μA	$V_{IN} = GND$ to V_{CC} , $V_{CC} = V_{CC}$ Max.
I _{LO}	Output Leakage Current		10	μA	V_{OUT} =GND to V_{CC} , V_{CC} = V_{CC} Max.
V _{IL}	Input Low Voltage		0.8	V	$V_{CC} = V_{CC}$ Max.
V _{IH}	Input High Voltage	2.0		V	$V_{CC} = V_{CC}$ Max.
V _{OL}	Output Low Voltage		0.4	V	I_{OL} = 100 μ A, V_{CC} = V_{CC} Min.
V _{OH}	Output High Voltage	2.4		V	I_{OH} = -100 μ A, V_{CC} = V_{CC} Min.
V _H	Supervoltage for A_{θ}	11.6	12.4	V	CE#=OE#=V _{IL} ,WE#=V _{IH}
I _H	Supervoltage Current for A ₉		200	μΑ	$CE\#=OE\#=V_{IL,}WE\#=V_{IH,}A_{9}=V_{H}Max.$

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Table 8: Power-up Timings							
Symbol	Parameter	Maximum	Units				
T _{PU-READ} ⁽¹⁾	Power-up to Read Operation	10	ms				
T _{PU-WRITE} ⁽¹⁾	Power-up to Write Operation	10	ms				

Table 9: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}^{(1)}$	I/O Pin Capacitance	$V_{I/O} = 0V$	12 pF
C _{IN} ⁽¹⁾	Input Capacitance	$V_{IN} = 0v$	6 pF

Note: ⁽¹⁾This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 10: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N _{END}	Endurance	1,000 & 10,000 ⁽²⁾	Cycles	MIL-STD-883, Method 1033
$T_{DR}^{(1)}$	Data Retention	100	Years	MIL-STD-883, Method 1008
V _{ZAP_HBM} ⁽¹⁾	ESD Susceptibility	1000	Volts	MIL-STD-883, Method 3015
	Human Body Model			
V _{ZAP_MM} ⁽¹⁾	ESD Susceptibility	200	Volts	JEDEC Standard A115
	Machine Model			
I _{LTH} ⁽¹⁾	Latch Up	100	mA	JEDEC Standard 17

Note: ⁽¹⁾This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

⁽²⁾See Ordering Information for desired type.



AC Characteristics

Table 11: **Read Cycle Timing Parameters** IEEE 28LF040-200 28LF040-250 Industry Symbol Symbol Min Max Min Max Units Parameter tAVAV T_{RC} Read Cycle time 200 250 ns tAVQV Address Access Time 200 250 T_{AA} ns tELQV T_{CE} Chip Enable Access Time 200 250 ns tGLQV T_{OE} **Output Enable Access Time** 120 120 ns $T_{CLZ}^{(1)}$ tEHQZ CE# Low to Active Output 0 0 ns $T_{OLZ}^{(1)}$ $T_{CHZ}^{(1)}$ tGHQZ OE# Low to Active Output 0 0 ns tELQX CE# High to High-Z Output 60 60 ns T_{OHZ}⁽¹⁾ tGLQX OE# High to High-Z Output 60 60 ns Т_{ОН}⁽¹⁾ **Output Hold from Address Change** tAXQX 0 0 ns

Table 12: Erase/Program Cycle Timing Parameters

IEEE	Industry				
Symbol	Symbol	Parameter	Min	Max	Units
tAVA	T _{BP}	Byte Program Cycle Time		40	μs
tWLWH	T _{WP}	Write Pulse Width (WE#)	200		ns
tAVWL	T _{AS}	Address Setup Time	10		ns
tWLAX	T _{AH}	Address Hold Time	100		ns
tELWL	T _{CS}	CE# Setup Time	0		ns
tWHEX	Т _{СН}	CE# Hold Time	0		ns
tGHWL	T _{OES}	OE# High Setup Time	20		ns
tWGL	T _{OEH}	OE# High Hold Time	20		ns
tWLEH	T _{CP}	Write Pulse Width (CE#)	200		ns
tDVWH	T _{DS}	Data Setup Time	100		ns
tWHDX	T _{DH}	Data Hold Time	20		ns
tWHWL2	T _{SE}	Sector Erase Cycle Time		4	ms
	T _{RST} ⁽¹⁾	Reset Command Recovery Time		4	μs
tWHWL3	T _{SCE}	Software Chip_Erase Cycle Time		20	ms
tEHEL	T _{CPH}	CE# High Pulse Width	50		ns
tWHWL1	T _{WPH}	WE# High Pulse Width	50		ns
	$T_{PCP}^{(1)}$	Protect Chip Enable Pulse Width	20		ns
	T _{PCH} ⁽¹⁾	Protect Chip Enable High Time	20		ns
	T _{PAS} ⁽¹⁾	Protect Address Setup Time	0		ns
	T _{PAH} ⁽¹⁾	Protect Address Hold Time	100		ns

Note: ⁽¹⁾This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

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Figure 5: WE# Controlled Byte Program Timing Diagram







Figure 7: Reset Command Timing Diagram

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Figure 11: Software Data Protect Timing Diagram



NOTE: THIS TIME INTERVAL SIGNAL CAN BE TSE OR TBP DEPENDING UPON THE SELECTED OPERATION MODE.

Figure 12: Data# Polling Timing Diagram



Note: This time interval signal can be T_{SE} or T_{BP} , depending upon the selected operation mode.







Figure 14: AC Input/Output Reference Wav eform



Figure 15: Test Load Example

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Figure 16: Byte Program Flowchart





Figure 17: Write Wait Options





Figure 18: Sector_Erase Flowchart





Figure 19: Software Product ID Flow



Product Ordering Information





Valid combinations

SST28LF040-200-4C- EH	SST28LF040-200-4C- EI	SST28LF040-200-4C- NH
SST28LF040-250-4C- EH SST28LF040-250-4C- PH	SST28LF040-250-4C- EI SST28LF040-250-4C- U1	SST28LF040-250-4C- NH
SST28LF040-200-3C- EH SST28LF040-200-3C- PH	SST28LF040-200-3C- EI	SST28LF040-200-3C- NH
SST28LF040-250-3C- EH SST28LF040-250-3C- PH	SST28LF040-250-3C- EI SST28LF040-250-3C- U1	SST28LF040-250-3C- NH
SST28LF040-200-4I- EH SST28LF040-250-4I- EH	SST28LF040-200-4I- EI SST28LF040-250-4I- EI	SST28LF040-200-4I- NH SST28LF040-250-4I- NH

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.