CONTENTS

1 FEATURES

- DTMF, modem and musical tone generation
- Stabilized output voltage level
- Low output distortion with on-chip filtering conforming to CEPT recommendations
- Latched inputs for data bus applications
- I^2C-bus compatible
- Selection of parallel or serial (I^2C-bus) data input (PCD3311C).

2 GENERAL DESCRIPTION

The PCD3311C and PCD3312C are single-chip silicon gate CMOS integrated circuits. They are intended principally for use in telephone sets to provide the dual-tone multi-frequency (DTMF) combinations required for tone dialling systems. The various audio output frequencies are generated from an on-chip 3.58 MHz quartz crystal-controlled oscillator. A separate crystal is used, and a separate microcontroller is required to control the devices.

Both the devices can interface to I^2C-bus compatible microcontrollers for serial input. The PCD3311C can also interface directly to all standard microcontrollers, accepting a binary coded parallel input.

With their on-chip voltage reference the PCD3311C and PCD3312C provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with CEPT recommendations.

In addition to the standard DTMF frequencies the devices can also provide:

- Twelve standard frequencies used in simplex modem applications for data rates from 300 to 1200 bits per second
- Two octaves of musical scales in steps of semitones.

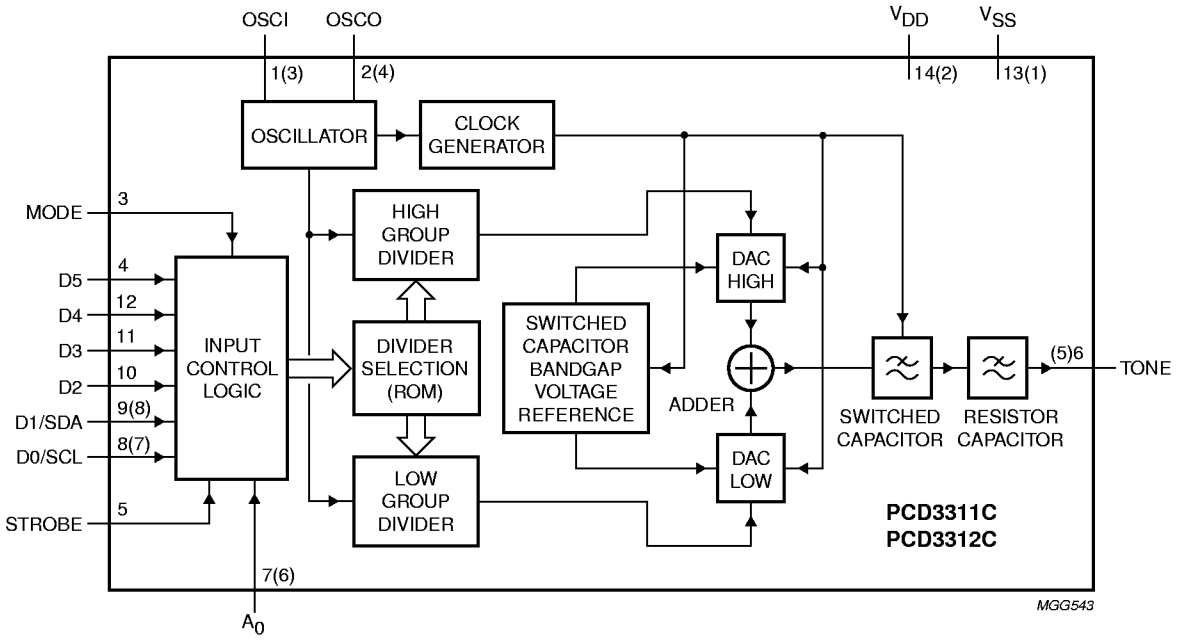
3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage	2.5	–	6.0	V
I_{DD}	operating supply current	–	–	0.9	mA
I_{stb}	standby current	–	–	3	µA
$V_{HG(RMS)}$	DTMF HIGH group output voltage level (RMS value)	158	192	205	mV
$V_{LG(RMS)}$	DTMF LOW group output voltage level (RMS value)	125	150	160	mV
G_v	pre-emphasis (voltage gain) of group	1.85	2.10	2.35	dB
THD	total harmonic distortion	–	–25	–	dB
T_{amb}	operating ambient temperature	–25	–	+70	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3311CP	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
PCD3311CT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCD3312CP	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCD3312CT	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1

5 BLOCK DIAGRAM



The un-parenthesised numbers are for the PCD3311CP, those in parenthesis for the PCD3312C.

Fig.1 Block diagram.

6 PINNING INFORMATION

6.1 Pinning PCD3311CP

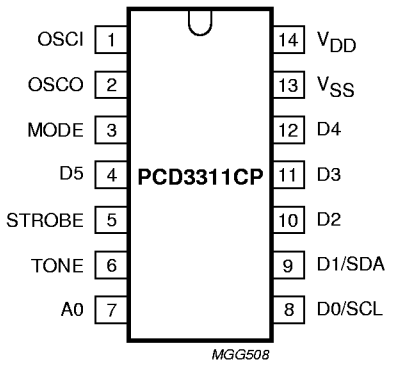


Fig.2 Pin configuration PCD3311CP.

6.2 Pin description PCD3311CP

SYMBOL	PIN	TYPE	DESCRIPTION
OSCI	1	I	oscillator input
OSCO	2	O	oscillator output
MODE	3	I	mode select input (selects I^2C or parallel data input)
D5	4	I	parallel data input
STROBE	5	I	strobe input (for loading data in parallel mode)
TONE	6	O	frequency output (DTMF, modem, musical tones)
A0	7	I	slave address input (to be connected to V_{DD} or V_{SS})
D0/SCL	8	I	parallel data input or I^2C-bus clock line
D1/SDA	9	I	parallel data input or I^2C-bus data line
D2 – D4	10 – 12	I	parallel data inputs
V_{SS}	13	P	negative supply
V_{DD}	14	P	positive supply

6.3 Pinning PCD3311CT

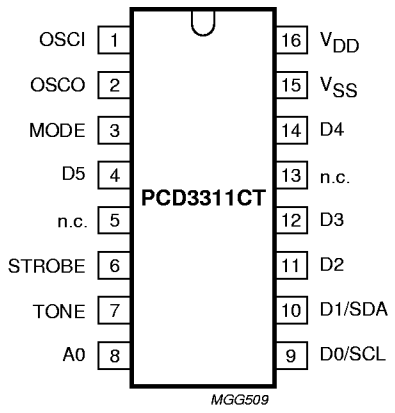


Fig.3 Pin configuration PCD3311CT.

6.4 Pin description PCD3311CT

SYMBOL	PIN	TYPE	DESCRIPTION
OSCI	1	I	oscillator input
OSCO	2	O	oscillator output
MODE	3	I	mode select input (selects I^2C or parallel data input)
D5	4	I	parallel data input
n.c.	5	–	not connected
STROBE	6	I	strobe input (for loading data in parallel mode)
TONE	7	O	frequency output (DTMF, modem, musical tones)
A0	8	I	slave address input (to be connected to V_{DD} or V_{SS})
D0/SCL	9	I	parallel data input or I^2C-bus clock line
D1/SDA	10	I	parallel data input or I^2C-bus data line
D2, D3	11, 12	I	parallel data inputs
n.c.	13	–	not connected
D4	14	I	parallel data input
V_{SS}	15	P	negative supply
V_{DD}	16	P	positive supply

6.5 Pinning PCD3312C

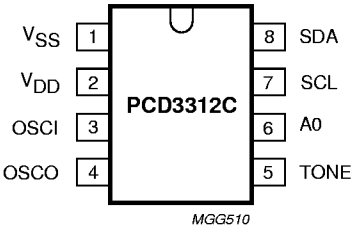


Fig.4 Pin configuration PCD3312C.

6.6 Pin description PCD3312C

SYMBOL	PIN	TYPE	DESCRIPTION
V_{SS}	1	P	negative supply
V_{DD}	2	P	positive supply
OSCI	3	I	oscillator input
OSCO	4	O	oscillator output
TONE	5	O	frequency output (DTMF, modem, musical tones)
A0	6	I	slave address input (to be connected to V_{DD} or V_{SS})
SCL	7	I	I^2C-bus clock line
SDA	8	I	I^2C-bus data line

7 FUNCTIONAL DESCRIPTION

7.1 General (see Fig.1)

The Input Control Logic decodes the input data to determine whether DTMF, modem or musical tones are selected; and which particular tone or combination of tones is required.

A code representing the required tones is sent to the Divider Selection ROM which selects the correct division ratio in both of the Frequency Dividers (or in one divider, if only a single tone is required).

The Oscillator circuit provides a square wave of frequency 3.58 MHz. Each Frequency Divider divides the frequency of the Oscillator to give a serial digital square wave with a frequency simply related to that of the required tone.

The output from each Frequency Divider goes to a DAC, which is also fed by a clock derived from the oscillator. Using these two signals, the DAC produces an approximate sine wave of the required frequency, with an amplitude derived from the Voltage Reference.

The output from the DAC goes to an Adder where, for DTMF, it is combined with the output from the other DAC.

The output from the Adder goes through two stages of Low Pass Filters to give a smoothed tone (single or dual), and finally to the TONE output.

7.2 Clock/oscillator connection

The timebase for the PCD3311C and PCD3312C is a crystal-controlled oscillator, requiring a 3.58 MHz quartz crystal to be connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock of 3.58 MHz.

7.3 Mode selection (PCD3311C)

The MODE input selects the data input mode for the PCD3311C. When MODE is connected to V_{DD} (HIGH), data can be received in the parallel mode. When connected to V_{SS} (LOW) or left open, data can be received via the serial I^2C-bus.

PCD 3312C has no MODE input as data input is via the I^2C-bus only.

7.4 Data inputs (PCD3311C)

Inputs D0, D1, D2, D3, D4 and D5 are used in the parallel data input mode of the PCD3311C. Inputs D0 and D1 are also used in serial input mode when they act as the SCL and SDA inputs respectively. Inputs D0 and D1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D2, D3, D4 and D5 have internal pull-down.

D4 and D5 are used to select between DTMF dual, DTMF single, modem and musical tones (see Table 1). D0, D1, D2 and D3 select the tone combination or single tone within the selected application. They also, in combination with D4, select the standby mode. See Tables 2, 3, 4 and 5.

PCD 3312C has no parallel data pins as data input is via the I^2C-bus.

Table 1 Use of D5 and D4 to select application

D5	D4	APPLICATION
LOW	LOW	DTMF single tones; musical tones; standby
LOW	HIGH	DTMF dual tones (all 16 combinations)
HIGH	LOW	modem tones
HIGH	HIGH	musical tones

7.5 Strobe input (PCD3311C)

The STROBE input (with internal pull-down) allows the loading of parallel data into D0 to D5 when MODE is HIGH.

The data inputs must be stable preceding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received. Figure 5 is an example of the timing relationship between STROBE and the data inputs.

When MODE is LOW, data is received serially via the I^2C-bus.

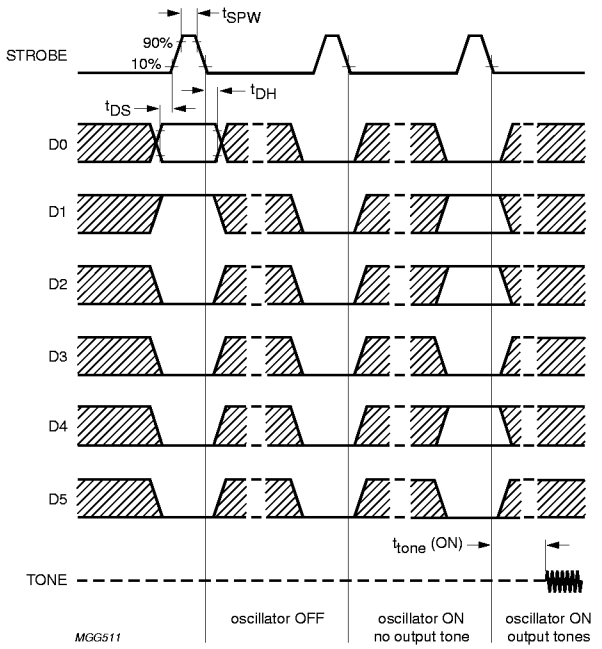


Fig.5 Timing of STROBE, parallel data inputs and TONE output (770 Hz + 1477 Hz in example) in the parallel mode (MODE = HIGH).

7.6 I²C-bus clock and data inputs

SCL and SDA are the serial clock and serial data inputs according to the I²C-bus specification, see Chapter 8. SCL and SDA must be pulled up externally to V_{DD}.

For the PCD3311C, SCL and SDA are combined with parallel inputs D0 and D1 respectively - D0/SCL and D1/SDA operate serially only when MODE is LOW.

7.7 Address input

Address input A0 defines the least significant bit of the I²C-bus address of the device (see Fig.6). The first 6 bits of the address are fixed internally. By tying the A0 of each device to V_{DD} (HIGH) and V_{SS} (LOW) respectively, two different PCD3311C or PCD3312C devices can be individually addressed on the bus.

Whether one or two devices are used, A0 must be connected to V_{DD} or V_{SS}.

7.8 I²C-bus data configuration (see Fig.6)

The PCD3311C and PCD3312C are always slave receivers in the I²C-bus configuration. The R/$\overline{W}$ bit in is thus always LOW, indicating that the master (microcontroller) is writing.

The slave address in the serial mode consists of 7 bits: 6 bits internally fixed, 1 externally set via A0. in the serial mode, the same input data codes are used as in the parallel mode. See Tables 2, 3, 4 and 5.

7.9 Tone output

The single and dual tones provided at the TONE output are first filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. The filtered tones fulfil the CEPT recommendations for total harmonic distortion of DTMF tones. An on-chip reference voltage provides output tone levels independent of the supply voltage. Tables 3, 4 and 5 give the frequency deviation of the output tones with respect to the standard DTMF, modem and music frequencies.

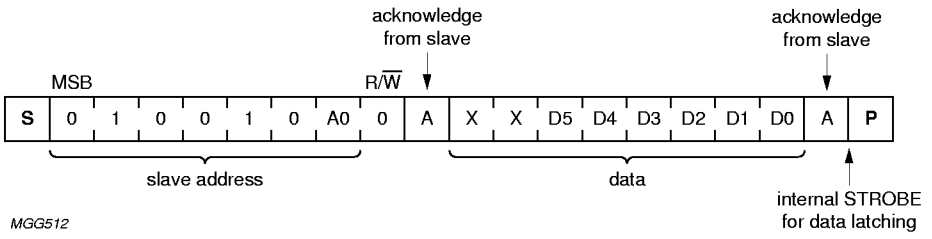


Fig.6 I²C-bus data format.

7.10 Power-on reset

In order to avoid an undefined state when the power is switched ON, the devices have an internal reset circuit which sets the standby mode (oscillator OFF).

7.11 TABLES OF INPUT AND OUTPUT

The specified output tones are obtained when a 3.579545 MHz crystal is used.

In each table, the logical states for the input data lines are related to voltage levels as follows:

1 = HIGH = V_{DD}

0 = LOW = V_{SS}

X = don't care

Table 2 Input data for no output tone, TONE in 3-state

D5	D4	D3	D2	D1	D0	HEX(1)	OSCILLATOR
X	0	0	0	0	0	00 or 20	ON
X	0	0	0	0	1	01 or 21	OFF
X	0	0	0	1	0	02 or 22	OFF
X	0	0	0	1	1	03 or 23	OFF

Note

1. The alternative HEX values depend on the value of D5.

Table 3 Input data and output for DTMF tones

D5	D4	D3	D2	D1	D0	HEX	SYMBOL	STANDARD FREQUENCY	TONE OUTPUT FREQ.	FREQUENCY DEVIATION	
								Hz	Hz	%	Hz
0	0	1	0	0	0	08	–	697	697.90	+0.13	+0.90
0	0	1	0	0	1	09	–	770	770.46	+0.06	+0.46
0	0	1	0	1	0	0A	–	852	850.45	–0.18	–1.55
0	0	1	0	1	1	0B	–	941	943.23	+0.24	+2.23
0	0	1	1	0	0	0C	–	1209	1206.45	–0.21	–2.55
0	0	1	1	0	1	0D	–	1336	1341.66	+0.42	+5.66
0	0	1	1	1	0	0E	–	1477	1482.21	+0.35	+5.21
0	0	1	1	1	1	0F	–	1633	1638.24	+0.32	+5.24
0	1	0	0	0	0	10	0	941+1336	–	–	–
0	1	0	0	0	1	11	1	697+1209	–	–	–
0	1	0	0	1	0	12	2	697+1336	–	–	–
0	1	0	0	1	1	13	3	697+1477	–	–	–
0	1	0	1	0	0	14	4	770+1209	–	–	–
0	1	0	1	0	1	15	5	770+1336	–	–	–
0	1	0	1	1	0	16	6	770+1477	–	–	–
0	1	0	1	1	1	17	7	852+1209	–	–	–
0	1	1	0	0	0	18	8	852+1336	–	–	–
0	1	1	0	0	1	19	9	852+1477	–	–	–
0	1	1	0	1	0	1A	A	697+1633	–	–	–
0	1	1	0	1	1	1B	B	770+1633	–	–	–
0	1	1	1	0	0	1C	C	852+1633	–	–	–
0	1	1	1	0	1	1D	D	941+1633	–	–	–
0	1	1	1	1	0	1E	*	941+1209	–	–	–
0	1	1	1	1	1	1F	#	941+1477	–	–	–

Table 4 Input data and output for modem tones

D5	D4	D3	D2	D1	D0	HEX	STANDARD FREQUENCY	TONE OUTPUT FREQ.	FREQUENCY DEVIATION		TELECOM. STANDARD
							Hz	Hz	%	Hz	
1	0	0	1	0	0	24	1300	1296.94	–0.24	–3.06	V.23
1	0	0	1	0	1	25	2100	2103.14	+0.15	+3.14	
1	0	0	1	1	0	26	1200	1197.17	–0.24	–2.83	Bell 202
1	0	0	1	1	1	27	2200	2192.01	–0.36	–7.99	
1	0	1	0	0	0	28	980	978.82	–0.12	–1.18	V.21
1	0	1	0	0	1	29	1180	1179.03	–0.08	–0.97	

D5	D4	D3	D2	D1	D0	HEX	STANDARD FREQUENCY	TONE OUTPUT FREQ.	FREQUENCY DEVIATION		TELECOM. STANDARD
							Hz	Hz	%	Hz	
1	0	1	0	1	0	2A	1070	1073.33	+0.31	+3.33	Bell 103
1	0	1	0	1	1	2B	1270	1265.30	−0.37	−4.70	
1	0	1	1	0	0	2C	1650	1655.66	+0.34	+5.66	V.21
1	0	1	1	0	1	2D	1850	1852.77	+0.15	+2.77	
1	0	1	1	1	0	2E	2025	2021.20	−0.19	−3.80	Bell 103
1	0	1	1	1	1	2F	2225	2223.32	−0.08	−1.68	

Table 5 Input/output for musical tones

D5	D4	D3	D2	D1	D0	HEX	NOTE	STD. FREQ. BASED ON A4 = 440 Hz	TONE OUTPUT FREQUENCY
								Hz	Hz
1	1	0	0	0	0	30	D#5	622.3	622.5
1	1	0	0	0	1	31	E5	659.3	659.5
1	1	0	0	1	0	32	F5	698.5	697.9
1	1	0	0	1	1	33	F#5	740.0	741.1
1	1	0	1	0	0	34	G5	784.0	782.1
1	1	0	1	0	1	35	G#5	830.6	832.3
1	1	0	1	1	0	36	A5	880.0	879.3
1	1	0	1	1	1	37	A#5	932.3	931.9
1	1	1	0	0	0	38	B5	987.8	985.0
1	1	1	0	0	1	39	C6	1046.5	1044.5
1	1	1	0	1	0	3A	C#6	1108.7	1111.7
1	0	1	0	0	1	29	D6	1174.7	1179.0
1	1	1	0	1	1	3B	D#6	1244.5	1245.1
1	1	1	1	0	0	3C	E6	1318.5	1318.9
1	1	1	1	0	1	3D	F6	1396.9	1402.1
0	0	1	1	1	0	0E	F#6	1480.0	1482.2
1	1	1	1	1	0	3E	G6	1568.0	1572.0
1	0	1	1	0	0	2C	G#6	1661.2	1655.7
1	1	1	1	1	1	3F	A6	1760.0	1768.5
0	0	0	1	0	0	04	A#6	1864.7	1875.1
0	0	0	1	0	1	05	B6	1975.5	1970.0
1	0	0	1	0	1	25	C7	2093.0	2103.1
1	0	1	1	1	1	2F	C#7	2217.5	2223.3
0	0	1	1	1	0	06	D7	2349.3	2358.1
0	0	0	1	1	1	07	D#7	2489.0	2470.4

8 I²C-BUS INTERFACE

The I²C-bus is for two-way communication between different ICs or modules. It uses only two lines, a serial data line (SDA) and a serial clock line (SCL), both of which are bi-directional. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 **Bit transfer** (see Fig.7)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

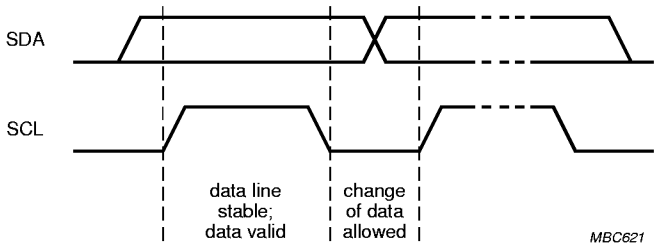


Fig.7 Bit transfer.

8.2 **Start and stop conditions** (see Fig.8)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

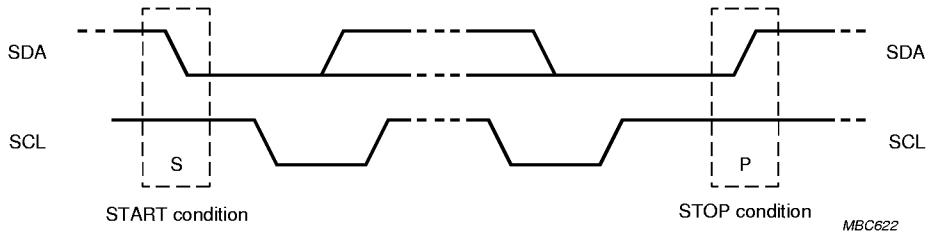


Fig.8 Start and stop conditions.

8.3 System configuration (see Fig.9)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls message transfer is the 'master' and the devices that are controlled by the master are the 'slaves'.

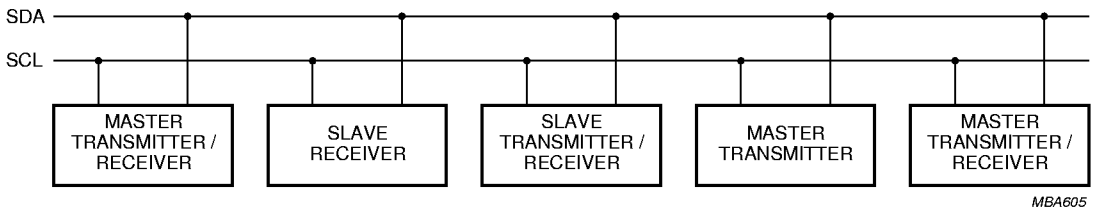


Fig.9 System configuration.

8.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge after the reception of each byte. Also a master must generate an acknowledge after reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge-related clock pulse. Set-up and hold times must be taken into account to ensure that the SDA line is stable LOW during the whole HIGH period of the acknowledge-related clock pulse. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate the stop condition.

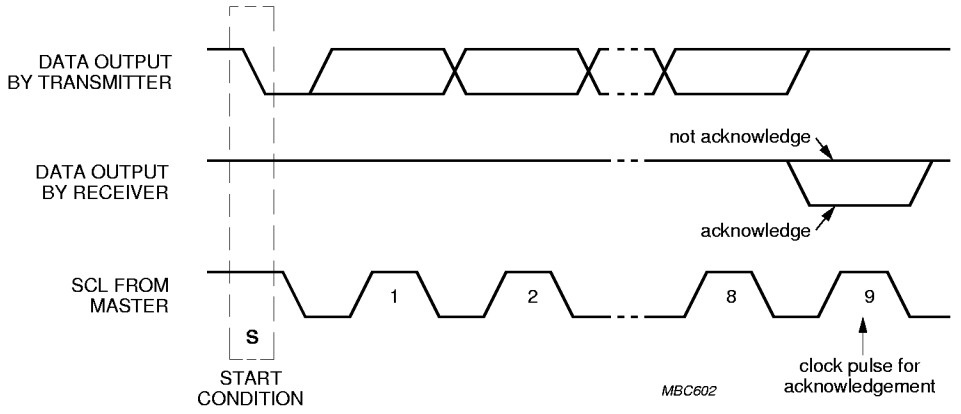


Fig.10 Acknowledgment on the I^2C-bus.

8.5 Timing specifications

The PCD3311C and PCD3312C accept data input from a microcontroller and are 'slave receivers' when operating via the I²C-bus. They support the 'standard' and 'low-speed' modes of the I²C-bus, but not the 'fast' mode detailed in *"The I²C-bus and how to use it"* document order no. 9398 393 40011. The timing requirements for the devices are described in Sections 8.5.1 and 8.5.2.

8.5.1 STANDARD MODE

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig.11, where the two signal levels are LOW = V_{IL} and HIGH = V_{IH}, see Chapter 11. Figure 12 shows a complete data transfer in standard mode. The time symbols are explained in Table 6.

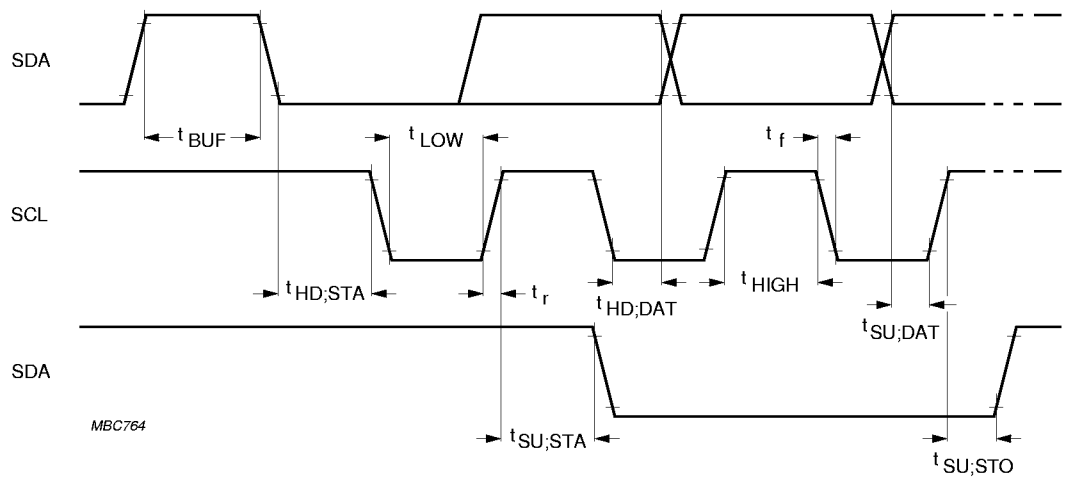
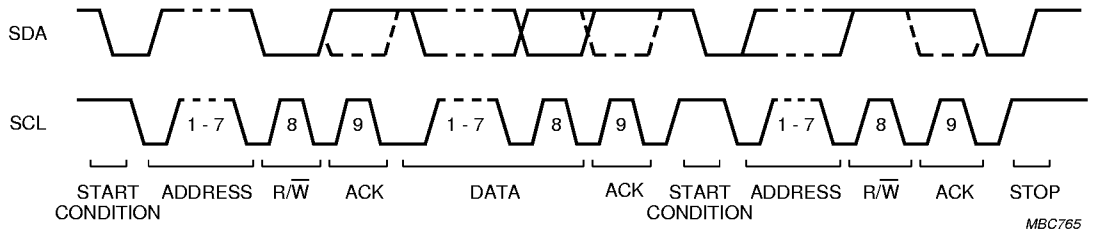


Fig.11 Standard mode timing.



Clock LOW minimum = 4.7 μs; clock HIGH minimum = 4 μs.
The dashed line is the acknowledgment of the receiver.
Mark-to-space ratio = 1 : 1 (LOW-to-HIGH).
Maximum number of bytes is unrestricted.
Premature termination of transfer is allowed by generation of STOP condition.
Acknowledge clock bit must be provided by master.

Fig.12 Complete data transfer in standard mode.

Table 6 Explanation of time symbols used in Fig.11

SYMBOL	PARAMETER	REMARKS	MIN.	MAX.	UNIT
f_{SCL}	SCL clock frequency		0	100	kHz
t_{SW}	tolerable pulse spike width		–	100	ns
t_{BUF}	bus free time	The time that the bus is free (SDA is HIGH) before a new transmission is initiated by SDA going LOW.	4.7	–	μs
$t_{SU;STA}$	set-up time repeated START	Only valid for repeated start code.	4.7	–	μs
$t_{HD;STA}$	hold time START condition	The time between SDA going LOW and the first valid negative-going transition of SCL.	4.0	–	μs
t_{LOW}	SCL LOW time	The LOW period of the SCL clock.	4.7	–	μs
t_{HIGH}	SCL HIGH time	The HIGH period of the SCL clock.	4.0	–	μs
t_r	rise time SDA and SCL		–	1.0	μs
t_f	fall time SDA and SCL		–	0.3	μs
$t_{SU;DAT}$	data set-up time		250	–	ns
$t_{HD;DAT}$	data hold time		0	–	ns
$t_{SU;STO}$	set-up time STOP condition		4.0	–	μs

8.5.2 LOW-SPEED MODE

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig.13, where the two signal levels are LOW = V_{IL} and HIGH = V_{IH}, see Chapter 11. Figure 14 shows a complete data transfer in low-speed mode.The time symbols are explained in Table 7.

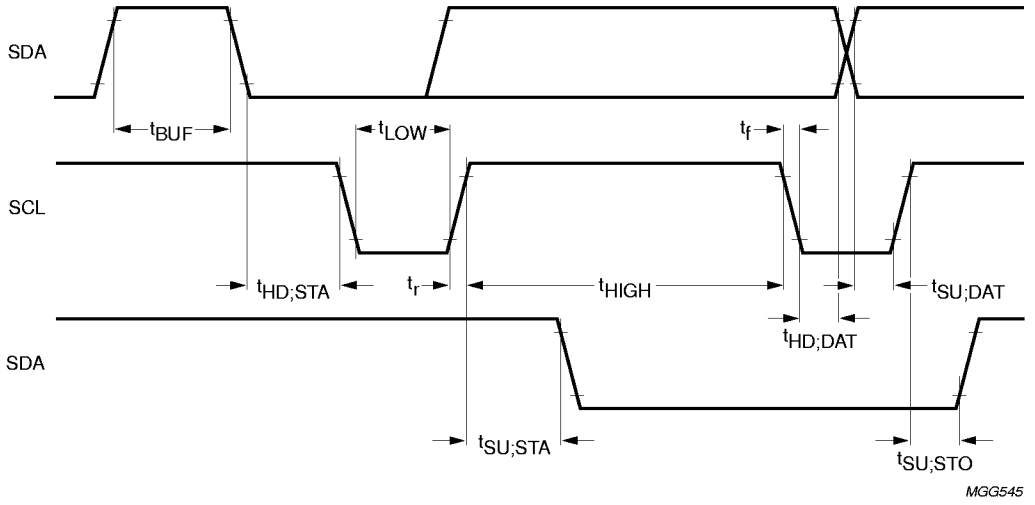
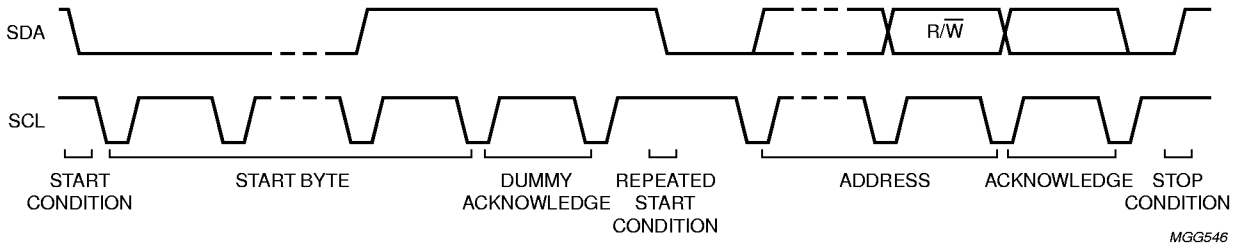


Fig.13 Low-speed mode timing.



Clock LOW minimum = 130 µs ±25 µs; clock HIGH minimum 390 µs ±25 µs.
Mark-to-space ratio = 1 : 3 (LOW-to-HIGH).
Start byte 0000 0001.
Maximum number of bytes = 6.
Premature termination of transfer not allowed.
Acknowledge clock bit must be provided by master.

Fig.14 Complete data transfer in low speed mode.

Table 7 Explanation of time symbols used in Fig.13

SYMBOL	PARAMETER	REMARKS	MIN.	MAX.	UNIT
f_{SCL}	SCL clock frequency		0	2	kHz
t_{SW}	tolerable pulse spike width		–	100	ns
t_{BUF}	bus free time	The time that the bus is free (SDA is HIGH) before a new transmission is initiated by SDA going LOW.	105	–	µs
$t_{SU;STA}$	set-up time repeated START	Only valid for repeated start code.	105	155	µs
$t_{HD;STA}$	hold time START condition	The time between SDA going LOW and the first valid negative-going transition of SCL.	365	415	µs
t_{LOW}	SCL LOW time	The LOW period of the SCL clock.	105	155	µs
t_{HIGH}	SCL HIGH time	The HIGH period of the SCL clock.	365	–	µs
t_r	rise time SDA and SCL		–	1.0	µs
t_f	fall time SDA and SCL		–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	ns
$t_{HD;DAT}$	data hold time		0	–	ns
$t_{SU;STO}$	set-up time STOP condition		105	155	µs

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handbook IC03, Section: General, Handling MOS devices"*).

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.8	+8.0	V
V_I	all input voltages	–0.8	V_{DD} + 0.8	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
P_{tot}	total power dissipation	–	300	mW
P_O	power dissipation per output	–	50	mW
I_{DD}	supply current through pin V_{DD}	–50	+50	mA
I_{SS}	supply current through pin V_{SS}	–50	+50	mA
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature	–25	+70	°C

11 CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz (g_{mL}); maximum series resistance = 50 Ω; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	operating supply voltage	2.5	–	6.0	V
I_{DD}	operating supply current (note 1)				
	no output tone	–	50	100	µA
	single output tone	–	0.5	0.8	mA
	dual output tone	–	0.6	0.9	mA
I_{stb}	static standby current (note 2)	–	–	3	µA
Inputs/outputs (SDA)					
D0 TO D5; MODE; STROBE					
V_{IL}	LOW level input voltage	0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	$0.7V_{DD}$	–	V_{DD}	V
D2 TO D5 MODE; STROBE; A0					
I_{IL}	pull-down input current; $V_I = V_{DD}$	–30	–150	–300	nA
SCL (D0); SDA (D1)					
I_{OL}	LOW level output current (SDA); V_{OL} = 0.4 V	3	–	–	mA
f_{SCL}	SCL clock frequency	–	–	100	kHz
C_i	input capacitance; $V_I = V_{SS}$	–	–	7	pF
t_i	allowable input spike pulse width	–	–	100	ns

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
TONE output (see test circuit, Fig.15)					
$V_{HG(RMS)}$	DTMF output voltage (RMS), HIGH group	158	192	205	mV
$V_{LG(RMS)}$	DTMF output voltage (RMS), LOW group	125	150	160	mV
V_{DC}	DC voltage level	–	$\frac{1}{2} V_{DD}$	–	V
G_v	voltage gain (pre-emphasis) of group	1.85	2.10	2.35	dB
THD	Total Harmonic Distortion; T_{amb} = 25 °C				
	dual tone (note 3)	–	–25	–	dB
	modem tone (note 4)	–	–29	–	dB
$\|Z_o\|$	output impedance	–	0.1	0.5	kΩ
OSCI input					
$V_{OSC(p-p)}$	maximum allowable amplitude at OSCI	–	–	$V_{DD} - V_{SS}$	V
Timing (V_{DD} = 3 V)					
$t_{OSC(ON)}$	oscillator start-up time	–	3	–	ms
$t_{TONE(ON)}$	TONE start-up time (note 5)	–	0.5	–	ms
t_{SPW}	STROBE pulse width (note 6)	400	–	–	ns
t_{DS}	data set-up time (note 6)	150	–	–	ns
t_{DH}	data hold time (note 6)	100	–	–	ns

Notes

1. Oscillator ON; V_{DD} = 3 V; crystal connected between OSCI and OSCO; D0/SCL and D1/SDA connected via resistance of 5.6 kΩ to V_{DD}; all other pins left open.
2. As note 1, but with oscillator OFF.
3. Related to the level of the LOW group frequency component, according to CEPT recommendations.
4. Related to the level of the fundamental frequency.
5. Oscillator must be running.
6. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

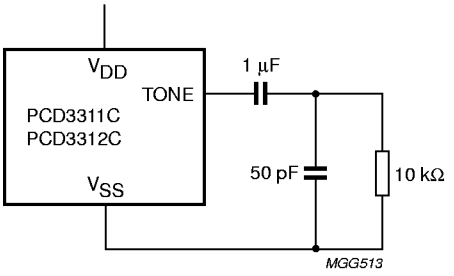


Fig.15 TONE output test circuit.

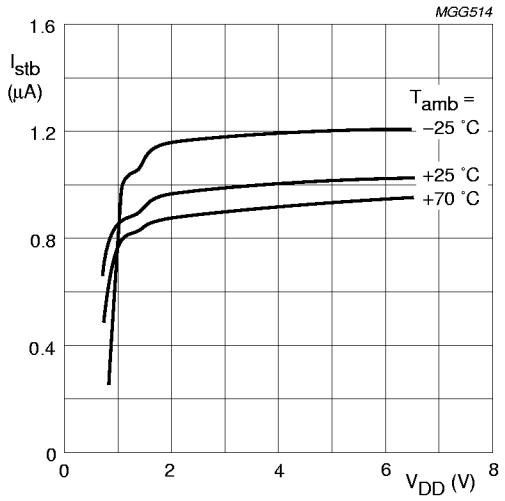


Fig.16 Standby supply current as a function of supply voltage; oscillator OFF.

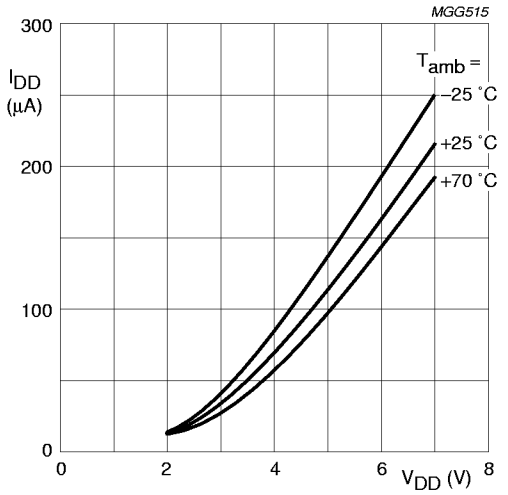


Fig.17 Operating supply current as a function of supply voltage; oscillator ON, no output at TONE.

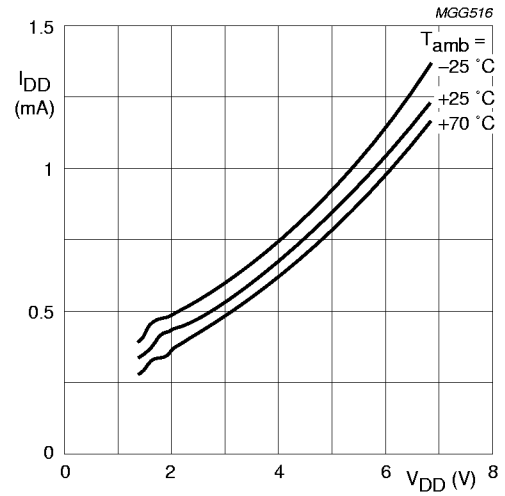


Fig.18 Operating supply current as a function of supply voltage; oscillator ON, dual tone at TONE.

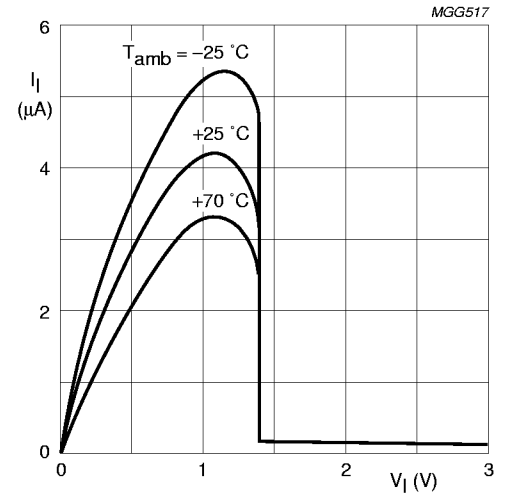


Fig.19 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

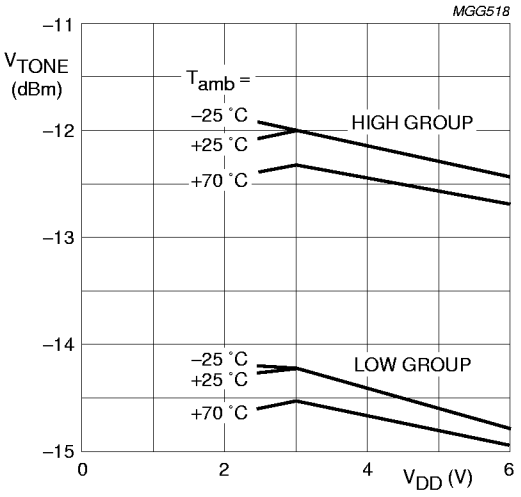


Fig.20 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

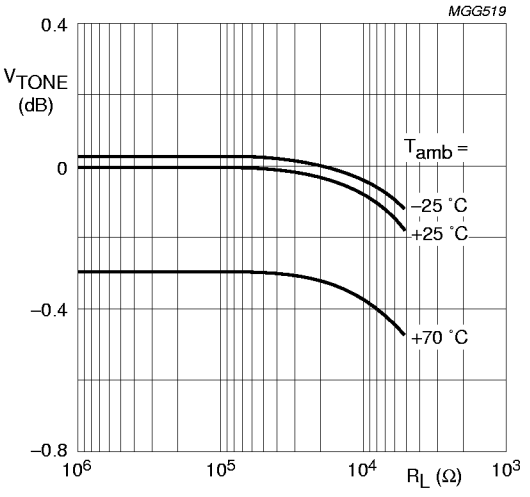


Fig.21 Dual tone output voltage level as a function of output load resistance.

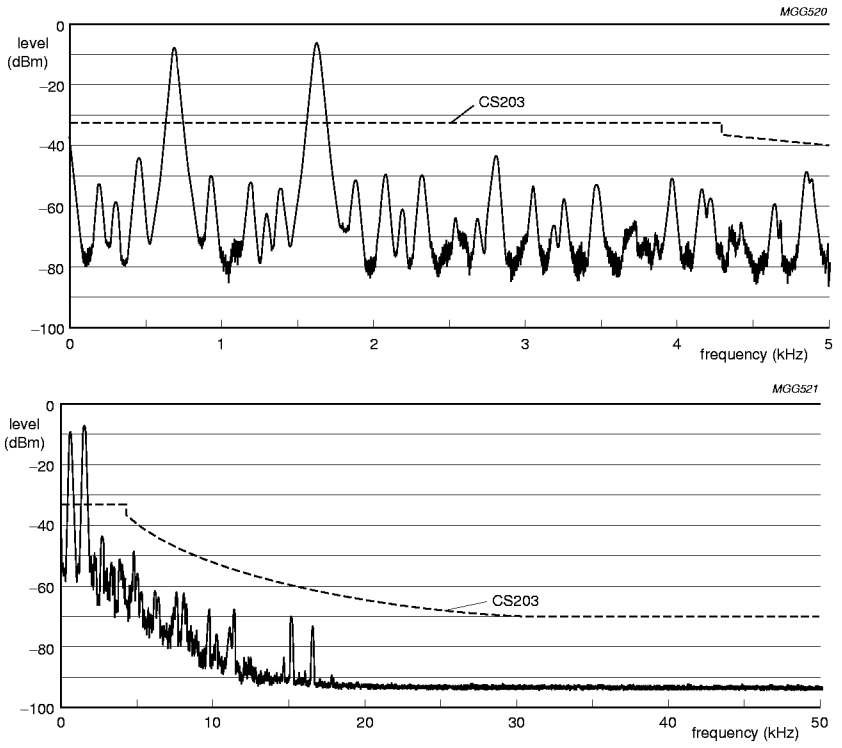


Fig.22 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

12 APPLICATION INFORMATION

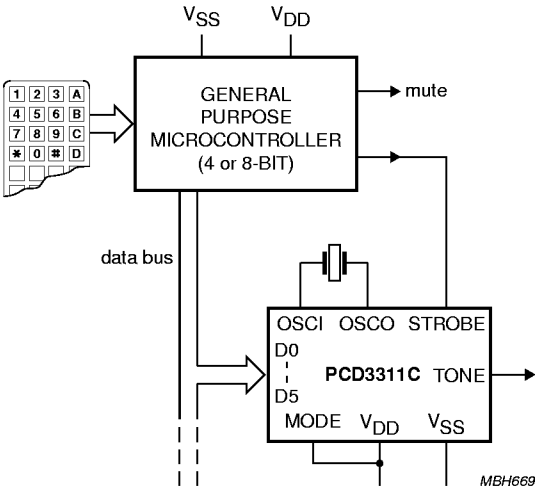


Fig.23 PCD3311C driven by microcontroller with parallel data bus.

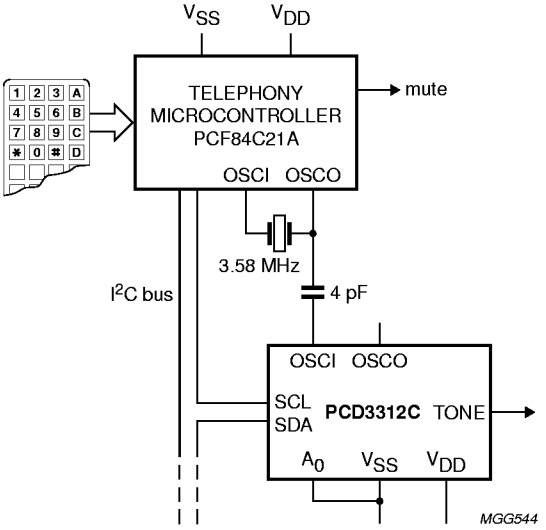
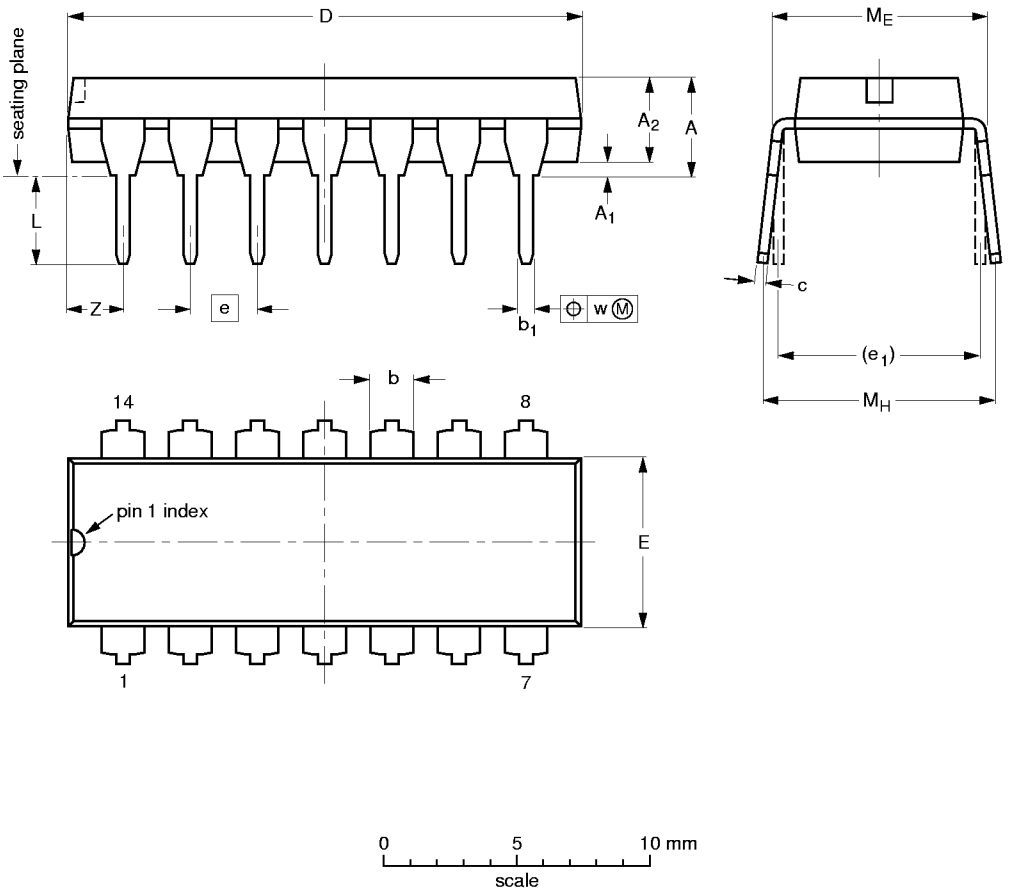


Fig.24 PCD3312C driven by microcontroller PCF84C21A. The PCF84C21A is a single-chip 8-bit microcontroller with 2 kbytes ROM and I^2C-bus. The same application is possible with the PCD3311C with MODE = V_{SS}.

13 PACKAGE OUTLINES

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

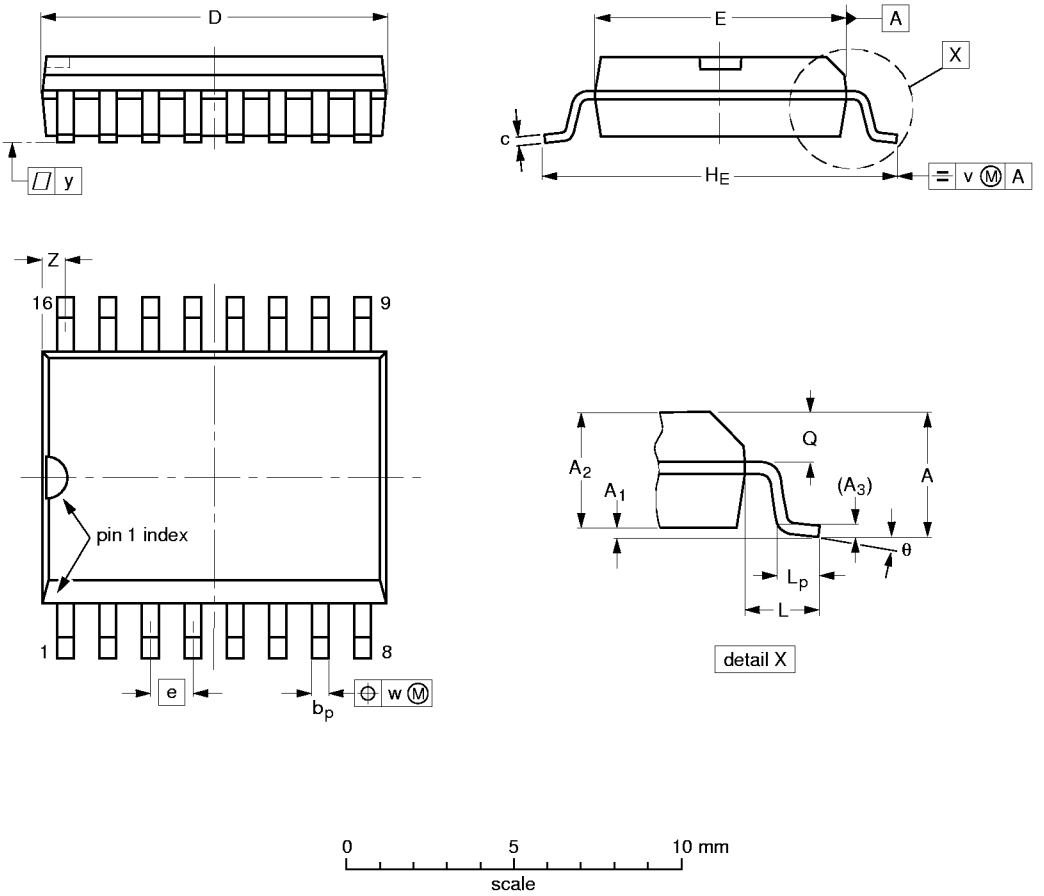
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

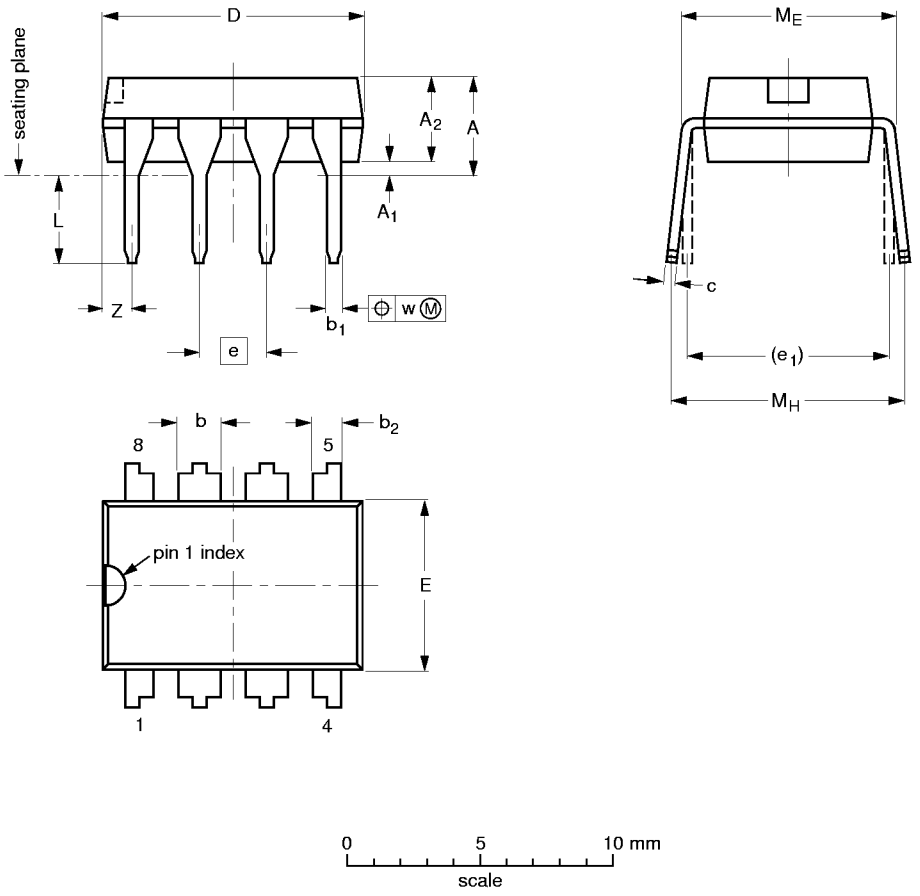
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~92-11-17~~ 95-01-24

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

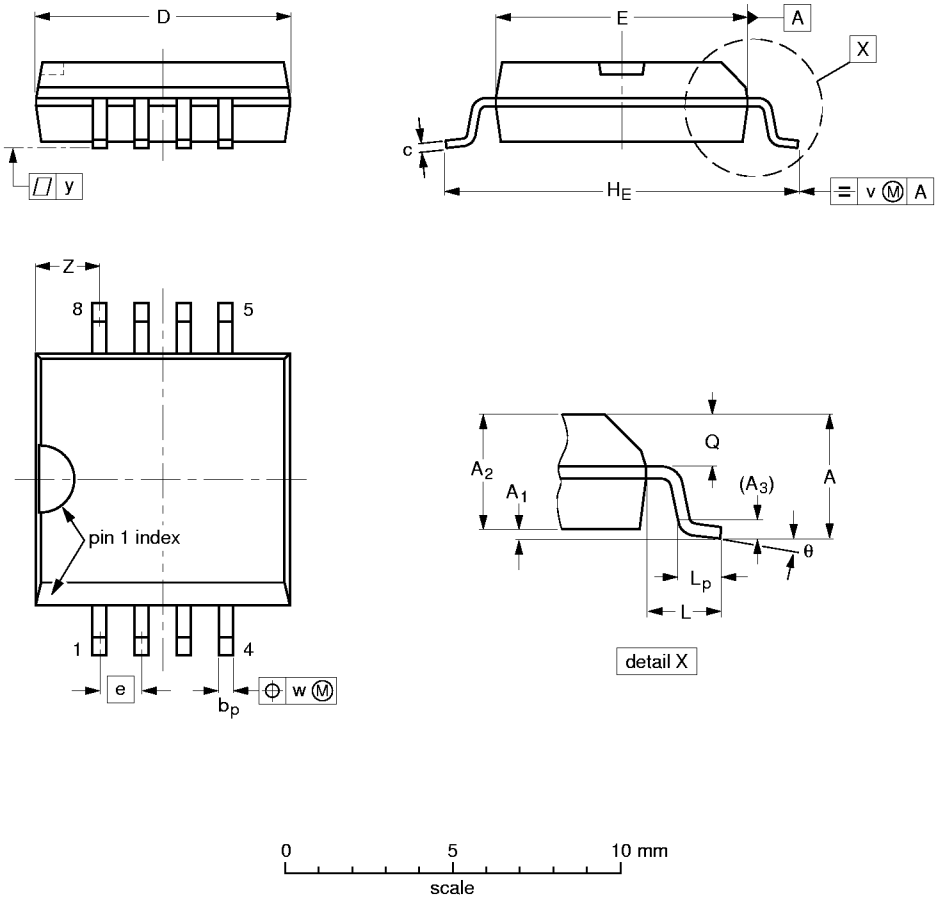
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

SO8: plastic small outline package; 8 leads; body width 7.5 mm **SOT176-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	7.65 7.45	7.6 7.4	1.27	10.65 10.00	1.45	1.1 0.45	1.1 1.0	0.25	0.25	0.1	2.0 1.8	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.30 0.29	0.30 0.29	0.050	0.42 0.39	0.057	0.043 0.018	0.043 0.039	0.01	0.01	0.004	0.079 0.071	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT176-1						~~91-08-13~~ 95-02-25

14 SOLDERING

14.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

14.2 DIP

14.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

14.3 SO

14.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

14.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.