HD61202
(Dot Matrix Liquid Crystal Graphic Display Column Driver)

Description

HD61202 is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit micro controller in the internal display RAM and generates dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to the on/off state of a dot of a liquid crystal display to provide more flexible than character display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic display with many dots.

The HD61202, which is produced in the CMOS process, can complete portable battery drive equipment in combination with a CMOS micro-controller, utilizing the liquid crystal display's low power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration in combination with the row (common) driver HD61203.

Features

- Dot matrix liquid crystal graphic display column driver incorporating display RAM
- RAM data direct display by internal display RAM
- RAM bit data 1: On
  RAM bit data 1: Off
- Internal display RAM address counter preset, increment
- Display RAM capacity: 512 bytes (4096 bits)
- 8-bit parallel interface
- Internal liquid crystal display driver circuit: 64
- Display duty cycle:
  Drives liquid crystal panels with 1/32–1/64 duty cycle multiplexing
- Wide range of instruction function:
  Display Data Read/Write, Display On/Off, Set Address, Set Display Start Line, Read Status
- Lower power dissipation: during display 2 mW max
- Power supply: V_{CC}: 5 V ± 10%
- Liquid crystal display driving voltage: 8 V to 17.0 V
- CMOS process

Ordering Information

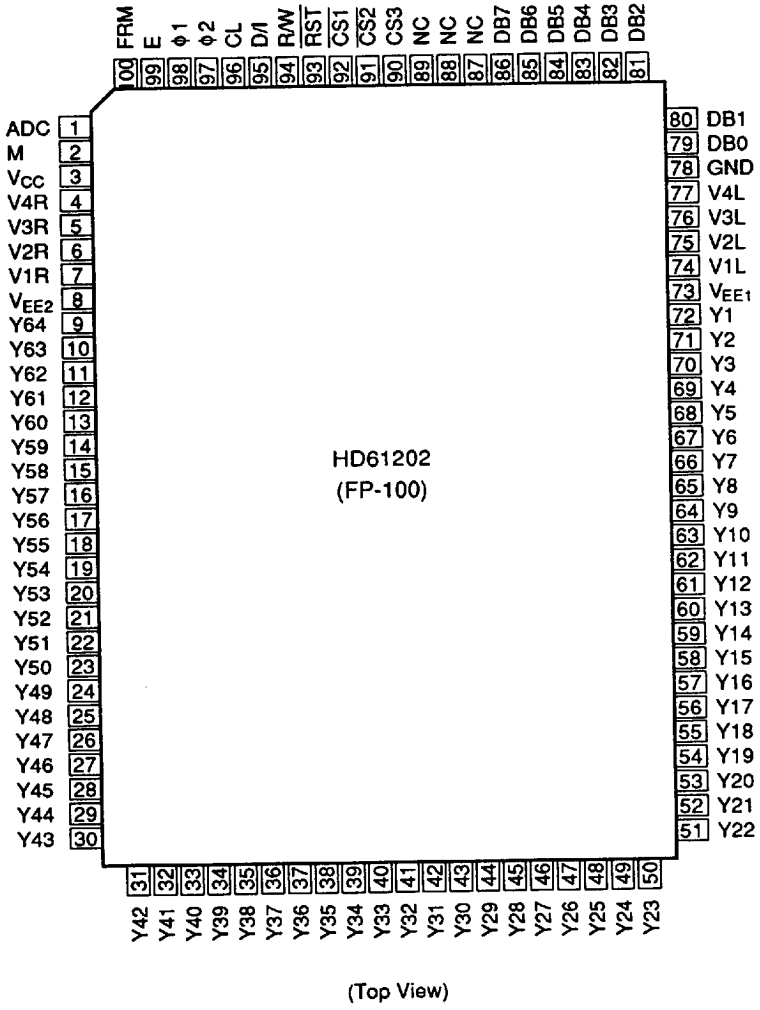
Type No.	Package
HD61202	100-pin plastic QFP(FP-100)
HD61202TFIA	100-pin thin plastic QFP(TFP-60)
HD61202D	Chip

Absolute Maximum Ratings

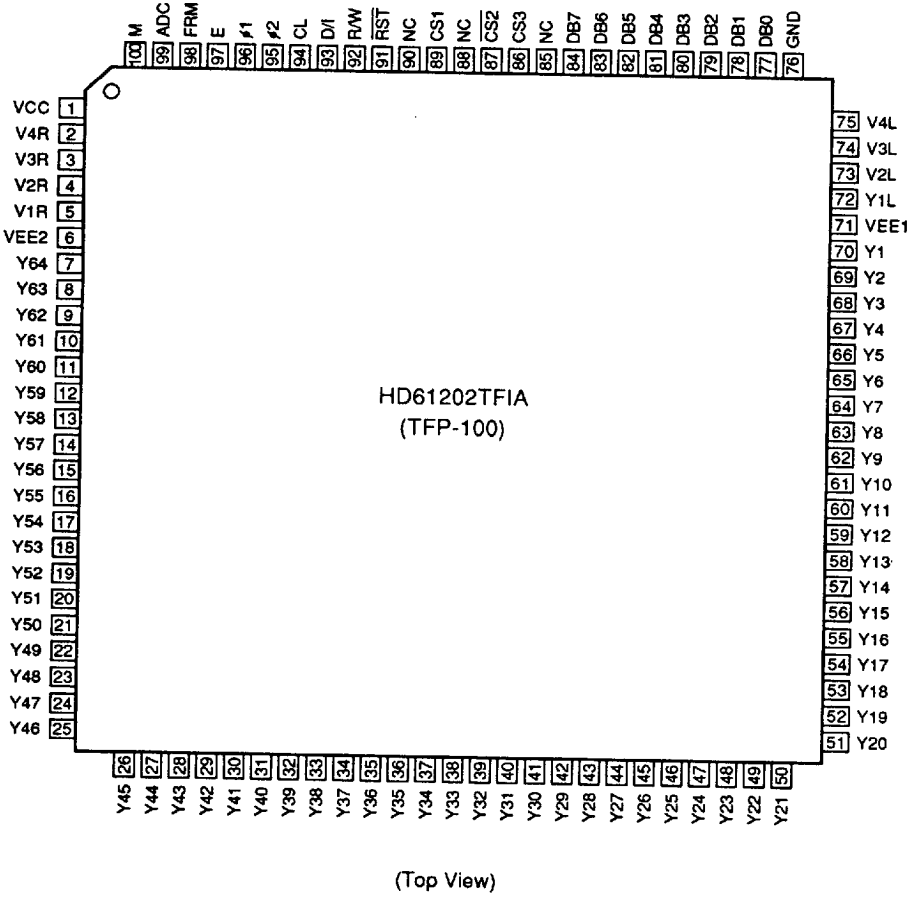
Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	−0.3 to +7.0	V	2
	V_{EE1} V_{EE2}	V_{CC} −19.0 to V_{CC} + 0.3	V	3
Terminal voltage (1)	V_{T1}	V_{EE} − 0.3 to V_{CC} + 0.3	V	4
Terminla voltage (2)	V_{T2}	−0.3 to V_{CC} + 0.3	V	2, 5
Operating temperature	Topr	−20 to +75	°C	
Storage temperature	Tstg	−55 to +125	°C	

Notes: 1. LSIs may be destroyed if they are used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the recommended operation conditions. Using them beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Apply the same supply voltage to V_{EE1} and V_{EE2}.
4. Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R, and V4R.
   Maintain
   $V_{CC} \geq V1L = V1R \geq V3L = V3R \geq V4L = V4R \geq V2L = V2R \geq V_{EE}$
5. Applies to M, FRM, CL, $\overline{RST}$, ADC, ϕ1, ϕ2, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0–DB7.

Pin Arrangement



(Top View)



(Top View)

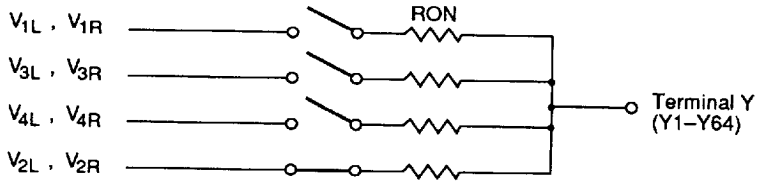
Electrical Characteristics

(GND = 0 V, V_{CC} = 4.5 to 5.5 V, V_{CC} – V_{EE} = 8 to 17.0 V, Ta = –20 to +75°C)

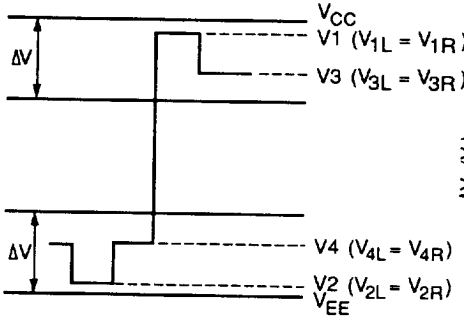
Item	Symbol	Limit Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IHC}	0.7 × V_{CC}	—	V_{CC}	V		1
	V_{IHT}	2.0	—	V_{CC}	V		2
Input low voltage	V_{ILC}	0	—	0.3 × V_{CC}	V		1
	V_{ILT}	0	—	0.8	V		2
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –205 µA	3
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA	3
Input leakage current	I_{IL}	–1.0	—	+1.0	µA	Vin = GND–V_{CC}	4
Three-state (off) input current	I_{TSL}	–5.0	—	+5.0	µA	Vin = GND–V_{CC}	5
Liquid crystal supply leakage current	I_{LSL}	–2.0	—	+2.0	µA	Vin = V_{EE} –V_{CC}	6
Driver on resistance	R_{ON}	—	—	7.5	kΩ	V_{CC} – V_{EE} = 15 V ±I_{LOAD} = 0.1 mA	8
Dissipation current	I_{CC} (1)	—	—	100	µA	During display	7
	I_{CC} (2)	—	—	500	µA	During access access cycle = 1 MHz	7

Notes:
1. Applies to M, FRM, CL, $\overline{RST}$, ϕ1, and ϕ2.
2. Applies to $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0–DB7.
3. Applies to DB0–DB7.
4. Applies to terminals except for DB0–DB7.
5. Applies to DB0–DB7 at high impedance.
6. Applies to V1L–V4L and V1R–V4R.
7. Specified when liquid crystal display is in 1/64 duty cycle mode.
   Operation frequency f_{CLK} = 250 kHz (ϕ1 and ϕ2 frequency)
   Frame frequency f_M = 70 Hz (FRM frequency)
   Specified in the state of
   Output terminal: not loaded
   Input level: $V_{IH} = V_{CC}$ (V)
   V_{IL} = GND (V)
   Measured at V_{CC} terminal
8. Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L, and V4R) when load current flows through one of the terminals Y1 to Y64. This value is specified under the following condition:

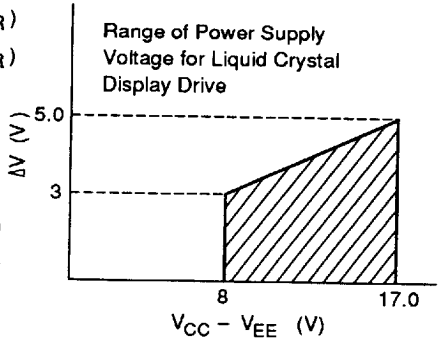
$$V_{CC} - V_{EE} = 15.5\ V$$
$$V_{1L} = V_{1R},\ V_{3L} = V_{3R} = V_{CC} - 2/7\ (V_{CC} - V_{EE})$$
$$V_{2L} = V_{2R},\ V_{4L} = V_{4R} = V_{CC} + 2/7\ (V_{CC} - V_{EE})$$



The following is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L = V1R and V3L = V3R and negative voltage to V2L = V2R and V4L = V4R within the ΔV range. This range allows stable impedance on driver output (RON). Notice that ΔV depends on power supply voltage $V_{CC} - V_{EE}$.



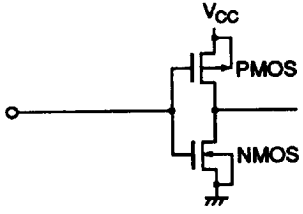
Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage $V_{CC} - V_{EE}$ and ΔV

Terminal Configuration

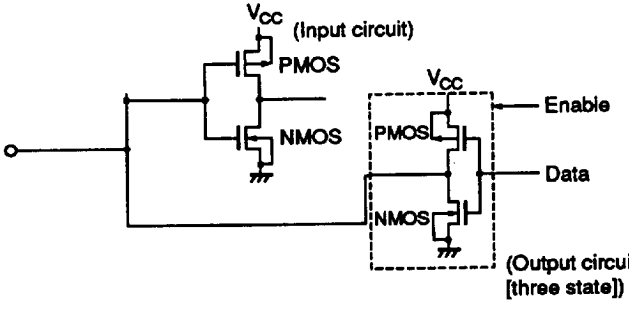
Input Terminal



Applicable terminals :
M, FRM, CL, $\overline{RST}$, ϕ1, ϕ2, $\overline{CS1}$, $\overline{CS2}$, CS3,
E, R/W, D/I, ADC

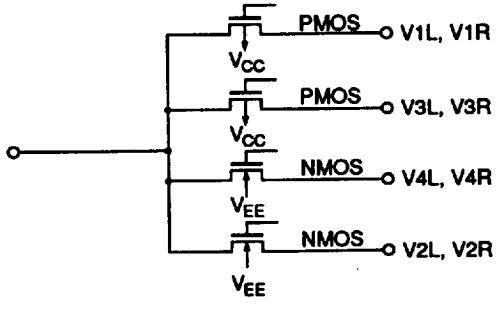
Input/Output Terminal

Applicable terminals: DB0–DB7



Output Terminal

Applicable Terminals:
Y1–Y64



Interface AC Characteristics

MPU Interface
(GND = 0 V, V_{CC} = 4.5 to 5.5 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Note
E cycle time	t_{CYC}	1000	—	—	ns	1, 2
E high level width	P_{WEH}	450	—	—	ns	1, 2
E low level width	P_{WEL}	450	—	—	ns	1, 2
E rise time	tr	—	—	25	ns	1, 2
E fall time	tf	—	—	25	ns	1, 2
Address setup time	t_{AS}	140	—	—	ns	1, 2
Address hold time	t_{AH}	10	—	—	ns	1, 2
Data setup time	t_{DSW}	200	—	—	ns	1
Data delay time	t_{DDR}	—	—	320	ns	2, 3
Data hold time (Write)	t_{DHW}	10	—	—	ns	1
Data hold time (Read)	t_{DHR}	20	—	—	ns	2

Notes: 1.

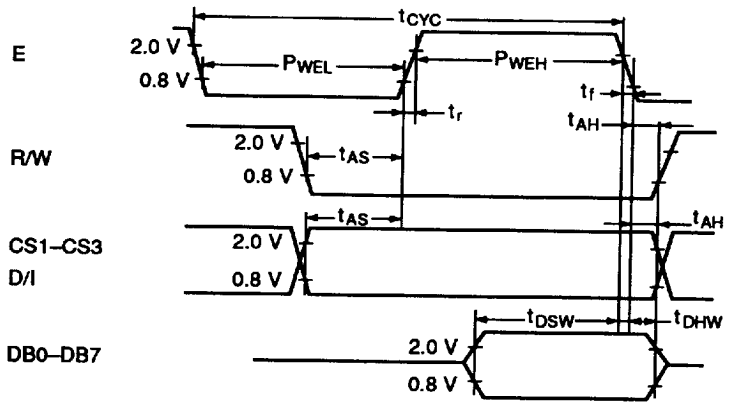


Figure 1 CPU Write Timing

Notes: 2.

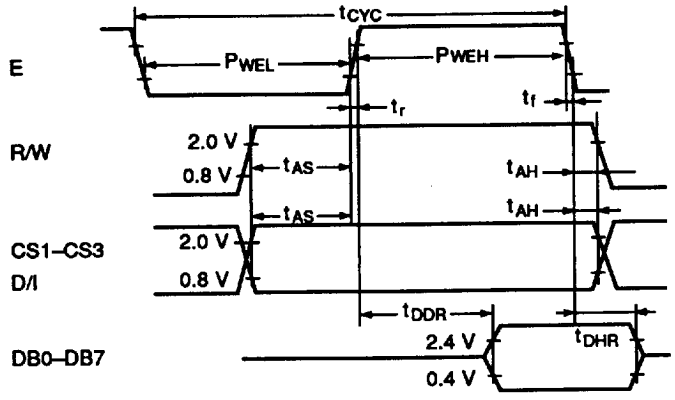
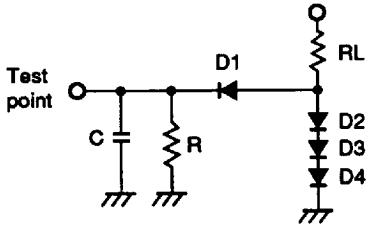


Figure 2 CPU Read Timing

3. DB0–DB7: load circuit



RL = 2.4 k Ω
R = 11 k Ω
C = 130 pF (including jig capacitance)
Diodes D1–D4 are all 1S2074 Ⓗ.

Clock Timing
(GND = 0 V, V_{CC} = 4.5 to 5.5 V, Ta = –20 to +75°C)

Item	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
ϕ1, ϕ2 cycle time	tcyc	2.5	—	20	µs	Fig. 3
ϕ1 low level width	$t_{WL\phi1}$	625	—	—	ns	Fig. 3
ϕ2 low level width	$t_{WL\phi2}$	625	—	—	ns	Fig. 3
ϕ1 high level width	$t_{WH\phi1}$	1875	—	—	ns	Fig. 3
ϕ2 high level width	$t_{WH\phi2}$	1875	—	—	ns	Fig. 3
ϕ1—ϕ2 phase difference	t_{D12}	625	—	—	ns	Fig. 3
ϕ2—ϕ1 phase difference	t_{D21}	625	—	—	ns	Fig. 3
ϕ1, ϕ2 rise time	tr	—	—	150	ns	Fig. 3
ϕ1, ϕ2 fall time	tf	—	—	150	ns	Fig. 3

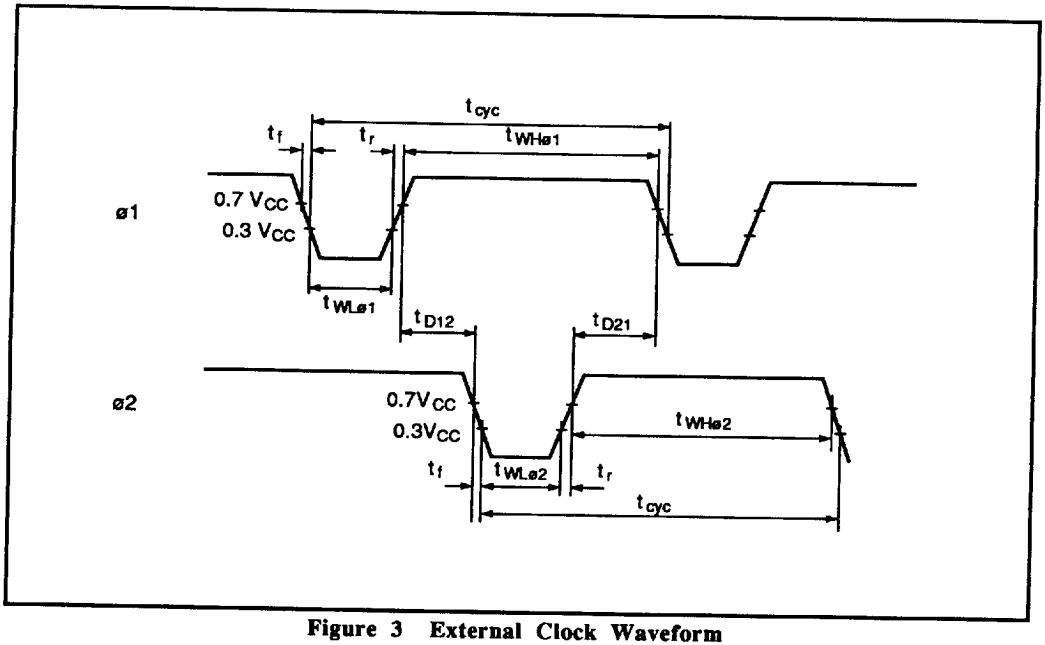


Figure 3 External Clock Waveform

Display Control Timing
(GND = 0V, V_{CC} = 4.5 to 5.5 V, Ta = –20 to +75 °C)

Item	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
FRM delay time	t_{DFRM}	–2	—	+2	µs	Fig. 4
M delay time	t_{DM}	–2	—	+2	µs	Fig. 4
CL low level width	t_{WLCL}	35	—	—	µs	Fig. 4
CL high level width	t_{WHCL}	35	—	—	µs	Fig. 4

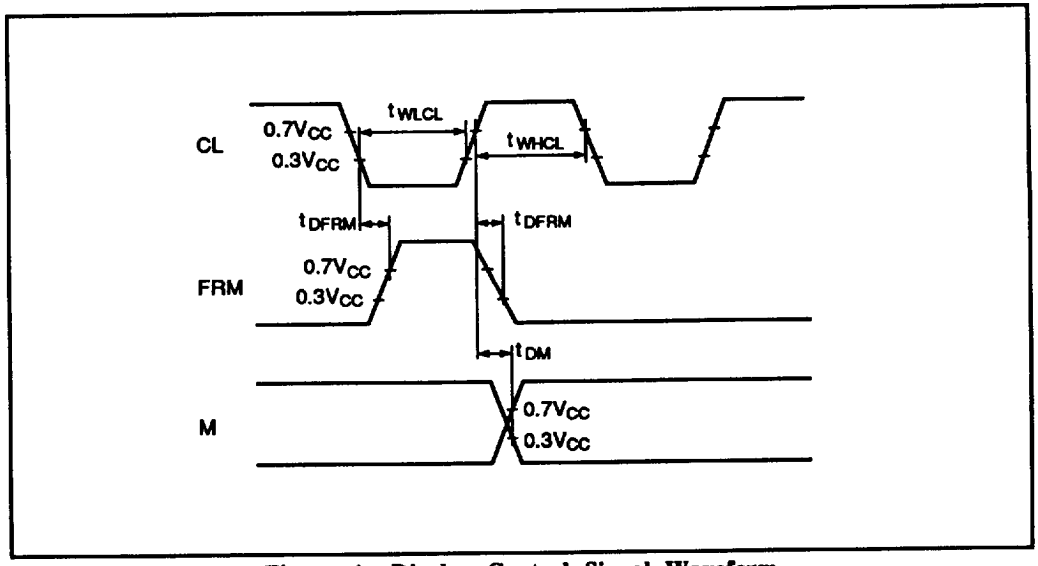
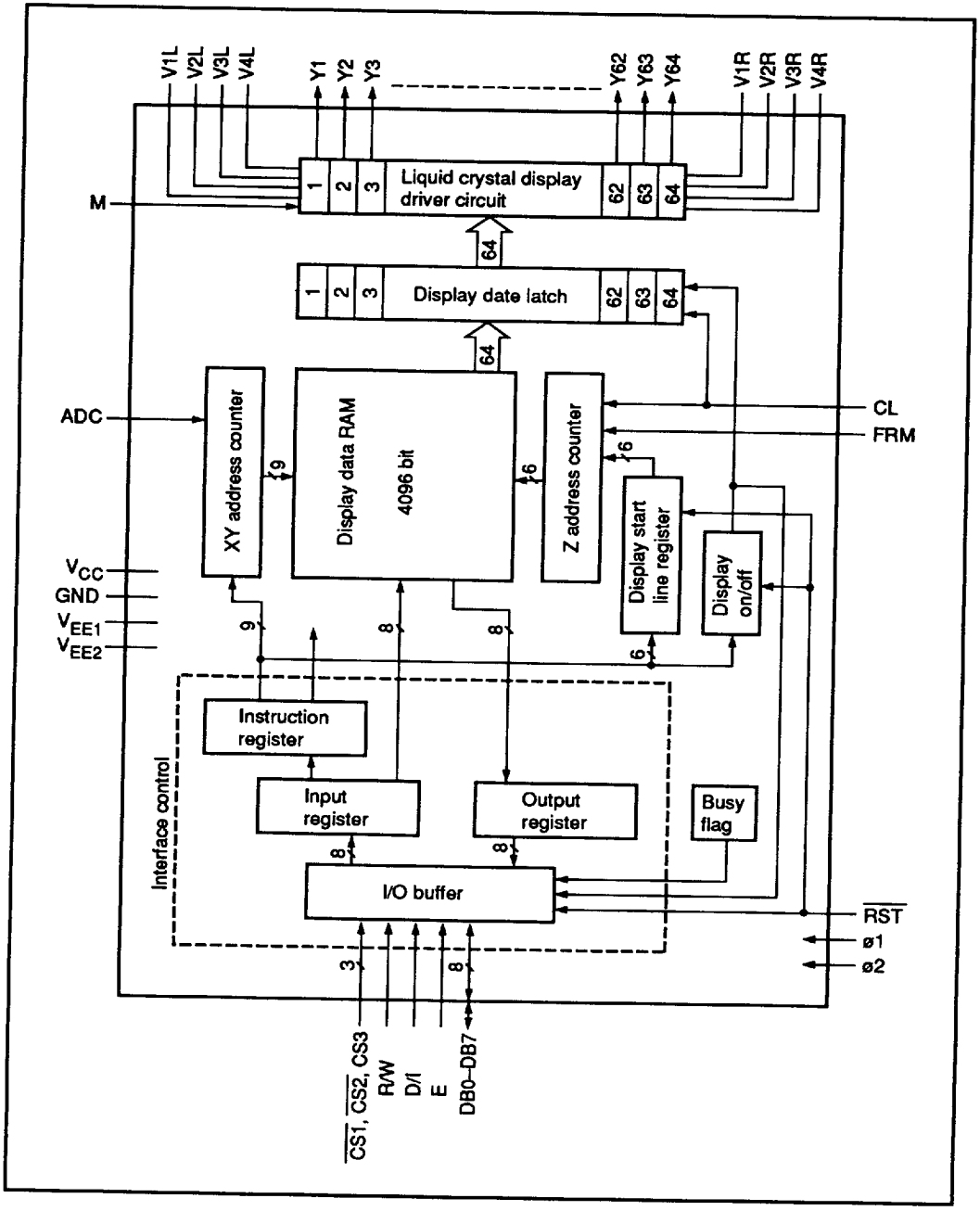


Figure 4 Display Control Signal Waveform

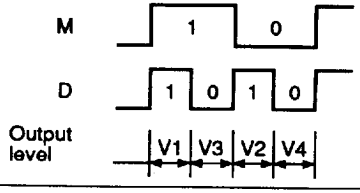
Block Diagram



Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND	2		Power supply	Power supply for internal logic. Recommended voltage is: GND = 0 V V_{CC} = 5 V ±10%
V_{EE1} V_{EE2}	2		Power supply	Power supply for liquid crystal display drive circuit. Recommended power supply voltage is $V_{CC} - V_{EE}$ = 8 to 17.0 V. Connect the same power supply to V_{EE1} and V_{EE2}. V_{EE1} and V_{EE2} are not connected each other in the LSI.
V1L, V1R V2L, V2R V3L, V3R V4L, V4R	8		Power supply	Power supply for liquid crystal display drive. Apply the voltage specified depending on liquid crystals within the limit of V_{EE} through V_{CC}. V1L (V1R), V2L (V2R): Selection level V3L (V3R), V4L (V4R): Non-selection level Power supplies connected with V1L and V1R (V2L & V2R, V3L & V3R, V4L & V4R) should have the same voltages.
$\overline{CS1}$ $\overline{CS2}$ CS3	3	I	MPU	Chip selection. Data can be input or output when the terminals are in the following conditions: Terminal Name: $\overline{CS1}$ $\overline{CS2}$ CS3 Condition: L L H
E	1	I	MPU	Enable. At write(R/W = Low): Data of DB0 to DB7 is latched at the fall of E. At read(R/W = High): Data appears at DB0 to DB7 while E is at high level.
R/W	1	I	MPU	Read/write. R/W = High: Data appears at DB0 to DB7 and can be read by the CPU. When E = high, CS1, CS2 = low and CS3 = high. R/W = Low: DB0 to DB7 can accept at fall of E when CS1, CS2 = low and CS3 = high.
D/I	1	I	MPU	Data/instruction. D/I = High: Indicates that the data of DB0 to DB7 is display data. D/I = Low: Indicates that the data of DB0 to DB7 is display control data.

Terminal Functions (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Functions
ADC	1	I	V_{CC}/GND	Address control signal to determine the relation between Y address of display RAM and terminals from which the data is output. ADC = High: Y1: $0, Y64: $63 ADC = Low: Y64: $0, Y1: $63
DB1-DB7	8	I/O	MPU	Data bus, three-state I/O common terminal.
M	1	I	HD61203	Switch signal to convert liquid crystal drive waveform into AC.
FRM	1	I	HD61203	Display synchronous signal (frame signal). Presets the 6-bit display line counter and synchronizes the common signal with the frame timing when the FRM signal becomes high.
CL	1	I	HD61203	Synchronous signal to latch display data. The rising CL signal increments the display output address counter and latches the display data.
ϕ1, ϕ2	2	I	HD61203	2-phase clock signal for internal operation. The ϕ1 and ϕ2 clocks are used to preform operations (I/O of display data and execution of instructions) other than display.
Y1-Y64	64	O	Liquid crystal display	Liquid crystal display column (segment) drive output. These pins outputs light on level when 1 is in the display RAM, and light off level when 0 is it. Relation among output level, M, and display data (D) is as follows: 
$\overline{RST}$	1	I	CPU or external CR	The following registers can be initialized by setting the $\overline{RST}$ signal to low level. 1. On/off register 0 set (display off) 2. Display start line register line 0 set (displays from line 0) After releasing reset, this condition can be changed only by instruction.
NC	3		Open	Unused terminals. Don't connect any lines to these terminals.

Note: 1 corresponds to high level in positive logic.

Function of Each Block

Interface Control

1. I/O buffer

Data is transferred through 8 data bus lines (DB0–DB7).

DB7: MSB (Most significant bit)

DB0: LSB (Least significant bit)

Data can neither be input nor output unless $\overline{CS1}$ to CS3 are in the active mode. Therefore, when $\overline{CS1}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{RST}$ and ADC; that is namely, the internal state is maintained and no instruction excutes. Besides, pay attention to $\overline{RST}$ and ADC which operate irrespectively of $\overline{CS1}$ to CS3.

2. Register

Both input register and output register are provided to interface to an MPU whose speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals (table 1).

a. Input register

The input register is used to store data temporarily before writing it into display data RAM.

The data from MPU is written into the input register, then into display data RAM automatically by internal operation. When $\overline{CS1}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in table 1, data is latched at the fall of the E signal.

b. Output register

The output register is used to store data temporarily that is read from display data RAM. To read out the data from output register, $\overline{CS1}$ to CS3 should be in the active mode and both D/I and R/W should be 1. With the read display data instruction, data stored in the output register is output while E is high level. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1.

The contents in the output register are rewritten by the read display data instruction, but are held by address set instruction, etc.

Therefore, the data of the specified address cannot be output with the read display data instruction right after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Figure 5 shows the CPU read timing.

Table 1 Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register)
1	0	Writes data into input register as internal operation (input register → display data RAM)
0	1	Busy check. Read of status data.
0	0	Instruction

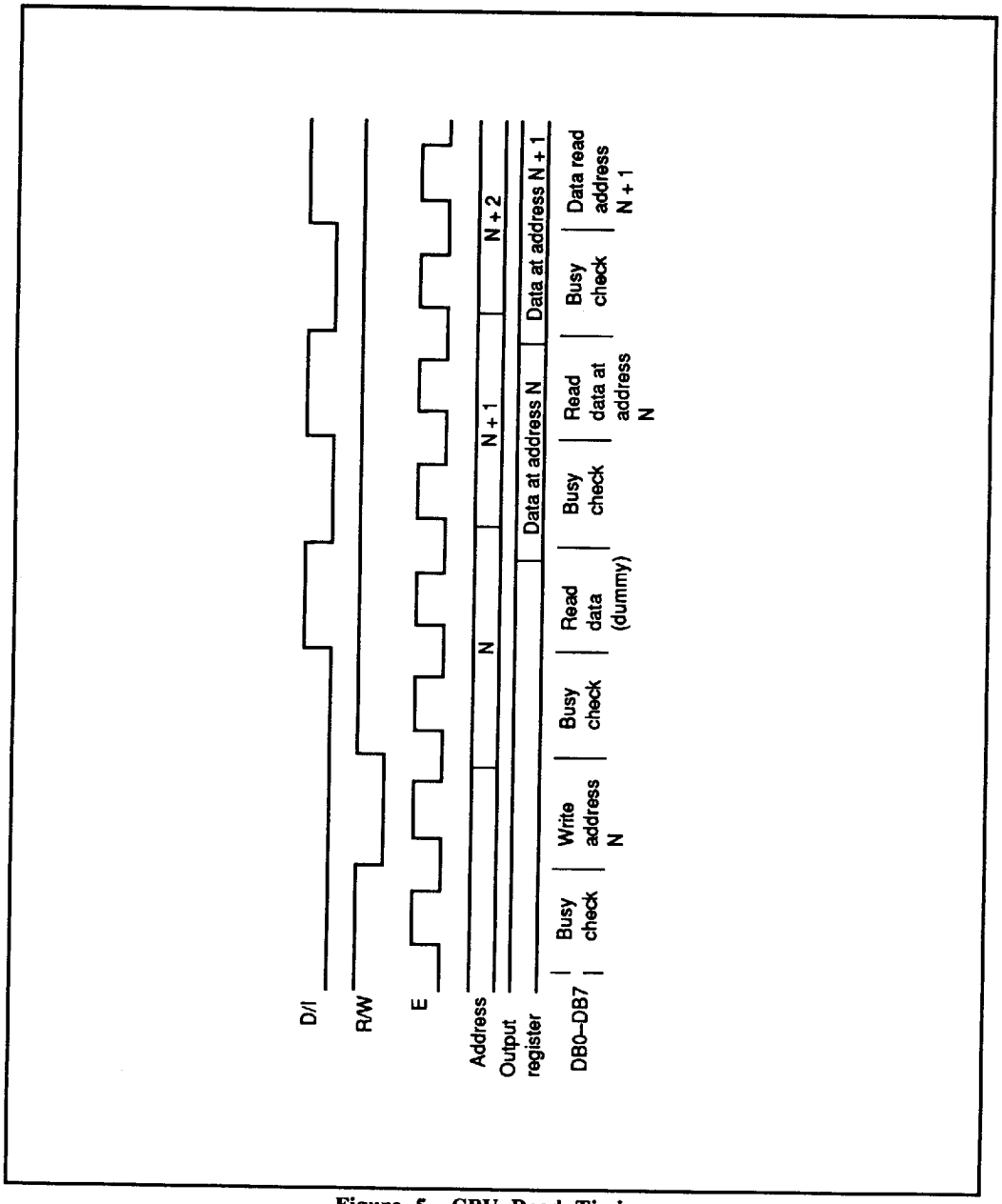


Figure 5 CPU Read Timing

Busy Flag

Busy flag = 1 indicates that HD61202 is operating and no instructions except status read instruction can be accepted. The value of the busy flag is read out on DB7 by the status read instruction. Make sure that the busy flag is reset (0) before issuing instructions.

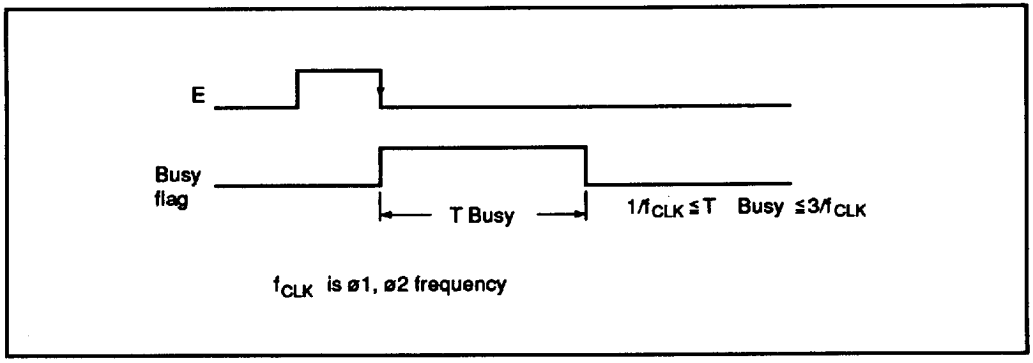


Figure 6 Busy Flag

Display On/Off Flip/Flop

The display on/off flip/flop selects one of two states, on state and off state of segments Y1 to Y64. In on state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in off state independent of the data in RAM. It is controlled by display on/off instruction. $\overline{RST}$ signal = 0 sets the segments in off state. The status of the flip/flop is output to DB5 by status read instruction. Display on/off instruction does not influence data in RAM. To control display data latch by this flip/flop, CL signal (display synchronous signal) should be input correctly.

Display Start Line Register

The display start line register specifies the line in RAM which corresponds to the top line of LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling of the screen.

6-bit display start line information is written into this register by the display start line set instruction. When high level of the FRM signal starts the display, the information in this register is transferred to the Z address counter, which controls the display address, presetting the Z address counter.

X, Y Address Counter

A 9-bit counter which designates addresses of the internal display data RAM. X address counter (upper 3 bits) and Y address counter (lower 6 bits) should be set to each address by the respective instructions.

1. X address counter
Ordinary register with no count functions. An address is set by instruction.

2. Y address counter
An address is set by instruction and is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Stores dot data for display. 1-bit data of this RAM corresponds to light on (data = 1) and light off (data = 0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment pins can be reversed by ADC signal.

As the ADC signal controls the Y address counter, reversing of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, never fail to connect ADC pin to V_{CC} or GND when using.

Figure 7 shows the relations between Y address of RAM and segment pins in the cases of ADC = 1 and ADC = 0 (display start line = 0, 1/64 duty cycle).

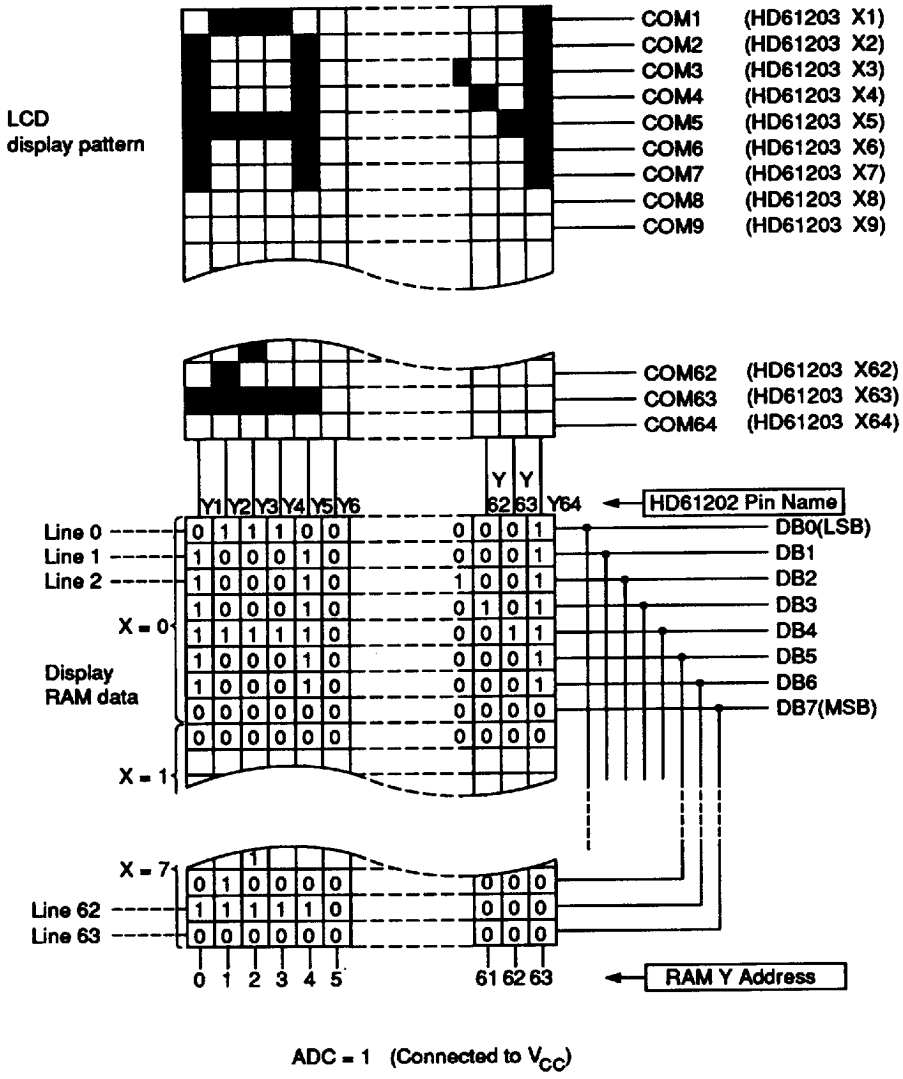


Figure 7 Relation between RAM Data and Display

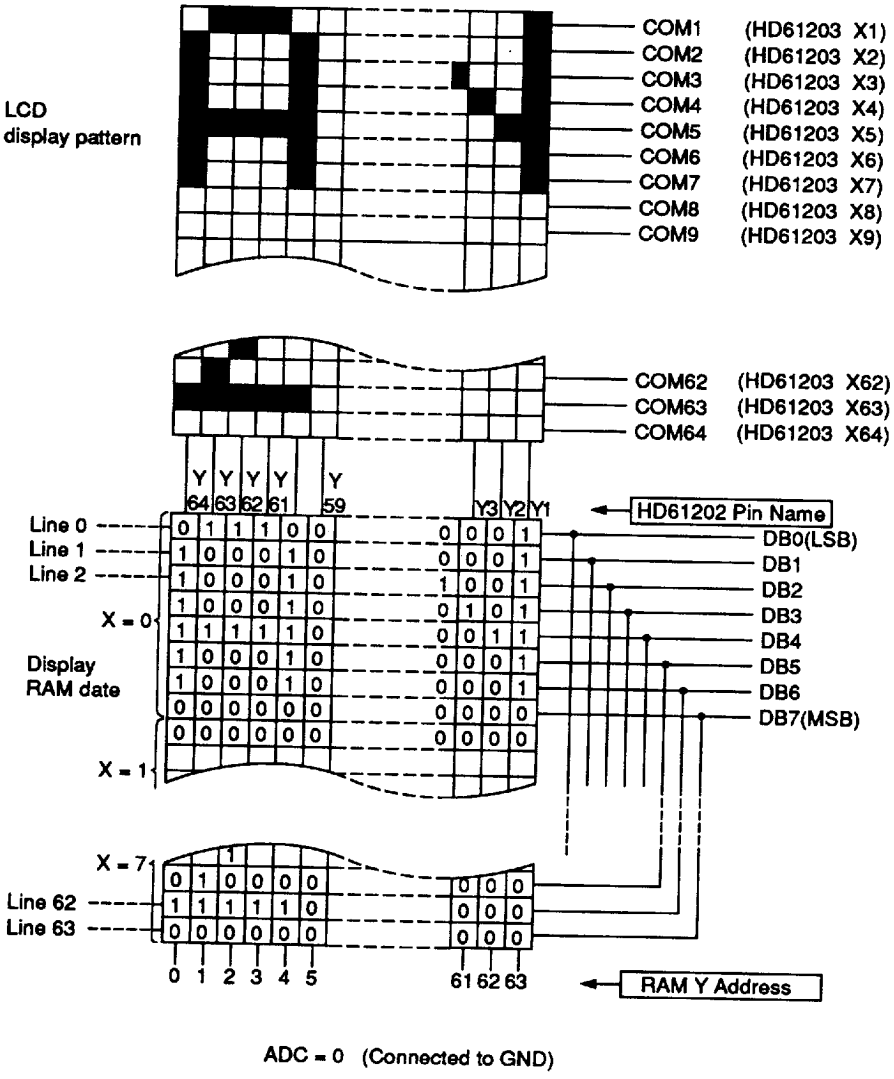


Figure 7 Relation between RAM Data and Display (cont)

Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6 bits and counts up at the fall of the CL signal. At the high level of FRM, the contents of the display start line register is preset at the Z counter.

Display Data Latch

The display data latch stores the display data temporarily that is output from display data RAM to the liquid crystal driving circuit. Data is latched at the rise of the CL signal. The display on/off instruction controls the data in this latch and does not influence data in display data RAM.

Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

Reset

The system can be initialized by setting $\overline{RST}$ terminal at low level when turning power on.

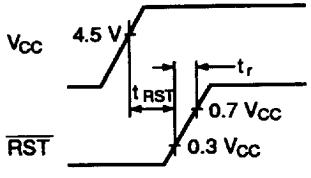
1. Display off
2. Set display start line register line 0.

While $\overline{RST}$ is low level, no instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4 = 0 (clear RESET) and DB7 = 0 (Ready) by status read instruction. The conditions of power supply at initial power up are shown in table 1.

Table 1 Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	—	—	µs
Rise time	t_r	—	—	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the registers except on/off register and in RAM.



Display Control Instructions

Outline

Table 2 shows the instructions. Read/write (R/W) signal, data/instruction (D/I) signal, and data bus signals (DB0 to DB7) are also called instructions because the internal operation depends on the signals from the MPU.
These explanations are detailed in the following pages. Generally, there are following three kinds of instructions:

1. Instruction to set addresses in the internal RAM
2. Instruction to transfer data from/to the internal RAM
3. Other instructions

In general use, the second type of instruction is used most frequently. Since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be shortened. During the execution of an instruction, the system cannot accept instructions other than status read instruction. Send instructions from MPU after making sure that the busy flag is 0, which is proof that an instruction is not being excuted.

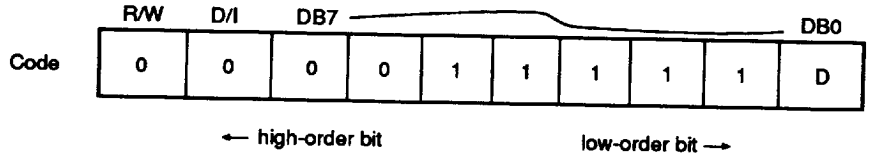
Table 2 Instructions

Instructions	Code R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Functions
Display on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected. 1: on, 0: off.
Display start line	0	0	1	1	Display start line (0–63)						Specifies the RAM line displayed at the top of the screen.
Set page (X address)	0	0	1	0	1	1	1	Page (0–7)			Sets the page (X address) of RAM at the page (X address) register.
Set address	0	0	0	1	Y address (0–63)						Sets the Y address in the Y address counter.
Status read	1	0	Busy	0	ON/ OFF	Reset	0	0	0	0	Reads the status. RESET 1: Reset 0: Normal ON/OFF 1: Display off 0: Display on Busy 1: Internal operation 0: Ready
Write display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM. Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
Read display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.

Note: 1. Busy time varies with the frequency (f_{CLK}) of ϕ1, and ϕ2.
($1/f_{CLK} \leq T_{BUSY} \leq 3/f_{CLK}$)

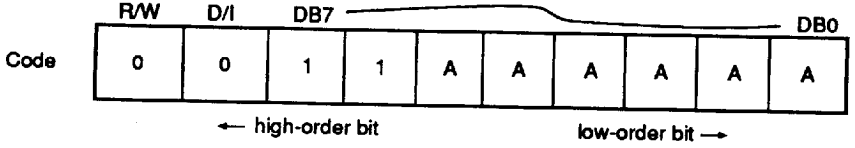
Detailed Explanation

Display on/off



The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

Display start line



Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen. Figure 8 shows examples of display (1/64 duty cycle) when the start line = 0–3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

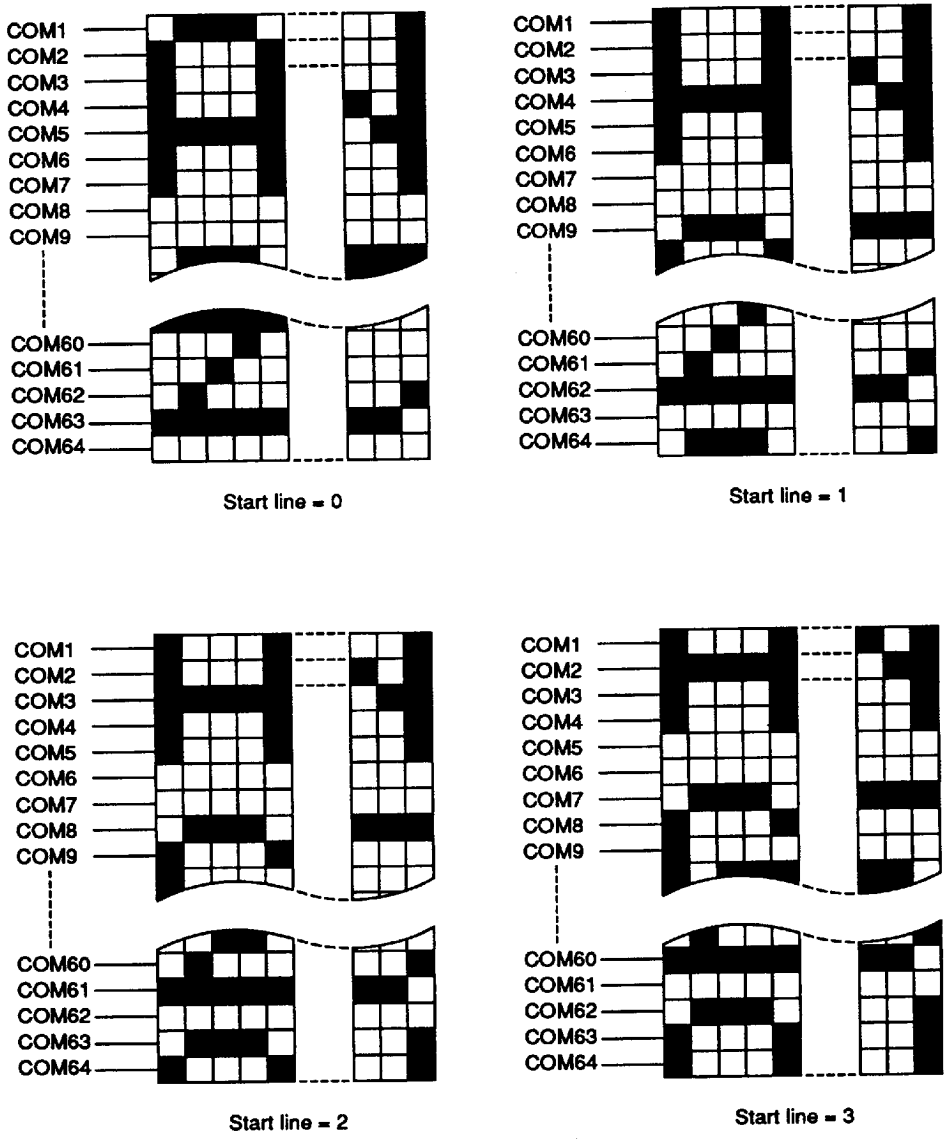


Figure 8 Relation Between Start Line and Display

Set page (X address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A

← high-order bit low-order bit →

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set. See figure 9.

Set Y address

	R/W	D/I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

← high-order bit low-order bit →

Y address AAAAAA (binary) of the display data RAM is set in the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

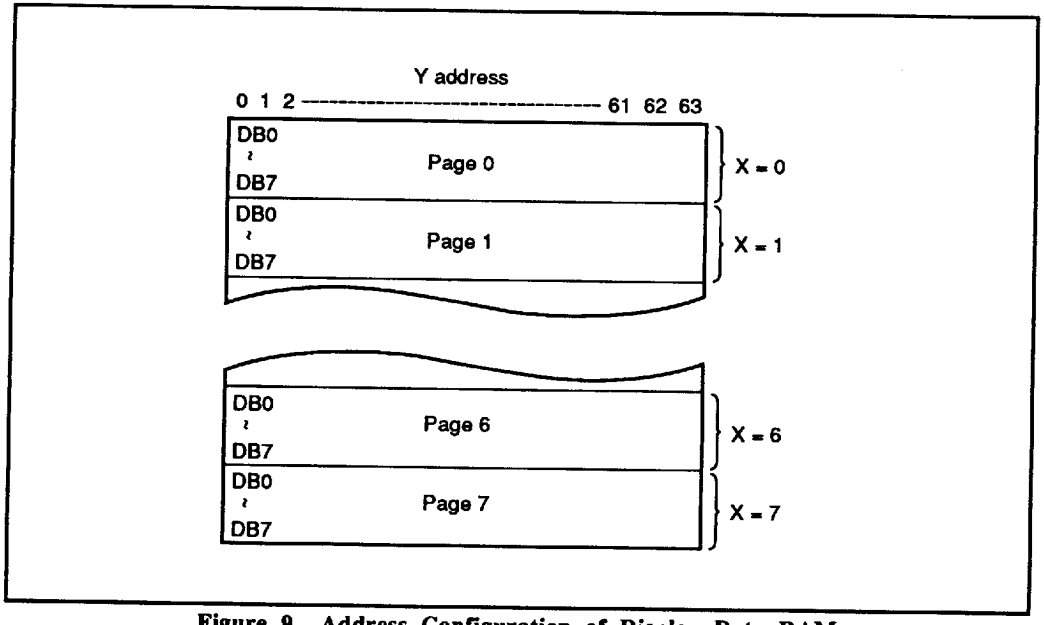
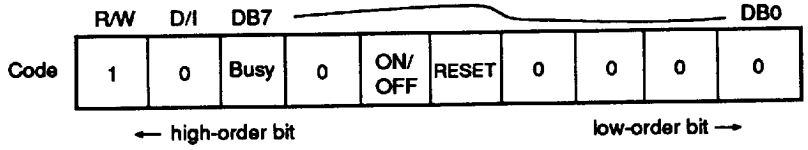


Figure 9 Address Configuration of Display Data RAM

Status Read

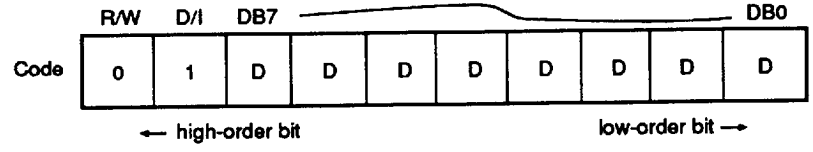


Busy: When Busy is 1, the LSI is executing internal operations. No instructions are accepted while Busy is 1, so you should make sure that Busy is 0 before writing the next instruction.

ON/OFF: Shows the liquid crystal display conditions: on condition or off condition.
When ON/OFF is 1, the display is in off condition.
When ON/OFF is 0, the display is in on condition.

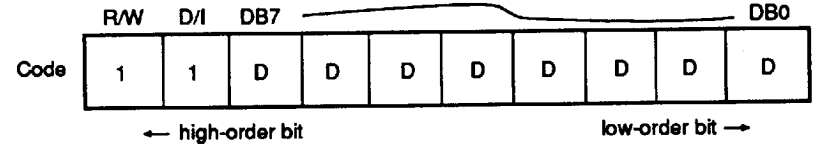
RESET: RESET = 1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.
RESET = 0 shows that initializing has finished and the system is in the usual operation condition.

Write Display Data



Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

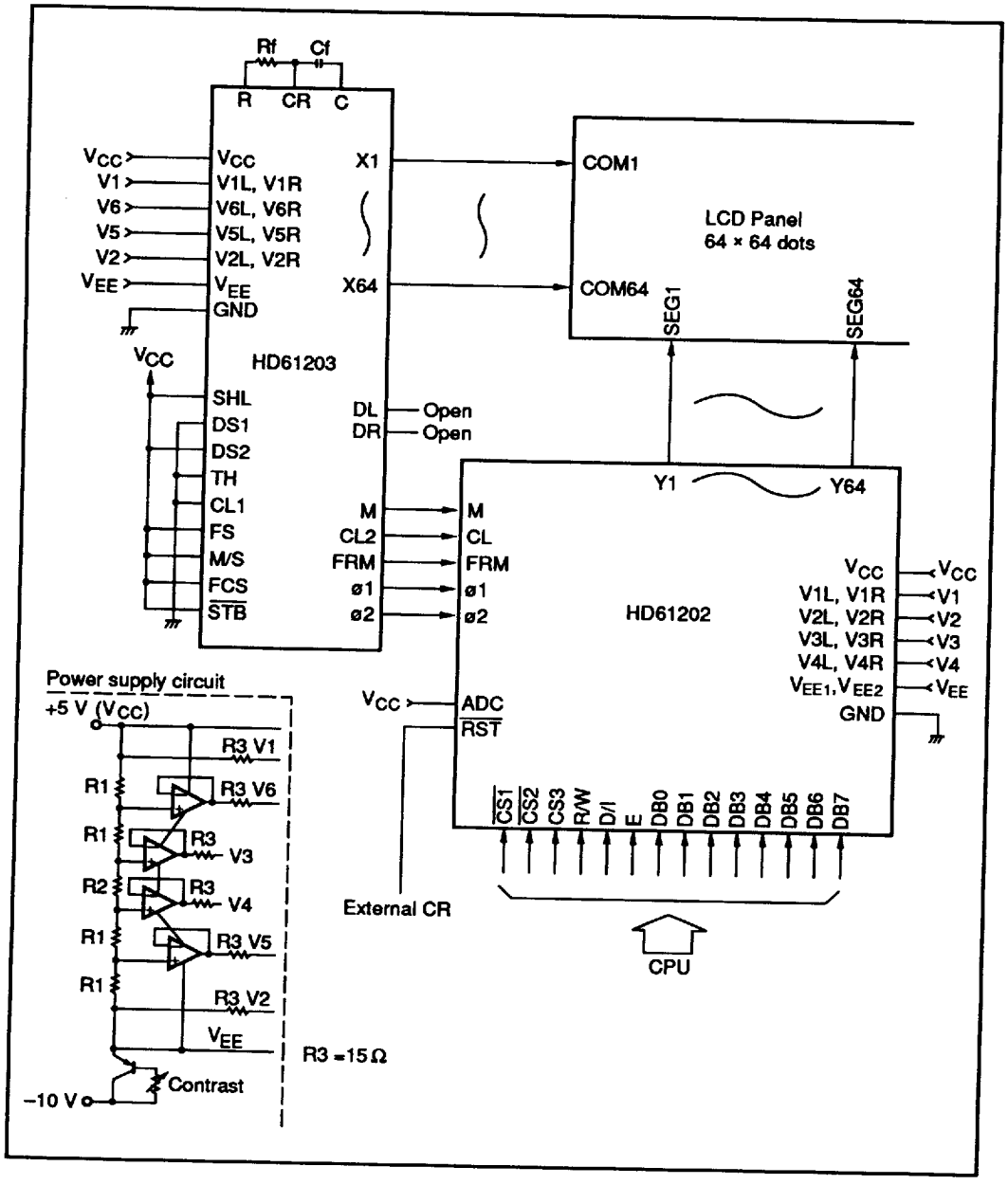
Read Display Data

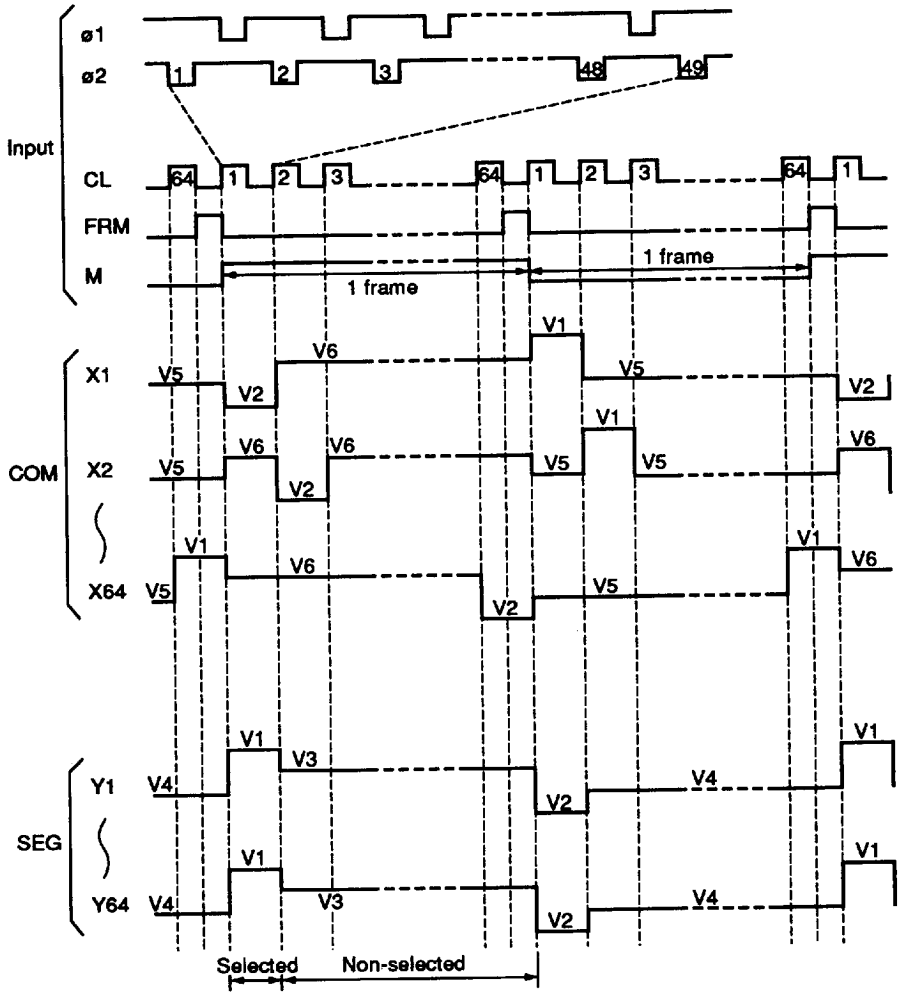


Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.
One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in "FUNCTION OF EACH BLOCK".

Use of HD61202

Interface with HD61203 (1/64 duty cycle)





The waveforms of Y1 to Y64 outputs vary with the display date. In this example, the top line of the panel lights up and other dots do not.

Figure 10 LCD Driver Timing Chart (1/64 duty cycle)

Interface with CPU

1. Example of connection with HD6800

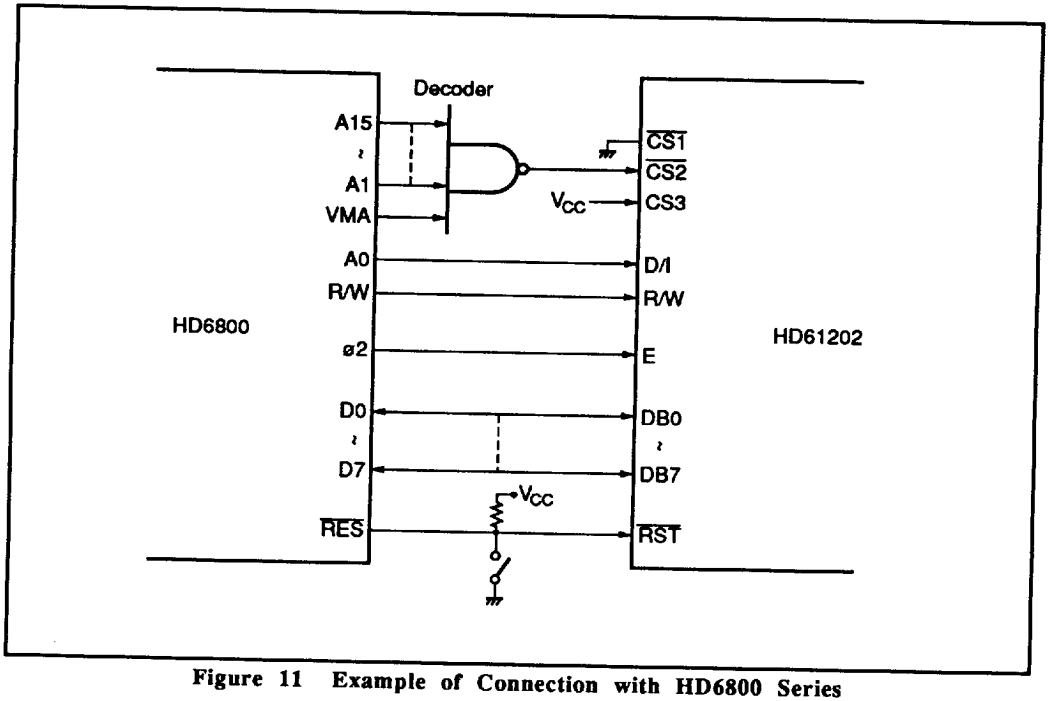


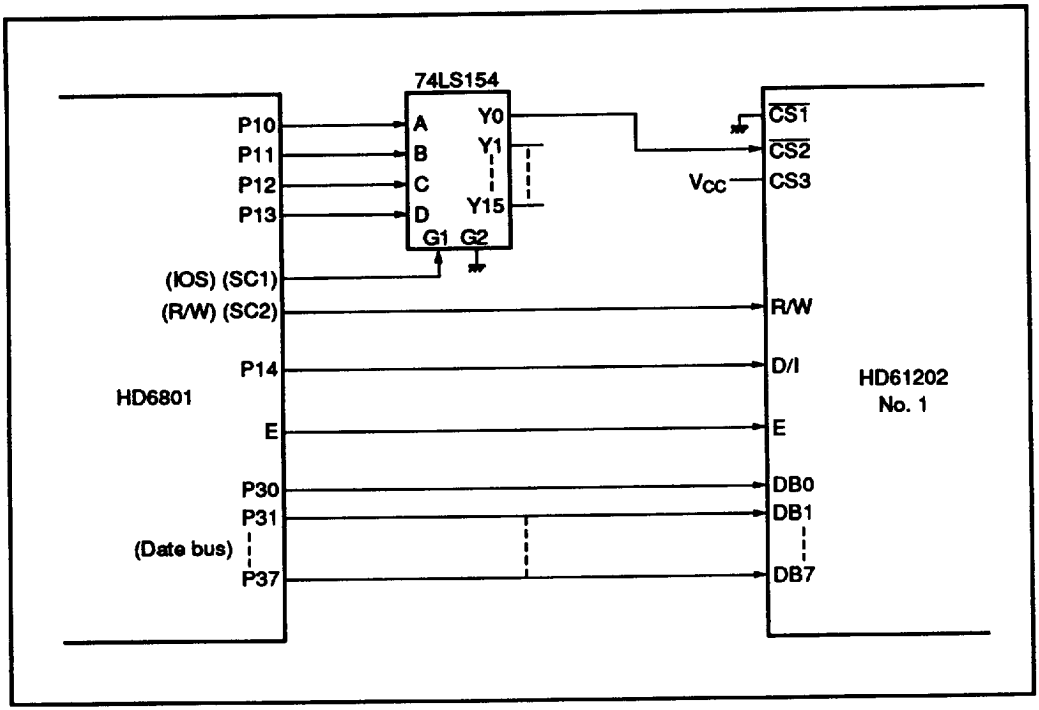
Figure 11 Example of Connection with HD6800 Series

In this decoder, addresses of HD61202 in the address area of HD6800 are:

Read/write of the display data	$FFFF
write of display instruction	$FFFE
Read out of status	$FFFE

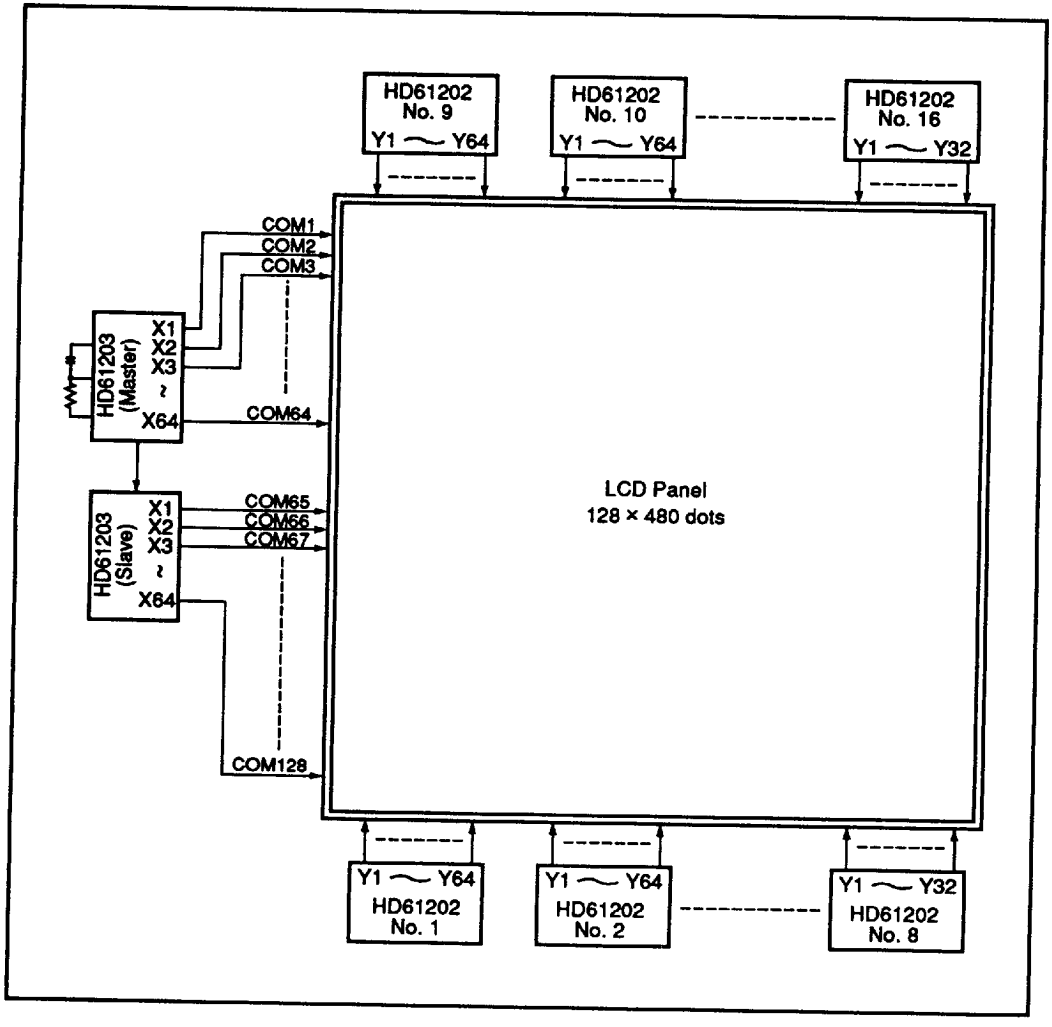
Therefore, you can control HD61202 by reading/writing the data at these addresses.

2. Example of connection with HD6801



- Set HD6801 to mode 5. P10 to P14 are used as the output port and P30 to P37 as the data bus.
- 74LS154 4-to-16 decoder generates chip select signal to make specified HD61202 active after decoding 4 bits of P10 to P13.
- Therefore, after enabling the operation by P10 to P13 and specifying D/I signal by P14, read/write from/to the external memory area ($0100 to $01FE) to control HD61202. In this case, IOS signal is output from SC1 and R/W signal from SC2.
- For details of HD6800 and HD6801, refer to their manuals.

Example of Application



Note: In this example, two HD61203s output the equivalent waveforms. So, stand-alone operation is possible. In this case, connect COM1 and COM65 to X1, COM2 and COM66 to X2, ..., and COM64 and COM128 to X64. However, for the large screen display, it is better to drive in 2 rows as in this example to guarantee the display quality.