CIRRUS LOGIC®

CL-PS7111

Preliminary Data Book

FEATURES

- **Ultra low power**
  - — Designed for applications that require long battery life while using standard AA/AAA batteries
  - — Average 45 mW/66 mW in normal operation (2.7 V/3.3 V, 13 MHz/18.432 MHz)
  - — Average 15 mW in idle mode (clock to the CPU stopped, everything else running)
  - — Average 15 µA in standby mode (realtime clock on, everything else stopped)
- **Performance matching 33-MHz Intel® '486-based PC**
  - — 15 Vax™-MIPS (Dhrystone®) at 18 MHz
- **ARM710a microprocessor**
  - — ARM7 CPU
  - — 8 Kbytes of four-way set-associative cache
  - — MMU with 64-entry TLB (transition look-aside buffer)
- **DRAM controller**
  - — Supports both 16- and 32-bit-wide DRAMs
- **ROM/SRAM/flash memory control**
  - — Decodes 4, 5, or 6 separate memory segments of 256 Mbytes

(cont.)

Low-Power System-on-a-Chip

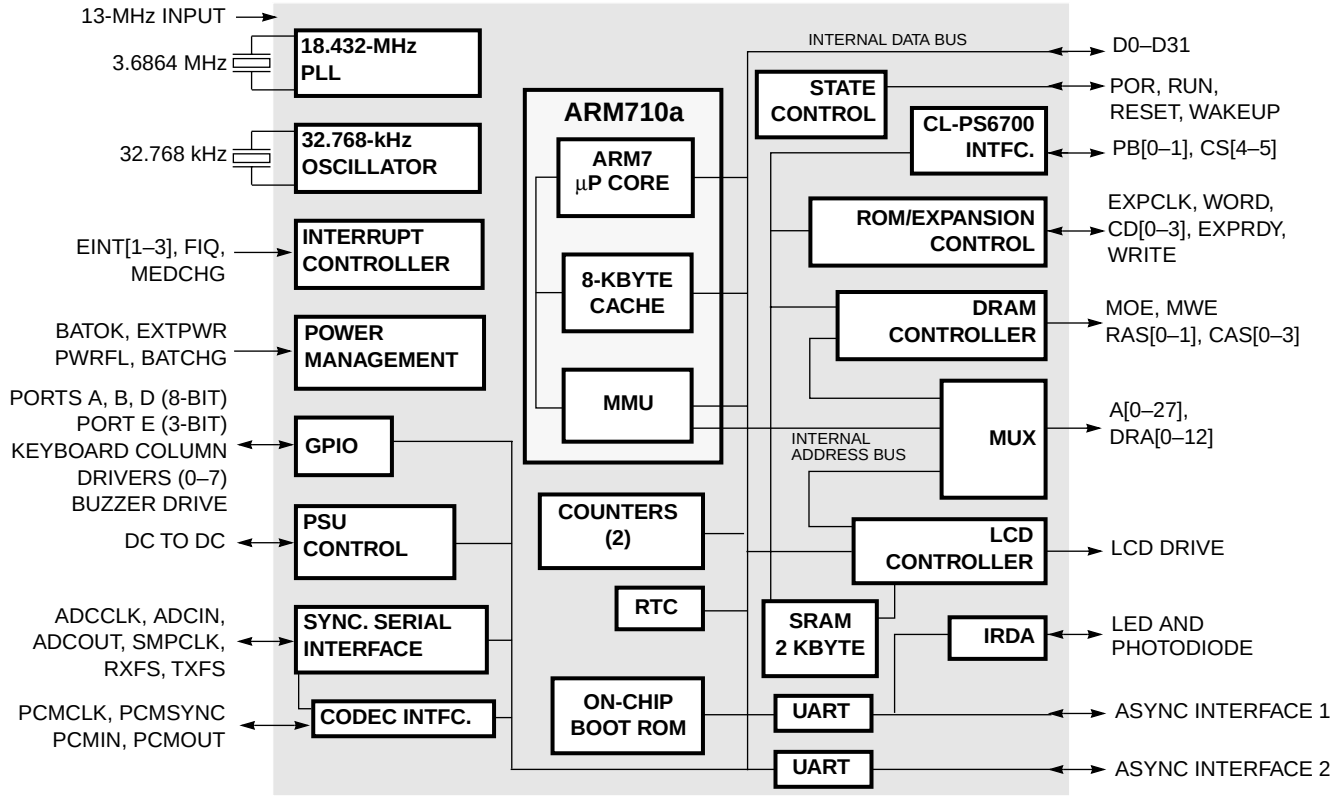
OVERVIEW

The CL-PS7111 is designed for ultra-low-power applications such as organizers/PDAs, two-way pagers, smart phones, and hand-held internet appliances. The core-logic functionality of the device is built around an ARM710a microprocessor with 8 Kbytes of four-way set-associative unified cache.

At 18.432 MHz (for 3.3-V operation), the CL-PS7111 delivers nearly 15 Vax-MIPS of performance (based on Dhrystone® benchmark) — roughly the same level of performance offered by a 33-MHz Intel® '486-based PC.

(cont.)

Functional Block Diagram



FEATURES (cont.)

Mbytes
- — Each segment can be configured as 8, 16, or 32 bits wide and support page-mode access
- — Programmable access time for conventional SRAM/ROM/flash memory

- **Support for up to two ultra-low-power CL-PS6700 PC Card controllers**
- **2 Kbytes of on-chip SRAM for fast program execution**
- **On-chip boot ROM**
- **Two synchronous serial interfaces**
  - — Supports SPI®[1] or Microwire®[2]-compatible
  - — Audio codec
- **27-bit general-purpose I/O**
  - — Three 8-bit and one 3-bit GPIO port
  - — Supports scanning keyboard matrix
- **Two UARTs**
  - — Supports bit rates up to 115.2 kbps
  - — Contains two 16-byte FIFOs for Tx and Rx
  - — Supports modem control signals
- **SIR (slow — up to 115.2 kbps — infrared) encoder**
  - — IrDA (Infrared Data Association) SIR protocol encoder can be optionally switched into Tx and Rx signals of UART 1 up to 115 kbps
- **DC-to-DC converter interface**
  - — Provides two 96-kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16)
- **LCD controller**
  - — Interfaces directly to a single-scan panel monochrome LCD
  - — Panel size is programmable from 16 to 1024 pixels in 16-pixel increments
  - — Video frame size programmable up to 128 Kbytes
  - — Bits per pixel programmable from 1, 2, or 4
- **Timer and counters**
- **3.3 V at 18.432 MHz and 2.7 V at 13 MHz**
- **208-pin VQFP package**
- **Evaluation kit available with BOM, schematics, and design database**

[1] SPI is a registered trademark of Motorola®.

[2] Microwire is a registered trademark of National Semiconductor®.

OVERVIEW (cont.)

As shown in the system block diagram, simply adding desired memory and peripherals to the highly integrated CL-PS7111 completes a hand-held organizer/PDA system board. All the interface logic is integrated on-chip.

Memory Interface

There are two main external memory interfaces and a DMA controller that fetches video display data for the LCD controller from main DRAM memory.

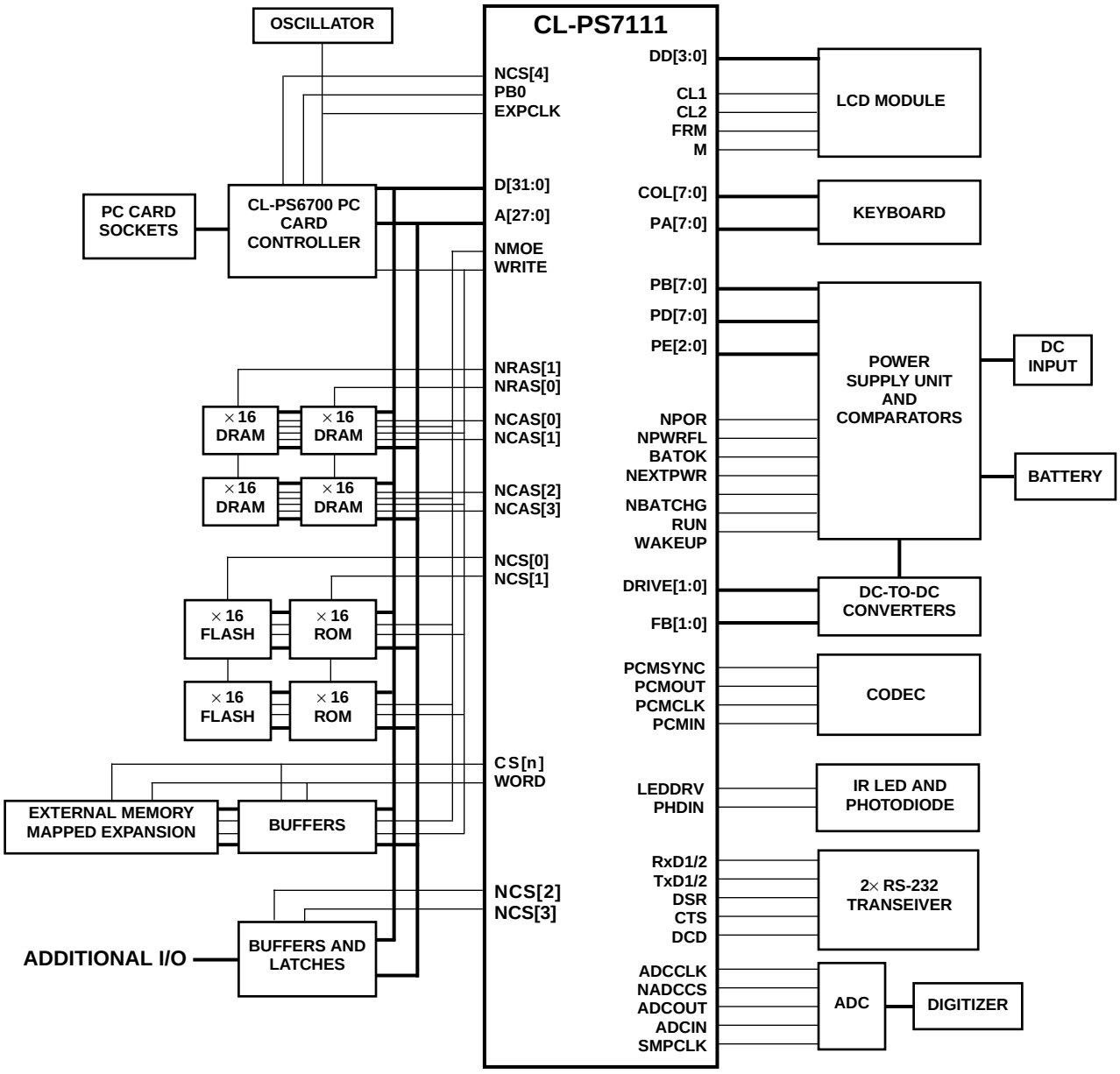
The SRAM/ROM-style interface has programmable wait-state timings and includes burst-mode capability, with six chip selects decoding six 256-Mbyte sections of addressable space. For maximum flexibility, each bank can be specified to be 8, 16 or 32 bits wide to enable the use of low-cost memory in a 32-bit system. The system can have an 8-bit-wide boot option to optimize memory size.

The programmable 16- or 32-bit-wide DRAM interface allows direct connection of up to two banks of DRAM, each bank containing up to 256 Mbytes. To assure the lowest possible power consumption, the CL-PS7111 supports self-refresh DRAMs, which are placed in a low-power state by the device when it enters low-power standby mode.

Serial Interface

For RS-232 serial communications, the CL-PS7111 includes two UARTs, both of which have two 16-byte FIFOs for receive and transmit data. The UARTs support bit rates of up to 115.2 kbps. An IrDA SIR protocol encoder/decoder can be optionally switched into the Rx/Tx signals to/from one of the UARTs to enable these signals to drive an infrared communication interface directly.

A full-duplex codec interface allows direct connection of a standard codec chip to the CL-PS7111, allowing storage and playback of sound. A separate synchronous serial interface supports two industry-standard protocols (SPI® and Microwire®) for interfacing to standard devices such as an ADC, allowing for peripheral expansion such as the use of a digitizer pen.



A CL-PS7111–Based System

OVERVIEW (cont.)

Power Management

The CL-PS7111 is designed for low-power operation. There are three basic power states:

- **Standby —** This state is equivalent to the computer being switched off (no display), and the main oscillator shut down.
- **Idle —** In this state**,** the device is functioning and all oscillators are running, but the processor clock is halted while waiting for an event such as a key press.
- **Operating —** This state is the same as the idle state, except that the processor clock is running.

Packaging

The CL-PS7111 is packaged in a 208-pin VQFP package, with a body size of 28-mm square, a lead pitch of 0.5 mm and thickness of 1.4 mm.

Table of Contents

REVISION HISTORY

Version 1.0 - Initial version, generated March 1997.

Version 2.0 - Generated September 1997.

In addition to minor revisions, the following modifications have been made to the CL-PS7111 Data Book.

List of Revisions

Version	Section	Page	Revision Note
2.0	Features	1	Under ultra low power, the following bullet was added: Average 45mW/66 mW in normal operation (2.7 V/3.3 V, 13 MHz/18.432 MHz).
2.0	Functional Block Diagram	1,19	For the Sync. Serial Interface, the pin names ADCCLK, ADCIN, ADCOUT, and SMPCLK replaced CLK, IN, and OUT. For the Codec Interface, the pin names PCMCLK, PCMSYNC, PCMIN, and PCMOUT replaced CLK, SYNC IN, OUT, and SMPCK.
2.0	3.7 State Control	24	New text was added.
2.0	4. Memory Map	43	This section was moved from Section 3.1 in version 1.0.
2.0	5. Register Descriptions	44 to 72	This section was moved from Section 3.2 in version 1.0. Bit numbers were added to the register descriptions. Register descriptions were also reformatted and reorganized to aid users' understanding.
2.0	Table 5-1	45	In the 'R/W' column, SYSFLG1 (8000.0140) and INTSR1 (8000.0240) were changed from RD to R, and STFCLR (8000.05C0) through STDBY (8000.0840) were changed from WR to W.
2.0	5.9 SYSFLG1	51	A description for the SSIBUSY bit was added.
2.0	5.38 SYSFLG1	71	The following text was added to the description of the CODECEN bit: This bit must always be set to '1'.

1. CONVENTIONS

This section presents acronyms, abbreviations, units of measurement, and conventions used in this data book.

Acronyms and Abbreviations

The following table lists abbreviations and acronyms used in this data book.

Acronym/ Abbreviation	Definition
AC	alternating current
ADC	analog-to-digital
codec	coder/decoder
CMOS	complementary metal-oxide semiconductor
CPU	central processing unit
DC	direct current
DMA	direct-memory access
DRAM	dynamic random-access memory
EPB	embedded peripheral bus
FCS	frame check sequence
FIFO	first in/first out
GPIO	general-purpose I/O
ICT	in circuit test
IR	infrared
IrDA	infrared data association
LCD	liquid-crystal display
LSB	least-significant bit
MIPS	millions of instructions per second

Acronym/ Abbreviation	Definition *(cont.)*
MMU	memory management unit
MSB	most-significant bit
PCB	printed circuit board
PDA	personal digital assistant
PIA	peripheral interface adapter
PLL	phase locked loop
PSU	power supply unit
p/u	pull-up resistor
RAM	random-access memory
RISC	reduced-instruction-set computer
ROM	read-only memory
RTC	realtime clock
SIR	slow (9600–115.2 kbps) infrared
SRAM	static random-access memory
SSI	synchronous serial interface
TLB	translation look-aside buffer
UART	universal asynchronous receiver transmitter
VQFP	very-tight-pitch quad flat pack

Units of Measurement

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz (cycle per second)
Kbyte	kilobyte (1,024 bytes)
kHz	kilohertz
kΩ	kilohm
Mbps	megabits (1,048,576 bits) per second
Mbyte	megabyte (1,048,576 bytes)
MHz	megahertz (1,000 kilohertz)
µF	microfarad
µA	microampere
µs	microsecond (1,000 nanoseconds)
mA	milliampere
ms	millisecond (1,000 microseconds)
ns	nanosecond
V	volt
W	watt

General Conventions

Hexadecimal numbers are presented with all letters in uppercase and a lowercase *h* appended. For example, 14h and 03CAh are hexadecimal numbers. Binary numbers are enclosed in single quotation marks when in text (for example, '11' designates a binary number). Numbers not indicated by an *h* or quotation marks are decimal.

Registers are referred to by acronym, as listed in Table 5-1 and Table 5-2, with bits listed in brackets MSB-to-LSB separated by a colon (:) (for example, CODR[7:0]) or LSB-to-MSB separated by a hyphen (for example, CODR[0–2]).

The use of 'tbd' indicates values that are 'to be determined', 'n/a' designates 'not available', and 'n/c' indicates a pin that is a 'no connect'.

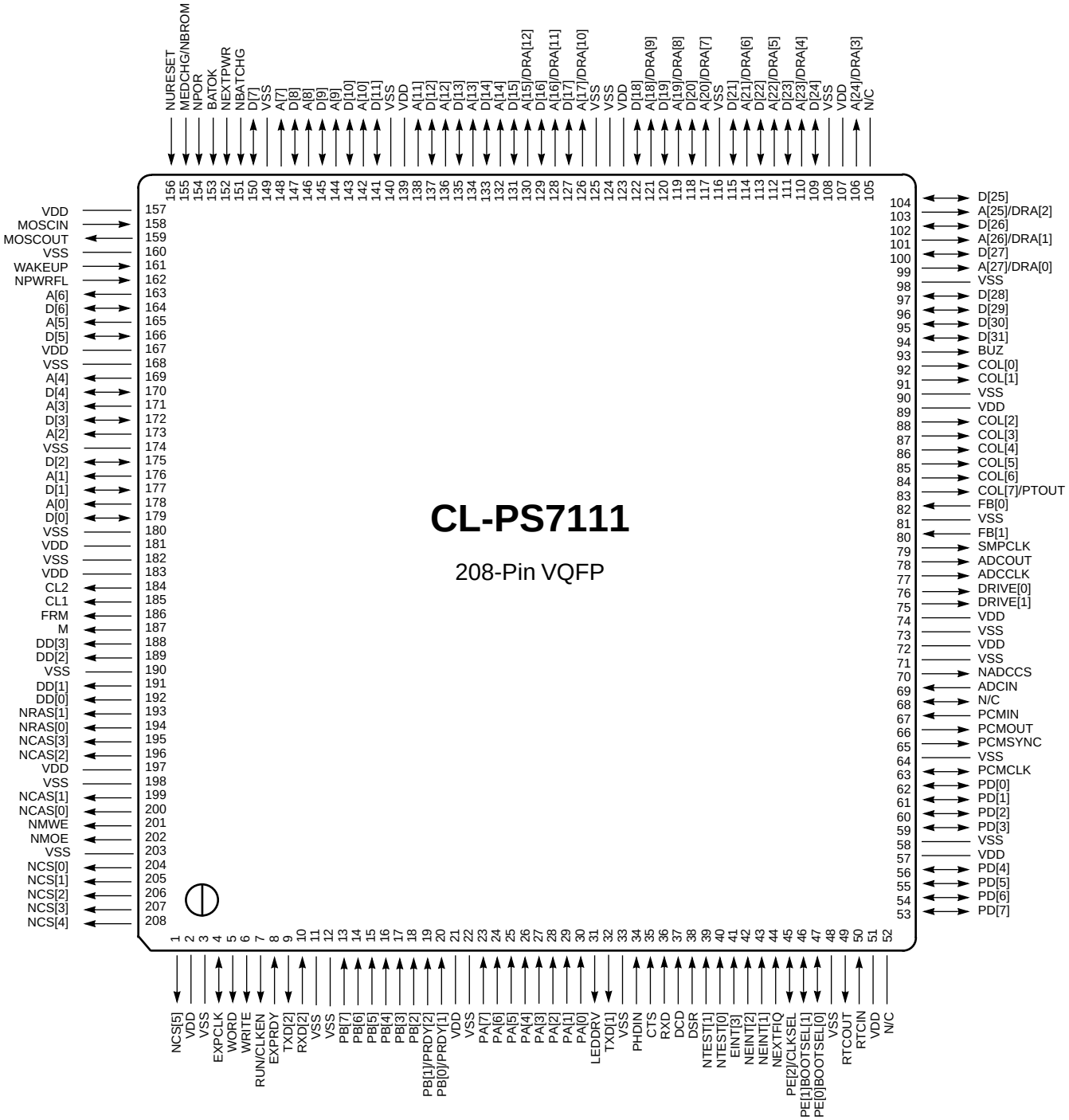
Pin Description Conventions

Abbreviations used for signal directions in Chapter 2 are listed in the following table:

Abbreviation	Direction
I	Input
O	Output
I/O	Input or output

2. PIN INFORMATION

2.1 Pin Diagram



2.2 Pin Descriptions

2.2.1 External Signal Functions

Function	Signal Name	Type	Description
Address and Data Bus	D[0–31]	I/O	32-bit system data bus for DRAM, ROM, and memory-mapped expansion.
	A[0–14]	O	Least-significant 15 bits of system byte address during ROM and expansion cycles.
	A[15]/ DRA[12]– A[27]/DRA[0]	O	13-bit multiplexed DRAM word address during DRAM cycles or address bits 16 to 27 of system byte address during ROM and expansion cycles.
Memory and Expansion Interface	NRAS[0–1]	O	DRAM RAS outputs to DRAM banks 0–1.
	NCAS[0–3]	O	DRAM CAS outputs for bytes 0 to 3 within 32-bit word. NCAS[0] enables D[7:0].
	NMOE	O	DRAM, ROM, and expansion output enable.
	NMWE	O	DRAM, ROM, and expansion write enable.
	NCS[0–3]	O	Expansion channel I/O strobes. Active-low, SRAM-like chip selects for expansion.
	NCS[4–5]	O	Expansion channel I/O strobes. Active-low chip select for expansion of low for CL-PS6700 interface.
	EXPRDY	I	Expansion channel ready. Extends bus cycle when low.
	WRITE	O	Transfer direction. Low during reads, high during writes from the CL-PS7111. Also connected to PTYPE of CL-PS6700.
	WORD	O	Word access enable. Driven high during word-wide cycles; low during byte-wide cycles.
	EXPCLK	I/O	Expansion clock output. Clock output at the same phase and speed as the CPU clock. In 13-MHz mode, this pin is used as the clock input.
Interrupts	MEDCHG/ NBROM	I	Media changed input. Active-high deglitched input for media insertion; should be set low during NPOR to enable boot code.
	NEXTFIQ	I	External active-low fast interrupt request input.
	EINT[3]	I	External active-high interrupt request input.
	NEINT[1–2]	I	Two general-purpose, active-low interrupt inputs.
Power Management	NPWRFL	I	Power fail input. Active-low deglitched input to force system into the standby state.
	BATOK	I	Main battery OK input. Falling edge generates a FIQ; a low level in standby mode inhibits system start up; deglitched input.
	NEXTPWR	I	External power sense. Must be driven low if the system is powered by external source.
	NBATCHG	I	New battery sense. Must be driven low if battery voltage falls below the ‘no-battery’ threshold.

2.2.1 External Signal Functions *(cont.)*

Function	Signal Name	Type	Description
State Control	NPOR	I	Power on reset input. Active-low input completely resets the system.
	RUN/CLKEN	O	System active output. High when system is active or idle, low while in the standby state.
	WAKEUP	I	Wake-up input signal. Rising edge forces system into operating state; active after a power on reset.
	NURESET	I	User reset input. Active-low input from user reset button.
Codec Interface	PCMCLK	I/O	Codec clock signal.
	PCMSYNC	O	Codec frame synchronization, pulse output.
	PCMOUT	O	Codec serial data output.
	PCMIN	I	Codec serial data input.
ADC Interface SSI1	ADCCLK	O	Serial clock output.
	SMPCLK	O	Serial sample clock output.
	NADCCS	O	Chip select for ADC interface.
	ADCOUT	O	Serial data output.
	ADCIN	I	Serial data input.
IrDA and RS-232 Interface	LEDDRV	O	Infrared LED drive output, multiplexed with UART1.
	PHDIN	I	Photo diode input, multiplexed with UART1.
	TxD[1–2]	O	RS-232 UART1 and two Tx outputs.
	RxD[1–2]	I	RS-232 UART1 and two Rx inputs.
	DSR	I	RS-232 DSR input.
	DCD	I	RS-232 DCD input.
	CTS	I	RS-232 CTS input.
LCD	DD[0–3]	O	LCD serial display data.
	CL[1]	O	LCD line clock.
	CL[2]	O	LCD pixel clock.
	FRM	O	LCD frame synchronization pulse output.
	M	O	LCD AC bias drive.

2.2.1 External Signal Functions *(cont.)*

Function	Signal Name	Type	Description
Keyboard	COL[0–7]	O	Keyboard column drives.
Buzzer Drive	BUZ	O	Buzzer drive output in 18.432-MHz mode.
General-Purpose I/O	PA[0–7]	I/O	Port A I/O.
	PB[0–7]	I/O	Port B I/O (default input).
	PD[0–7]	I/O	Port D I/O (higher drive, default output).
	PE[0–2]	I/O	Port E I/O (three bits only, default input).
DC-to-DC Drives	DRIVE[0–1]	O	DC-to-DC converter drive outputs.
	FB[0–1]	I	DC-to-DC feedback inputs.
Test	NTEST[0–1]	I	Test mode select inputs.
Oscillators	MOSCIN/ MOSOUT	I/O	Main 3.6864-MHz oscillator for 18.432-MHz PLL.
	RTCIN/ RTCOUT	I/O	Realtime clock 32.768-kHz oscillator.

2.2.2 Numeric Pin Listing

Pin No.	Signal	Buffer	Reset and Pin Test Reset State	Pin No.	Signal	Buffer	Reset and Pin Test Reset State
1	NCS[5]	I/O - strength 1	Low	27	PA[3]	I/O - strength 1	Input
2	VDD	Pad power	–	28	PA[2]	I/O - strength 1	Input
3	VSS	Pad power	–	29	PA[1]	I/O - strength 1	Input
4	EXPCLK	I/O - strength 1	Low/Input	30	PA[0]	I/O - strength 1	Input
5	WORD	I/O - strength 1	Low	31	LEDDRV	I/O - strength 1	Low
6	WRITE	I/O - strength 1	Low	32	TXD[1]	I/O - strength 1	High
7	RUN/CLKEN	I/O - strength 1	Low	33	VSS	Pad power	–
8	EXPRDY	I/O - strength 1	Input	34	PHDIN	I/O - strength 1	Input
9	TXD[2]	I/O - strength 1	High	35	CTS	I/O - strength 1	Input
10	RXD[2]	I/O - strength 1	Input	36	RXD[1]	I/O - strength 1	Input
11	VSS	Core power	–	37	DCD	I/O - strength 1	Input
12	VSS		–	38	DSR	I/O - strength 1	Input
13	PB[7]	I/O - strength 1	Input	39	NTEST[1]	Input with p/u	High Input
14	PB[6]	I/O - strength 1	Input	40	NTEST[0]	Input with p/u	High Input
15	PB[5]	I/O - strength 1	Input	41	EINT[3]	I/O - strength 1	Input
16	PB[4]	I/O - strength 1	Input	42	NEINT[2]	I/O - strength 1	Input
17	PB[3]	I/O - strength 1	Input	43	NEINT[1]	I/O - strength 1	Input
18	PB[2]	I/O - strength 1	Input	44	NEXTFIQ	I/O - strength 1	Input
19	PB[1]/PRDY[2]	I/O - strength 1	Input	45	PE[2]/CLKSEL	I/O - strength 1	Input
20	PB[0]/PRDY[1]	I/O - strength 1	Input	46	PE[1] / BOOTSEL[1]	I/O - strength 1	Input
21	VDD	Pad power	–	47	PE[0]/ BOOTSEL[0]	I/O - strength 1	Input
22	VSS	Pad power	–	48	VSS	32K oscillator power	–
23	PA[7]	I/O - strength 1	Input	49	RTCOUT	32K oscillator	X
24	PA[6]	I/O - strength 1	Input	50	RTCIN	32K oscillator	X
25	PA[5]	I/O - strength 1	Input	51	VDD	32K oscillator power	–
26	PA[4]	I/O - strength 1	Input	52	N/C[a]		
53	PD[7]	I/O - strength 1	Low	79	SMPCLK	I/O - strength 1	Low

2.2.2 Numeric Pin Listing *(cont.)*

Pin No.	Signal	Buffer	Reset and Pin Test Reset State	Pin No.	Signal	Buffer	Reset and Pin Test Reset State
54	PD[6]	I/O - strength 1	Low	80	FB[1]		Input
55	PD[5]	I/O - strength 1	Low	81	VSS	I/O - strength 1	Input
56	PD[4]	I/O - strength 1	Low	82	FB[0]	I/O - strength 1	Input
57	VDD	Pad power	–	83	COL[7]/ PTOUT	I/O - strength 1	High
58	VSS	Pad power	–	84	COL[6]	I/O - strength 1	High
59	PD[3]	I/O - strength 1	Low	85	COL[5]	I/O - strength 0[b]	High
60	PD[2]	I/O - strength 1	Low	86	COL[4]	I/O - strength 1	High
61	PD[1]	I/O - strength 1	Low	87	COL[3]	I/O - strength 1	High
62	PD[0]	I/O - strength 1	Low	88	COL[2]	I/O - strength 1	High
63	PCMCLK	–	Input	89	VDD	Pad power	–
64	VSS	Core power	–	90	VSS	Pad power	–
65	PCMSYNC	I/O - strength 1	Low	91	COL[1]	I/O - strength 1	High
66	PCMOUT	I/O - strength 1	Low	92	COL[0]	I/O - strength 1	High
67	PCMIN	I/O - strength 1	Input	93	BUZ	I/O - strength 1	Low
68	N/C	I/O - strength 1	Low	94	D[31]	I/O - strength 1	Low
69	ADCIN	I/O - strength 1	Input	95	D[30]	I/O - strength 1	Low
70	NADCCS	I/O - strength 1	High	96	D[29]	I/O - strength 1	Low
71	VSS	Core power	–	97	D[28]	I/O - strength 1	Low
72	VDD	Core power	–	98	VSS	–	
73	VSS	Pad power	–	99	A[27]/DRA[0]	I/O - strength 2	Low
74	VDD	Pad power	–	100	D[27]	I/O - strength 1	Low
75	DRIVE[1]	I/O - strength 3	High/Low	101	A[26]/DRA[1]	I/O - strength 2	Low
76	DRIVE[0]	I/O - strength 3	High/Low	102	D[26]	I/O - strength 1	Low
77	ADCCLK	I/O - strength 1	Low	103	A[25]/DRA[2]	I/O - strength 1	Low
78	ADCOUT	I/O - strength 1	Low	104	D[25]	I/O - strength 1	Low
77	ADCCLK	I/O - strength 1	Low	105	N/C		
78	ADCOUT	I/O - strength 1	Low	106	A[24]/DRA[3]	I/O - strength 1	Low
107	VDD	Pad power	–	136	A[12]	I/O - strength 1	Low
108	VSS	Pad power	–	137	D[12]	I/O - strength 1	Low

2.2.2 Numeric Pin Listing *(cont.)*

Pin No.	Signal	Buffer	Reset and Pin Test Reset State	Pin No.	Signal	Buffer	Reset and Pin Test Reset State
109	D[24]	I/O - strength 1	Low	138	A[11]	I/O - strength 1	Low
110	A[23]/DRA[4]	I/O - strength 1	Low	139	VDD	Pad power	–
111	D[23]	I/O - strength 1	Low	140	VSS	Pad power	–
112	A[22]/DRA[5]	I/O - strength 1	Low	141	D[11]	I/O - strength 1	Low
113	D[22]	I/O - strength 1	Low	142	A[10]	I/O - strength 1	Low
114	A[21]/DRA[6]	I/O - strength 1	Low	143	D[10]	I/O - strength 1	Low
115	D[21]	I/O - strength 1	Low	144	A[9]	I/O - strength 1	Low
116	VSS		–	145	D[9]	I/O - strength 1	Low
117	A[20]/DRA[7]	I/O - strength 1	Low	146	A[8]	I/O - strength 1	Low
118	D[20]	I/O - strength 1	Low	147	D[8]	I/O - strength 1	Low
119	A[19]/DRA[8]	I/O - strength 1	Low	148	A[7]	I/O - strength 1	Low
120	D[19]	I/O - strength 1	Low	149	VSS		–
121	A[18]/DRA[9]	I/O - strength 1	Low	150	D[7]	I/O - strength 1	Low
122	D[18]	I/O - strength 1	Low	151	NBATCHG	I/O - strength 1	Input
123	VDD	Pad power	–	152	NEXTPWR	I/O - strength 1	Input
124	VSS	Pad power	–	153	BATOK	I/O - strength 1	Input
125	VSS	Core power	–	154	NPOR	Schmitt I/O	Input
126	A[17]/DRA[10]	I/O - strength 1	Low	155	MEDCHG/ NBROM	I/O - strength 1	Input
127	D[17]	I/O - strength 1	Low	156	NURESET	Schmitt I/O	Input
128	A[16]/DRA[11]	I/O - strength 1	Low	157	VDD	Osc power	–
129	D[16]	I/O - strength 1	Low	158	MOSCIN	3M6864 Osc	X
130	A[15]/DRA[12]	I/O - strength 1	Low	159	MOSCOUT	3M6864 Osc	X
131	D[15]	I/O - strength 1	Low	160	VSS	Osc power	–
132	A[14]	I/O - strength 1	Low	161	WAKEUP	Schmitt I/O	Input
133	D[14]	I/O - strength 1	Low	162	NPWRFL	I/O - strength 1	Input
134	A[13]	I/O - strength 1	Low	163	A[6]	I/O - strength 1	Input
135	D[13]	I/O - strength 1	Low	164	D[6]	I/O - strength 1	Low
165	A[5]	I/O - strength 1	Low	187	M	I/O - strength 1	Low
166	D[5]	I/O - strength 1	Low	188	DD[3]	I/O - strength 1	Low

2.2.2 Numeric Pin Listing *(cont.)*

Pin No.	Signal	Buffer	Reset and Pin Test Reset State	Pin No.	Signal	Buffer	Reset and Pin Test Reset State
167	VDD	Pad power	–	189	DD[2]	I/O - strength 1	Low
168	VSS	Pad power	–	190	VSS		–
169	A[4]	I/O - strength 1	Low	191	DD[1]	I/O - strength 1	Low
170	D[4]	I/O - strength 1	Low	192	DD[0]	I/O - strength 1	Low
171	A[3]	I/O - strength 2	Low	193	NRAS[1]	I/O - strength 1	High
172	D[3]	I/O - strength 1	Low	194	NRAS[0]	I/O - strength 1	High
173	A[2]	I/O - strength 2	Low	195	NCAS[3]	I/O - strength 1	High
174	VSS		–	196	NCAS[2]	I/O - strength 1	High
175	D[2]	I/O - strength 1	Low	197	VDD	Pad power	–
176	A[1]	I/O - strength 1	Low	198	VSS	Pad power	–
177	D[1]	I/O - strength 1	Low	199	NCAS[1]	I/O - strength 2	High
178	A[0]	I/O - strength 1	Low	200	NCAS[0]	I/O - strength 2	High
179	D[0]	I/O - strength 1	Low	201	NMWE	I/O - strength 1	High
180	VSS	Core power	–	202	NMOE	I/O - strength 1	High
181	VDD	Core power	–	203	VSS		–
182	VSS	Pad power	–	204	NCS[0]	I/O - strength 1	High
183	VDD	Pad power	–	205	NCS[1]	I/O - strength 1	High
184	CL[2]	I/O - strength 1	Low	206	NCS[2]	I/O - strength 1	High
185	CL[1]	I/O - strength 1	Low	207	NCS[3]	I/O - strength 1	High
186	FRM	I/O - strength 1	Low	208	NCS[4]	I/O - strength 1	Low

[a] Pins that are ‘no connect’ (N/C) may have a signal.

[b] Also has analog bypass path for oscillator test.

3. FUNCTIONAL DESCRIPTION

The CL-PS7111 is a single-device embedded controller designed to be used in low-cost and low-power applications such as hand-held personal organizers and hand-held internet browsers. There are other devices offered by Cirrus Logic (http://www.cirrus.com) that can be used around the CL-PS7111 to build a complete hand-held organizer, such as the CL-PS6700 PCMCIA controller, fax/modem chipsets, IR chipsets, codecs, and so on. The CL-PS7111 operates at 2.7 V (at 13.0 MHz) or 3.3 V (at 18.432 MHz).

The various peripheral functions are built around an ARM710a microprocessor with 8 Kbytes of four-way set-associative cache. At 18.432 MHz the CL-PS7111 delivers approximately 15 MIPS of sustained performance and 18.4 MIPS of peak performance. This is approximately the same as a 33-MHz ’486-based PC.

The CL-PS7111 design is optimized for low-power dissipation. At 3.3 V and 18.432-MHz clock speed, the device typically dissipates 66 mW during the ‘operating state’ (all oscillators, PLL, LCD, and processor clock running), 15 mW in the ‘idle state’ (all oscillators and LCD running, but processor clock is halted), and 15 µW in the ‘standby state’ (no display and the main oscillator is shut down). At 2.7 V and 13.0 MHz, the respective values are 45 mW, 9 mW, and 15 µW.

The CL-PS7111 can interface to two banks of DRAM; each bank can be up to 256 Mbytes. There is also an interface for two ROM/flash and three expansion devices, each up to 256 Mbytes, and an interface to two CL-PS6700 PCMCIA controllers. The expansion devices could be additional ROM/SRAM/Flash. In addition, the CL-PS7111 provides 2 Kbytes of on-chip SRAM and internal 128 bytes of boot ROM. The SRAM may be used for critical program storage as well as LCD frame buffer. The start address of the frame buffer can reside anywhere in the addressable memory space. A system can therefore be designed with SRAM only for very low power applications.

The boot ROM is hardware selectable on power-on or reset. This boot ROM initializes UART1 and downloads the application-specific main boot code into the on-chip SRAM. Once download is complete, execution jumps to the start of the on-chip SRAM.

The CL-PS7111 supports a number of serial interfaces including two high-speed (115 kbps) UARTs with Rx and Tx FIFOs, a codec interfaces with FIFO and an additional synchronous serial interface.

The CL-PS7111 is fabricated in a 0.6-µm CMOS process and is fully static. The CL-PS7111 is available in a 208-pin VQFP package.

Figure 3-1 shows a system-level block diagram for the CL-PS7111. As is shown, all the peripherals (such as the LCD module, keyboard, PCMCIA socket, and so on) can be added without any glue logic.

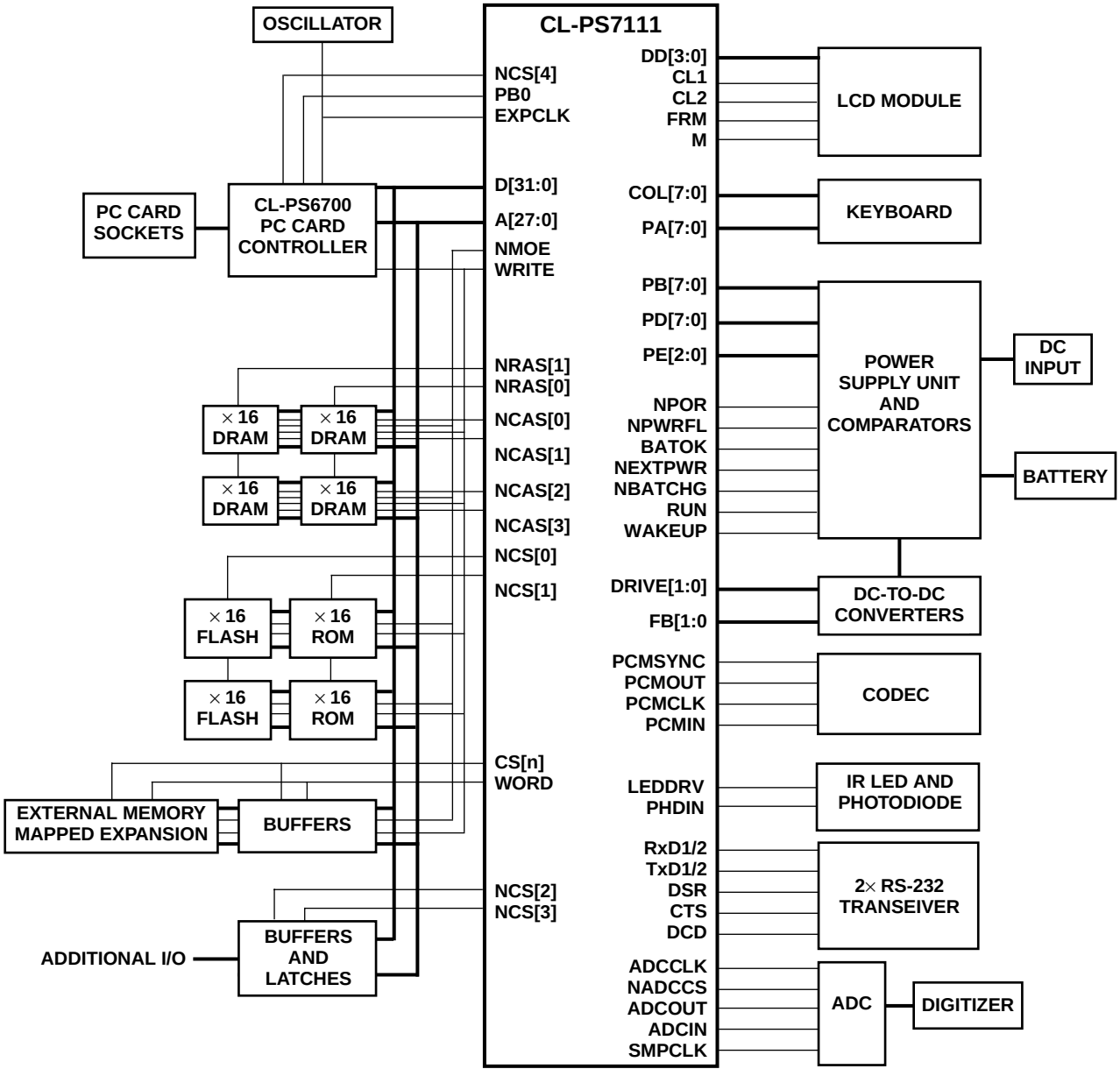


Figure 3-1. System-Level Block Diagram

3.1 Main Functional Blocks

The CL-PS7111 is built around the ARM710a processor core. For a more detailed description of the ARM710a, refer to the *ARM710a Macrocell Data Sheet* (http://www.arm.com/).

The main functional blocks in CL-PS7111 are:

- ARM7 CPU core
- 8 Kbytes of unified instruction and data cache, a four-way set-associative
- Memory management unit (MMU)
- Two 16-bit general-purpose counters
- A 32-bit realtime clock and comparator
- On-chip boot ROM programmed with serial boot load sequence
- Advanced system state control and power management
- Direct interface to two CL-PS6700 PCMCIA controllers
- Expansion and ROM interface for four, five, or six 256-Mbyte expansion segments with independent wait state control
- DRAM controller supporting Fast Page mode, self-refresh in Standby mode, and both 16-bit and 32-bit-wide memory
- Programmable LCD controller with 1-, 4-, or 16-level grayscaler
- 2 Kbytes of SRAM for a small LCD frame buffer
- IrDA SIR protocol controller, capable of speeds up to 115.2 kbps
- Two full-duplex 16C550 style UARTs with two 16-byte FIFOs
- Main oscillator with PLL (phase locked loop) to generate the system clock of 18.432 MHz from a 3.6864-MHz crystal
- Optional external 13-MHz clock input
- A low-power 32.768-kHz oscillator
- Interrupt and fast interrupt controller
- 27 bits of general-purpose I/Os
- Two DC-to-DC converter interfaces
- One synchronous serial interface for Microwire® or SPI® peripherals (such as ADCs)
- Telephony codec interface with 16-byte FIFOs for transmit and receive
- Programmable frame buffer start address, allowing a system to be built using only external or internal SRAMs for memory, eliminating any need for DRAMs
- Pin test and device-isolation test logic
- External tracing support for debug

Figure 3-2 shows a simplified functional block diagram of the CL-PS7111. All external memory and peripheral devices are connected to the 8-, 16-, or 32-bit data bus, using the external 28-bit address bus and control signals. Bus transfer times can be extended by using the EXPRDY signal to lengthen bus cycles. The maximum burst transfer rate of the external bus is approximately 70 Mbytes per sec. using 32-bit-wide DRAM at 18.432 MHz or 25 Mbytes per sec. using 16-bit-wide DRAM at 13 MHz.

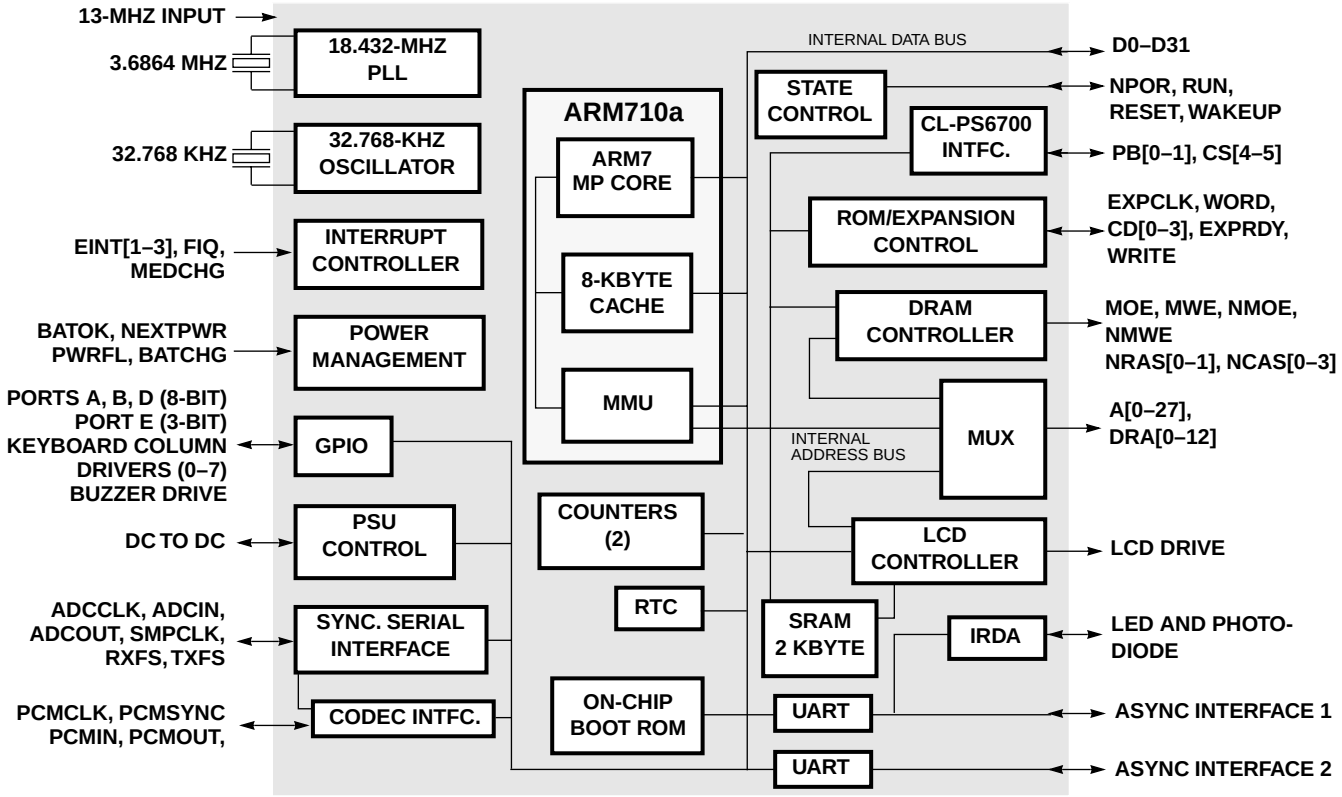


Figure 3-2. CL-PS7111 Block Diagram

3.2 System Maximization

A maximum-configured system using the CL-PS7111 is shown in Figure 3-3. This system assumes all DRAMs and ROMs are 16-bit-wide devices. Watch-dog-timer tick rate is 1 Hz (in 13-MHz and 18.432-MHz modes). This 1-Hz clock is generated by a divider chain that divides the 64-Hz clock. The LSB of the RTCDIV field (SYSFLG[21:16]) provides the 1-Hz clock.

NOTE: The keyboard can be connected to more GPIO bits than illustrated to allow more than 64 keys. These extra pins, however, will not be wired into the WAKEUP pin functionality.

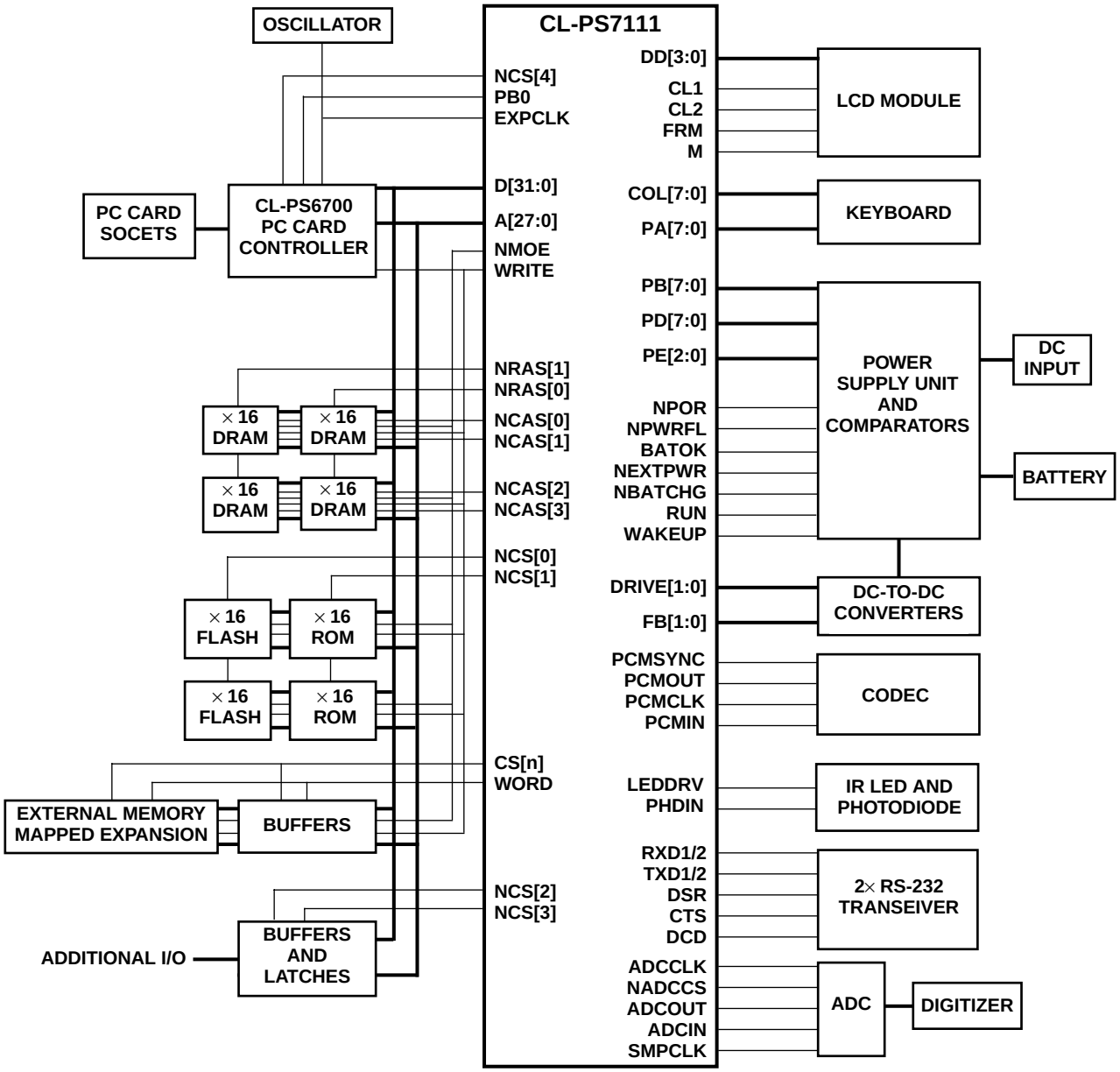


Figure 3-3. A Maximized CL-PS7111–Based System

3.3 Endian Functionality

The CL-PS7111 uses a little-endian configuration for internal registers. However, it is possible to connect the device to a big-endian external memory system. Table 3-1 and Table 3-2 demonstrate the behavior of the CL-PS7111 in big- and little-endian mode, including the effect of performing non-aligned word accesses. The register definitions in Chapter 5 define the behavior of the internal CL-PS7111 registers in big-endian mode in more detail.

The NCAS[3:0] lines for DRAM must always be connected with the same byte lane regardless of the endian functionality, so that NCAS[0] is connected with D[7:0], and NCAS[3] with D[31:24]. In a little-endian system, NCAS[0] is asserted for a read/write to byte 0 of DRAM and in a big-endian system NCAS[3] is asserted to access byte 0 of DRAM.

Table 3-1. Endian Functionality and Read Operations

Address (W/B)	Data in Memory	Byte Lanes to Memory/Ports/Registers								R0 Contents	
		Big-endian Memory				Little-endian Memory				Big-endian	Little-endian
		7:0	15:8	23:16	31:24	7:0	15:8	23:16	31:24		
Word + 0 (W)	11223344	44	33	22	11	44	33	22	11	11223344	11223344
Word + 1 (W)	11223344	44	33	22	11	44	33	22	11	44112233	44112233
Word + 2 (W)	11223344	44	33	22	11	44	33	22	11	33441122	33441122
Word + 3 (W)	11223344	44	33	22	11	44	33	22	11	22334411	22334411
Word + 0 (B)	11223344	X[a]	X	X	11	44	X	X	X	00000011	00000044
Word + 0 (B)	11223344	X	X	22	X	X	33	X	X	00000022	00000033
Word + 0 (B)	11223344	X	33	X	X	X	X	22	X	00000033	00000022
Word + 0 (B)	11223344	44	X	X	X	X	X	X	11	00000044	00000011

[a] X indicates a 'don't care' state.

Table 3-2. Endian Functionality and Write Operations

Address (W/B)	Register Contents	Byte Lanes to Memory/Ports/Registers							
		Big-endian Memory				Little-endian Memory			
		7:0	15:8	23:16	31:24	7:0	15:8	23:16	31:24
Word + 0 (W)	11223344	44	33	22	11	44	33	22	11
Word + 1 (W)	11223344	44	33	22	11	44	33	22	11
Word + 2 (W)	11223344	44	33	22	11	44	33	22	11
Word + 3 (W)	11223344	44	33	22	11	44	33	22	11
Word + 0 (B)	11223344	44	44	44	**44**[a]	**44**	44	44	44

Table 3-2. Endian Functionality and Write Operations *(cont.)*

Address (W/B)	Register Contents	Byte Lanes to Memory/Ports/Registers							
		Big-endian Memory				Little-endian Memory			
		7:0	15:8	23:16	31:24	7:0	15:8	23:16	31:24
Word + 0 (B)	11223344	44	44	**44**	44	44	**44**	44	44
Word + 0 (B)	11223344	44	**44**	44	44	44	44	**44**	44
Word + 0 (B)	11223344	**44**	44	44	44	44	44	44	**44**

[a] Bold indicates active byte lane.

3.4 CPU Core

The ARM710a microprocessor is a 32-bit RISC processor with an 8-Kbyte unified cache. This cache has 512 lines of four words arranged as a four-way set association. The cache is directly connected to the ARM710a microprocessor and caches the *virtual address* from the processor. The MMU translates the virtual address into a physical address, and contains a 64-entry TLB (translation look aside buffer) and is *post cache*; that is, it only translates external memory references (cache misses) to save power.

The big end bit in the ARM710a control register sets whether the CL-PS7111 treats words in memory as being stored in big-endian or little-endian format. See Chapters 5 and 11 of the *ARM710a Macrocell Data Sheet* for more information on the control register. Memory is viewed as a linear collection of bytes numbered upwards from zero. Bytes 0 to 3 hold the first stored word, bytes 4 to 7 the second, and so on. In the little-endian scheme, the lowest numbered byte in a word is considered to be the least-significant byte of the word, and the highest numbered byte is the most-significant. Byte 0 of the memory system should be connected to data lines 7 through 0 (D[7:0]) in this scheme. In the big-endian scheme, the most-significant byte of a word is stored at the lowest numbered byte and the least-significant byte is stored at the highest numbered byte. However, the memory controller of the CL-PS7111 will align the byte lane such that byte 0 of the memory system may always be connected to D[7:0]. Load and store are the only instructions affected by the endian functionality. For details on the ARM7 instruction set and CPU architecture, refer to the *ARM710a Macrocell Data Sheet*.

3.5 Counters

The CL-PS7111 has two integrated identical timer counters: TC1 and TC2. Each timer counter has an associated 16-bit read/write data register and control bits in the System Control registers. Each counter is immediately loaded with the value written to the data register. This value decrements on the second active clock edge, arriving after the write (after the first complete period of the clock). When the timer counter underflows (reaches 0) the appropriate interrupt asserts. The timer counters can be read at any time. The clock source and mode are selected by writing to various bits in the System Control registers. Clock sources, when running from an 18.432-MHz master clock, are 512kHz and 2 kHz. When using the 13-MHz source, the default frequencies are 541 kHz and 2.115 kHz, respectively. However, in non-PLL mode, an optional divide by 26 frequency can be generated, thus generating a 500-kHz frequency when using the 13-MHz source. This divider is enabled by setting OSTB (Operating System Timing in SYSCON2[12]). When OSTB is set high to select the 500-kHz mode, the 500-kHz frequency is routed to the timers instead of 512 kHz. This does not affect the frequencies derived from any of the other internal peripherals.

The timer counters can operate in two modes: free-running or prescale.

3.5.1 Free-Running Mode

In free-running mode, the counter wraps around to 0xFFFF, then underflows and continues to count down. Any value written to TC1 or TC2 decrements on the second edge of the selected clock.

3.5.2 Prescale Mode

In prescale mode, the value written to TC1 or TC2 automatically reloads when the counter underflows. Any value written to TC1 or TC2 decrements on the second edge of the selected clock. This mode can produce a programmable frequency to drive the buzzer or generate a periodic interrupt.

3.6 Realtime Clock

The CL-PS7111 contains a 32-bit RTC (realtime clock). The RTC is written and read the same as the timer counters, but is 32 bits wide. The RTC is always clocked at 1 Hz, generated from the 32.768-kHz oscillator. It also contains a 32-bit output-match register, that can be programmed to generate an interrupt when the time in the RTC matches a specific time written to this register. The RTC is only reset by an NPOR cold reset. Because the Realtime Clock Data register is updated from the 1-Hz clock derived from the 32-kHz source (asynchronous to the main memory system clock) the data register must always be read twice to ensure a valid and stable reading. This also applies when reading back the RTCDIV field (SYSFLG1[21:16]), reflecting the status of the six LSBs of the realtime clock counter.

3.7 State Control

The CL-PS7111 supports three operating states: standby, idle, and operating.

In the following descriptions, the RUN/CLKEN pin is used for the run functionality or the CLKEN functionality, allowing an external oscillator to be disabled in 13-MHz mode. Either RUN or CLKEN functionality is selected according to the state of CLKENSL bit (SYSCON2[[13]).

Table 3-3 shows how different modules in CL-PS7111 behave in different states.

Table 3-3. Peripheral Status in Different Operating States

Module	Operating	Idle	Standby	NPOR Reset	NURESET Reset
DRAM Ctrl	ON	ON	Self refresh	OFF	Self refresh
UARTs	ON	ON	OFF	Reset	Reset
LCD FIFO	ON	ON	Reset	Reset	Reset
LCD	ON	ON	OFF	Reset	Reset
ADC Interface	ON	ON	OFF	Reset	Reset
Codec	ON	ON	OFF	Reset	Reset
Timers	ON	ON	OFF	Reset	Reset
RTC	ON	ON	ON	ON	ON
DC-to-DC	ON	ON	OFF	Reset	Reset
CPU	ON	OFF	OFF	Reset	Reset

Table 3-3. Peripheral Status in Different Operating States *(cont.)*

Module	Operating	Idle	Standby	NPOR Reset	NURESET Reset
Interrupt Ctrl	ON	ON	ON	Reset	Reset
PLL/CLKEN	ON	ON	OFF	OFF	OFF

Standby State

The standby state is as if the computer is switched off, there is no display and the main oscillator is shut down. When the 18.432-MHz mode is selected, the PLL will be shut down. In 13-MHz mode, if the CLKENSL bit is set low, then the CLKEN signal will be forced low and can disable an external oscillator. Only the realtime clock is running. The device automatically enters the standby state after power is first applied or after a system reset. The only exit from the standby state is to the operating state. Before entering the standby state, if external I/O devices (such as CL-PS6700s connected to NCS[4] or NCS[5]) are in use, the software must check for idle before issuing the write to the standby location.

When in standby, all system memory and states are maintained and the system clock is kept current. The PLL/on-chip oscillator or external oscillator is disabled, and the system is static except for the low-power (32-kHz) watch crystal oscillator and divider chain to the realtime clock. The RUN signal is driven low. This signal can be used externally in the system to power down other system modules.

Idle State

The idle state means the device is functioning, but the processor clock is halted while it waits for an event, such as a key press, to generate an interrupt (a rising edge on the external wake-up pin or a rising edge on the decode of Port A bits 0–5 or 7). The PLL (in 18.432-MHz mode) or the external 13-MHz clock source always remains active in the idle state.

Operating State

The operating state is the same as the idle state, except that the processor clock is running.

The device is forced into the standby state at power up or reset by the NPOR signal (called a ‘cold’ reset) and is the only completely asynchronous reset to the CL-PS7111. The transition to the operating state is caused by a rising edge on the WAKEUP input signal, or by a rising edge on any of the Port A bits 0–5 or 7 (corresponding to keyboard input). After a cold reset, these are the only possible events for waking up the device. When entering the standby state from the operating state, the software should leave some interrupt sources enabled, meaning there is a third possible means of exit from the standby state if an enabled interrupt is generated (for example, the RTC interrupt). Once self-refresh is enabled for the DRAMs, any transition to the standby state forces the DRAMs to the self-refresh state before stopping the PLL or external oscillator.

Once in the operating state, the idle state is entered by writing to a special internal memory location in the CL-PS7111. If an interrupt or wake-up event occurs, execution of the next instruction continues in the operating state. A write to the STDBY-WAKEUP internal memory location causes the transition from the operating state to the standby state.

The system can also be forced into the standby state by hardware if the NPWRFL or NURESET inputs are forced low. In this case, the transition is synchronized with DRAM cycles to avoid errors or short cycles.

The system only transitions to the operating state from the standby state if either the NEXTPWR input is low or the BATOK and NPWRFL inputs are high. This prevents the system attempting to start when the power supply is inadequate (for example, when the main batteries are flat corresponding to a low level in NPWRFL or BATOK).

From standby mode, when the WAKEUP signal is applied, the CL-PS7111 initializes into a ready-to-start state and waits for the first clocks, although the CPU is still held in reset. When the first clock is applied, there is a delay of about eight clocks before the CPU is first clocked.

Figure 3-4 is a state diagram for the CL-PS7111.

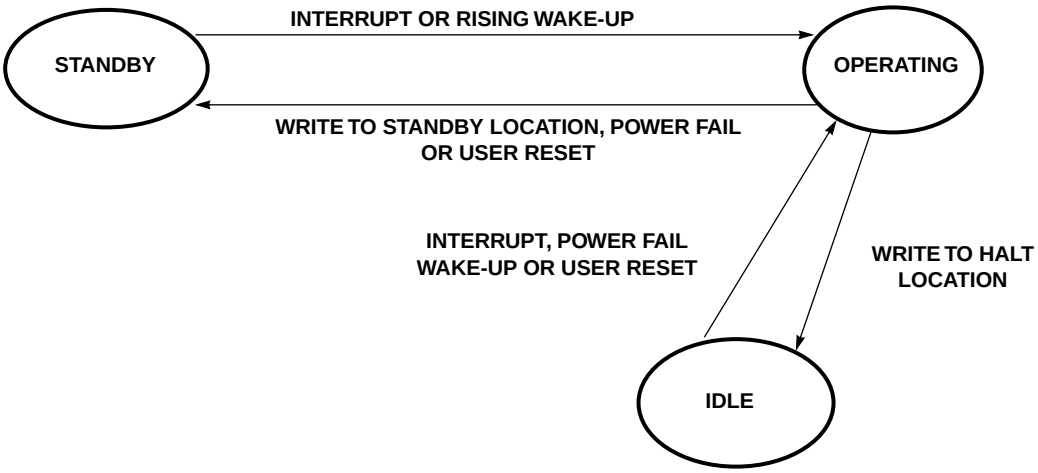


Figure 3-4. State Diagram

3.8 Expansion and ROM Interface

Six separate linear memory or expansion segments are decoded by the CL-PS7111, two of which can be reserved for two PCMCIA cards each interfacing to the single device CL-PS6700. Each segment is 256 Mbytes and can be interfaced by using a conventional SRAM-like interface. Aside from the six segments, an additional segment is dedicated for the on-chip 2 Kbytes of SRAM and is fully decoded such that the addresses for the SRAM do not repeat within the bank. Any of the six segments can be individually programmed to be 8-, 16-, or 32-bits wide, support Page mode access, and execute from 1–4 wait states for nonsequential accesses, and 0–3 for burst mode accesses. The zero-wait-state sequential access feature is designed to support burst mode ROMs; for writable memory devices that use the NMWE pin, zero-wait-state sequential accesses are not permitted and one wait state is the minimum that should be programmed in the sequential field of the appropriate MEMCFG register. Bus cycles can also be extended using the EXPRDY input signal. Page mode access is accomplished by running up to four accesses together. This can significantly improve bus bandwidth to devices such as ROMs. Sequential Burst mode access is always faulted (the bus returned to idle) after four accesses, regardless of bus width to allow DMA and refresh cycles to occur.

Bits 5 and 6 of the SYSCON2 register (see Section 5.38 on page 70) independently enable the interfaces to the CL-PS6700 (PCMCIA slot drivers). When either of these interfaces are enabled, the corresponding device select (NCS4 and/or NCS5) becomes dedicated to that CL-PS6700 interface. The state of SYSCON2[5] determines the function of device select NCS4 (such as the CL-PS6700 interface or standard device select functionality); SYSCON2[6] controls NCS5 in a similar way. There is no interaction between these bits.

For applications that require a small display (such as an alphanumeric one-way pager), on-chip SRAM can be used as the frame buffer and no external DRAM are required.

The width of the boot device can be chosen by selecting values of PE[1] and PE[0] during power on reset. These inputs are latched by the rising edge of NPOR to select the boot option. See Table 3-4 for boot options.

Table 3-4. Boot Options

PE1	PE0	Boot Block (NCS[0])
0	0	32 bit
0	1	8 bit
1	0	16 bit
1	1	Undefined

3.8.1 CL-PS7111 Boot ROM

The 128 bytes of on-chip Boot ROM contain an instruction sequence to initialize the device, then configures UART1 to receive serial data that will then be placed in the 2-Kbyte on-chip SRAM. Once the download is complete, execution will start at the beginning of the on-chip SRAM. This would allow (for example) code to be downloaded to program system flash during a product's manufacturing process. See Appendix A for details on the ROM Boot Code with comments to describe the stages of execution.

Selection of the Boot ROM option is determined by the state of the MEDCHG pin during power-on reset. If MEDCHG is high while NPOR is active, then the CL-PS7111 will boot from an external memory device connected to NCS0 (normal boot mode). If MEDCHG is low, then the boot will be from the on-chip ROM. Note that in both cases, following the deassertion of power on reset, the CL-PS7111 will be in standby mode and requires a low-to-high transition on the external wake-up pin to actually start the boot sequence.

The effect of booting from the on-chip Boot ROM is to reverse the decoding for all device selects internally. In addition, the sense of bit 1 in the Memory Configuration register is reversed so that 00 = 8 bit access. Table 3-5 lists the device select address ranges, and Table 3-6 shows the bus width field combinations that apply after the device has been booted from the on-chip Boot ROM. The control signal for the boot option is latched by NPOR, which means that the remapping of addresses and bus widths will continue to apply until NPOR is asserted again. After booting from the Boot ROM, the contents of the Boot ROM can be read back from address 0x00000000 and in normal mode of operation the Boot ROM, contents can be read back from address 0x70000000.

Table 3-5. Device Select Address Ranges After Boot From On-Chip Boot ROM

Address Range (Hexadecimal)	Chip Select
0000.0000 – 0FFF.FFFF	CS[7] (internal only)
1000.0000 – 1FFF.FFFF	CS[6] (internal only)
2000.0000 – 2FFF.FFFF	NCS[5]
3000.0000 – 3FFF.FFFF	NCS[4]

Table 3-5. Device Select Address Ranges After Boot From On-Chip Boot ROM *(cont.)*

Address Range (Hexadecimal)	Chip Select
4000.0000 – 4FFF.FFFF	NCS[3]
5000.0000 – 5FFF.FFFF	NCS[2]
6000.0000 – 6FFF.FFFF	NCS[1]
7000.0000 – 7FFF.FFFF	NCS[0]

Table 3-6. Expansion And ROM Interface Bus Width After Boot From On-Chip Boot ROM

Bus Width Field In ROM Test Mode	Expansion Transfer Mode
00	8-bit-wide bus access
01	Reserved
10	32-bit-wide bus access
11	16-bit-wide bus access

3.8.2 CL-PS6700 PCMCIA controller interface

Figure 3-5 shows the interface between the CL-PS6700 and the CL-PS7111. For details on the CL-PS6700, please refer to the *CL-PS6700 Data Book* (available under NDA).

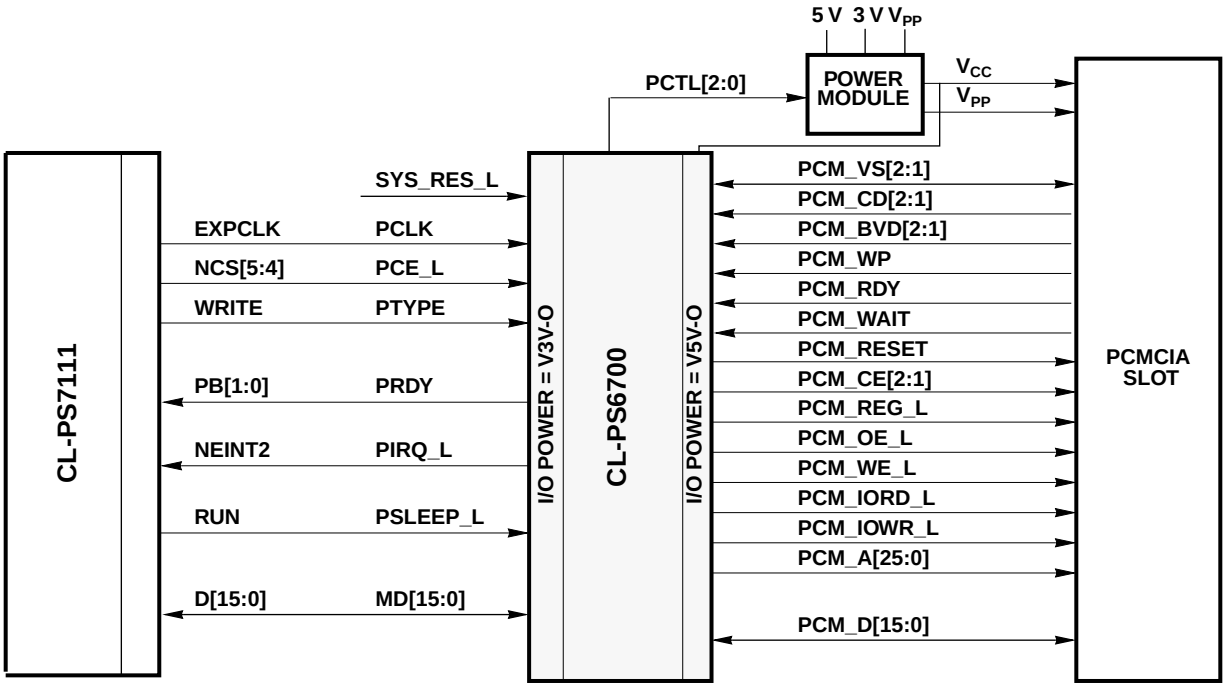


Figure 3-5. CL-PS7111-to-CL-PS6700 Interface

Two expansion memory areas are dedicated to supporting up to two CL-PS6700 PCMCIA controllers. These are selected by NCS[4] and NCS[5] (once enabled by bits 5 and 6 of SYSCON2 respectively). For efficient, low-power operation, both address and data are carried on the lower 16 bits of the CL-PS7111 data bus. Accesses are initiated by a read or write to or from the area of memory allocated for NCS[4] or NCS[5]. The memory map within each of these areas is segmented to allow different types of PCMCIA access to take place for attribute, I/O, and common memory space. The CL-PS6700 internal registers are memory mapped within the address space as shown in Table 3-7.

Table 3-7. CL-PS6700 Memory Map

Access Type	Addresses for CL-PS6700 Interface 1	Addresses for CL-PS6700 Interface 2
Attribute	0x40000000 – 0x43FFFFFF	0x50000000 – 0x53FFFFFF
I/O	0x44000000 – 0x47FFFFFF	0x54000000 – 0x57FFFFFF
Common Memory	0x48000000 – 0x4BFFFFFF	0x58000000 – 0x5BFFFFFF
CL-PS6700 registers	0x4C000000 – 0x4FFFFFFF	0x5C000000 – 0x5FFFFFFF

An access to one of the CL-PS6700 devices will occur according to the following protocol and the timing in the AC timing specifications in Chapter 6: ELECTRICAL SPECIFICATIONS on page 71. A transaction is initiated by an access to the NCS4 or NCS5 area. The chip select is asserted and, on the first clock, the upper 10 bits of the PCMCIA address (along with 6 bits of size, space and slot information) are put out onto the lower 16 bits of the CL-PS7111 data bus. Only word and single-byte accesses are supported and the slot field is hardcoded to '11', as the chip selects are used to select the device to be accessed. This avoids the need to configure the interface during reset. The space field is made directly from the A26 and A27 CPU address bits, according to the decode shown in Table 3-8. The size file is forced to '11' if a word access is required, or '00' for a byte access. On the second clock cycle, the remaining 16 bits of the PCMCIA address are multiplexed out onto the lower 16 bits of the data bus. If the transaction selected is a CL-PS6700 register transaction, or a write to the PCMCIA card (assuming there is space available in the write buffer) then the access will continue on the following two clock cycles, during which the upper and lower halves of the word to be read or written will be put onto the lower 16 bits of the main data bus.

Table 3-8. Space Field Decoding

Space Field Value	PCMCIA Memory Space
00	Attribute
01	I/O
10	Common Memory
11	CL-PS6700 registers

PCMCIA writes can be posted to the CL-PS6700 device with the same timing as CL-PS6700 internal register writes, and are completed by the CL-PS6700 device independent of processor activity. If a posted write times out or fails to complete, the CL-PS6700 will issue an interrupt. When the write queue is already full, the PRDY signal deasserts and the transaction waits pending an available slot in the queue. In this case the CPU waits until the write can be posted successfully.

The 'ptype' signal to the CL-PS6700 should be connected to the CL-PS7111 WRITE output. During PCMCIA accesses, the polarity of this pin changes and becomes low to signify a write and high to signify a

read, becoming valid with the first half word of the address. During the second half word of the address it is always forced high to meet the requirement of the CL-PS6700.

The PRDY signals from each of the two CL-PS6700 devices are connected to Port B bits 0 and 1, respectively. When the PCMCIA 1 or 2 control bits in the SYSCON2 register are deasserted, these port bits are available for GPIO. Each PRDY indicates that the CL-PS6700 device driving the PRDY signal is busy accessing cards if there is no transaction in progress between the CL-PS7111 and CL-PS6700. If a PCMCIA access is attempted while the device is busy, the CPU waits for the card to become available, but DMA for the LCD continues. The CL-PS7111 can access the registers in the CL-PS6700, regardless of the state of the PRDY signal. If the CL-PS7111 needs to access the PCMCIA card through the CL-PS6700, it waits until the PRDY signal is high before initiating a transfer request. Once a request is sent, PRDY indicates whether data is available.

For PCMCIA reads, the PRDY signal from the CL-PS6700 deasserts until the read data is ready, when it is reasserted and the access completes in the same way as a register access. For a byte access, only one 16-bit data transfer is required to complete the access. While PRDY is deasserted, the device select to the CL-PS6700 is deasserted and the main bus released so that DMA for the LCD controller can continue in the background. The CL-PS7111 will rearbitrate for control of the bus when the PRDY signal is reasserted to indicate that the read or write transaction can complete. The CPU is always stalled until the PCMCIA access completes.

A card read operation can be split into a request cycle and a data cycle, or combined into a single request/data transfer cycle, depending on whether the data requested from the card is available in the prefetch queue of the selected CL-PS6700.

The request portion of the cycle for a card read is similar to the request phase for a card write previously described. If the requested data is available in the prefetch queue, the CL-PS6700 asserts PRDY before the rising edge of the third clock and the CL-PS7111 continues the cycle to read the data. Otherwise, PRDY is deasserted and the request cycle completes. The CL-PS7111 then allows the DMA controller to gain control of the bus allowing LCD refreshes to continue. When the CL-PS6700 is ready with the data, it asserts the PRDY signal. The CL-PS7111 then arbitrates for the bus and once the request is granted the suspended read cycle resumes. The CL-PS7111 resumes the cycle by asserting the appropriate chip select and data transfers on the next two clocks.

There is no support within the CL-PS7111 for detecting time-outs. The CL-PS6700 must be programmed to force the cycle to complete (with invalid data for a read) and generate an interrupt if a read or write access is timed out. The system software can then determine which access was not successfully completed by reading the status registers within the CL-PS6700.

DMA is supported only by emulation. That is, the CL-PS6700 will assert its PDREQ (open-drain output, register external pull-up is required) signal to issue a DMA request. This output will be connected to one of the CL-PS7111 external interrupts and can be used to interrupt the CPU so software can service the DMA request under program control.

Either of the two CL-PS6700 devices can generate an interrupt PIRQ (pull-up required on PIRQ). The PIRQ output is open-drain on the CL-PS6700. If there are two CL-PS6700, they can be wire-OR'ed to the same interrupt, which can be connected to one of the CL-PS7111 active-low external interrupt sources. On the receipt of an interrupt, the CPU can read the Interrupt Status registers on the CL-PS6700 to determine the cause of the interrupt.

All transactions are synchronous to the EXPCLK output from the CL-PS7111 (in 18.432-MHz mode) or external 13-MHz clock. The RUN signal, or a GPIO signal from CL-PS7111, can be connected to the

PSLEEP pin of the CL-PS6700, allowing them to be put into a power saving state before the CL-PS7111 enters standby mode.

NOTE: It is essential that the software monitors the appropriate status registers within the CL-PS6700 to ensure no pending posted bus transactions before standby mode is entered. Failure to do this will result in incomplete PCMCIA accesses.

3.9 DRAM Controller

The DRAM controller in the CL-PS7111 allows all connections to directly interface up to two banks of DRAM. The width of the memory interface is programmable to 16-bit or 32-bit. The two banks have to be the same width. Each bank can be up to 256 Mbytes. Two RAS lines and four CAS lines are provided, one CAS line per byte line. CAS0 enables D[7:0] in little-endian as well as big-endian modes. The DRAM device size is not programmable. Therefore, devices used that are smaller than the largest size supported (1-Gbit), lead to a segmented memory map, each bank being separated by 256 Mbytes. Segments smaller than the bank size repeat within the bank. Table 3-9 shows the mapping of physical address-to-DRAM row and column address. This mapping has been organized to support any DRAM device size from 4--Mbit to 1-Gbit with a 'square' row and column configuration (the number of column addresses equals the number of row addresses). If a non-square DRAM is used, further fragmentation of the memory map can occur, although the smallest contiguous segment is always 1-Mbyte. With proper mapping of pages and sections by the MMU, contiguous memory blocks can be created.

The DRAM controller breaks all sequential access that the minimum page sizes defined support.

Table 3-9. Physical-to-DRAM Address Mapping

Memory Address	DRAM Column ×16 mode	DRAM Column ×32 mode	DRAM Row ×16 mode	DRAM Row ×32 mode	Pin Name
0	A1[a]	A2	A9	A10	A27/DRA0
1	A2	A3	A10	A11	A26/DRA1
2	A3	A4	A11	A12	A25/DRA2
3	A4	A5	A12	A13	A24/DRA3
4	A5	A6	A13	A14	A23/DRA4
5	A6	A7	A14	A15	A22/DRA5
6	A7	A8	A15	A16	A21/DRA6
7	A8	A9	A16	A17	A20/DRA7
8	A18	A19	A17	A18	A19/DRA8
9	A20	A21	A19	A20	A18/DRA9
10	A22	A23	A21	A22	A17/DRA10
11	A24	A25	A23	A24	A16/DRA11
12	A26	A27	A25	A26	A15/DRA12

[a] This bit will be generated by the DRAM controller.

An example of the DRAM connections for a typical system can be found in Figure 3-3 on page 20.

Table 3-10 and Table 3-11 show the address mapping for various DRAMs with square and non-square row and address inputs, assuming two ×16 devices are connected to each RAS line, with 32-bit-wide DRAM operation selected. This mapping is then repeated every 256 Mbytes for each DRAM bank. *n* is derived as shown in Equation 3-1.

$$n = 0 \times C + \text{bank number} \qquad \textbf{Equation 3-1}$$

where,
0 × C for bank 0
0 × D for bank 1)

Table 3-10. DRAM Address Mapping for an External 32-Bit-Wide DRAM Memory System

Device Size	Address Configuration	Total Size of Bank	Address Range of Segment(s)	Size of Segment(s)
4 Mbits	9 Row × 9 Column	1 Mbyte	n000.0000–n00F.FFFF	1 Mbyte
16 Mbits	10 Row × 10 Column	4 Mbytes	n000.0000–n03F.FFFF	4 Mbytes
16 Mbits	12 Row × 8 Column	4 Mbytes	n000.0000– n007.FFFF n010.0000–n017.FFFF n040.0000–n047.FFFF n050.0000–n057.FFFF n100.0000–n107.FFFF n110.0000–n117.FFFF n140.0000–n147.FFFF n150.0000–n157.FFFF	512 Kbytes
64 Mbits	11 Row × 11 Column	16 Mbytes	n000.0000–n0FF.FFFF	16 Mbytes
64 Mbits	13 Row × 9 Column	16 Mbytes	n000.0000–n01F.FFFF n040.0000–n05F.FFFF n100.0000–n11F.FFFF n140.0000–n15F.FFFF n400.0000–n41F.FFFF n440.0000–n45F.FFFF n500.0000–n51F.FFFF n540.0000–n55F.FFFF	2 Mbytes
256 Mbits	12 Row × 12 Column	64 Mbytes	n000.0000–n3FF.FFFF	64 Mbytes
1 Gbit	13 Row × 13 Column	256 Mbytes	n000.0000–nFFF.FFFF	256 Mbytes

Table 3-11. DRAM Address Mapping for a 16-bit DRAM Memory System

Device Size	Address Configuration	Total Size of Bank	Address Range of Segment(s)	Size of Segment(s)
4 Mbits	9 Row × 9 Column	0.5 Mbyte	n000.0000– n007.FFFF	0.5 Mbyte
16 Mbits	10 Row × 10 Column	2 Mbytes	n000.0000–n01F.FFFF	2 Mbytes
16 Mbits	12 Row × 8 Column	2 Mbytes	n000.0000–n003.FFFF n008.0000–n00B.FFFF n020.0000–n023.FFFF n028.0000–n02B.FFFF n080.0000–n083.FFFF n088.0000–n08B.FFFF n0A0.0000–n0A3.FFFF n0A8.0000–n0AB.FFFF	256 Kbytes
64 Mbits	11 Row × 11 Column	8 Mbytes	n000.0000–n07F.FFFF	8 Mbytes
64 Mbits	13 Row × 9 Column	8 Mbytes	n000.0000–n00F.FFFF n020.0000–n02F.FFFF n080.0000–n08F.FFFF n0A0.0000–n0AF.FFFF n200.0000–n20F.FFFF n220.0000–n22F.FFFF n280.0000–n28F.FFFF n2A0.0000–n2AF.FFFF	1 Mbyte
256 Mbits	12 Row × 12 Column	32 Mbytes	n000.0000–n1FF.FFFF	32 Mbytes
1 Gbit	13 Row × 13 Column	128 Mbytes	n000.0000–n7FF.FFFF	128 Mbytes

The DRAM controller contains a programmable refresh counter. The refresh rate is controlled using DRFPR (DRAM Refresh Period register).

Sixteen- or 32-bit DRAM selection is made based on the value of SYSCON2[2]. Both banks must have the same width.

SYSCON2	0 × 8000 1100	Bit 2 (DRAMSZ)	0 = 32-bit DRAM
			1 = 16-bit DRAM

The default DRAM width is 32 bits, because SYSCON2 is reset to all zeroes at power up.

3.10 LCD Controller

The LCD controller provides all the necessary control signals to interface directly to a single-scan panel multiplexed LCD. The panel size is programmable and can be any width (line length) from 16 to 1024 pixels in 16-pixel increments. The total video frame size is programmable up to 128 Kbytes. This equates to a theoretical maximum panel size of 1024 × 256 pixels in 4-bits-per-pixel mode. The video frame buffer can be located in any portion of memory controlled by the chip select or system DRAM. Its start address will be fixed at address 0xC000.0000 within each chip select or DRAM bank. The start address of the LCD frame buffer is defined in FBADDR register [3:0]. The default start address is 0xC000 0000 (FBADRR =0x0C). A system can be built using no DRAM. One option is to use the on-chip 2-Kbyte SRAM as the LCD buffer for small panels. In this option, the LCD frame buffer start address must be set to 0x6. Programming of FBADDR is permitted only when the LCD is disabled. (This is to avoid possible cycle corruption when changing the register contents while a LCD DMA cycle is in progress.) There is no hardware protection to prevent this, so it is necessary for the software to disable the LCD controller before reprogramming FBADDR. The frame buffer start address must not be programmed to 0x4 or 0x5 if either CL-PS6700 interface is in use (PCMEN1 or 2 bits in the SYSCON2 register enabled).

NOTE: Never program FBADDR to 0x7 or 0x8 as these are the locations for the on-chip Boot ROM and internal registers.

The screen is mapped to the frame buffer as one contiguous block where each horizontal line of pixels is mapped to a set of consecutive bytes or words in the frame buffer. The frame buffer can be accessed word-wide as pixel 0 is mapped to the LSB in the buffer, the pixels arranged in a little-endian scheme.

The pixel bit rate and the LCD refresh rate can be programmed from 18432 – 576 kHz when operating in the 18.432-MHz mode, or 1300 – 203 kHz when operating from a 13-MHz clock. The LCD controller is programmed by writing to LCDCON. Programming LCDCON while the LCD controller is enabled causes the DMA address generator to be reset and a new frame to be started immediately.

The LCD controller also contains two 32-bit palette registers, allowing any 4-, 2-, or 1-bit pixel value to be mapped to any one of the available 16 grayscale values.

The required DMA bandwidth to support a half-VGA panel (640 × 240) displaying 4-bits per pixel data at an 80-Hz refresh rate is approximately 6.2 Mbytes/sec. Assuming the frame buffer is stored in DRAM, the maximum theoretical bandwidth available is 43 Mbytes/sec. at 18.432 MHz, or 29.7 Mbytes/sec. at 13 MHz. If 16-bit DRAM is used, this drops to 15 Mbytes/sec., still leaving sufficient bandwidth for other memory activity.

The LCD controller uses a 9-stage 32-bit-wide FIFO to buffer display data, which is replenished by hardware DMA under the control of the CL-PS7111 DMA controller. The LCD controller module requests new data when there are five words remaining in the FIFO, meaning for a half-VGA panel displaying 4-bitsper-pixel data at an 80-Hz refresh rate, the maximum allowable DMA latency is approximately 3.2 μs. Assuming the frame buffer is located in DRAM memory, the worst case latency is almost exactly 3.2 μs, with 13-MHz page mode cycles. If 16-bit-wide DRAM is being used, the worst case latency will double. In this case, the maximum permissible display size is halved to approximately 320 × 240 pixels, assuming the same refresh rate must be maintained.

Figure 3-6 shows the organization of the video map for all combinations of bits per pixel.

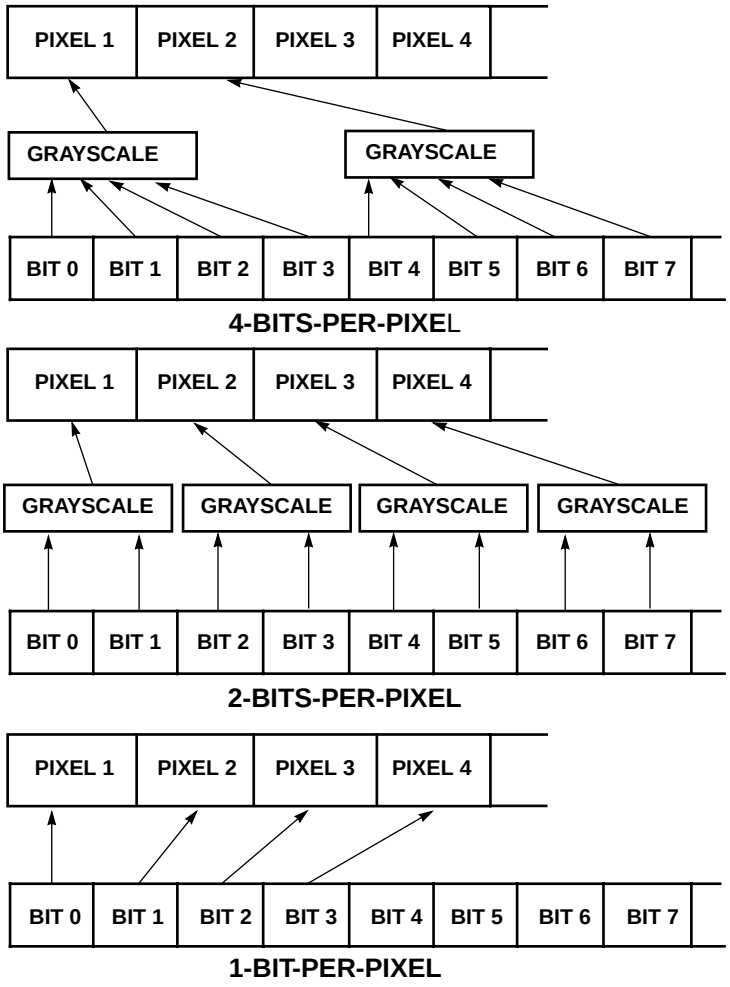


Figure 3-6. Video Buffer Mapping

The refresh rate is not affected by the number of bits per pixel. However, the LCD controller fetches twice the data per refresh for 4-bits-per-pixel compared to 2-bits-per-pixel. The main reason for reducing the number of bits per pixel is to reduce the power consumption of the memory where the video buffer is mapped.

3.11 Two Internal UARTs and SIR Encoder

The CL-PS7111 contains two built-in UART, UART1 and UART2. Both UARTs support bit rates of up to 115.2 kbps and contain two 16-byte FIFOs for receive and transmit.

UART1 supports the three modem-control input signals: CTS, DSR, and DCD. The additional RI input modem control line is not supported. Output modem control lines (such as RTS and DTR) are not explicitly supported, but can be implemented using bits from the GPIO ports in the CL-PS7111. UART2 has only receive and transmit pins.

UART operation and line speed are controlled by UBRLCR1 (UART Bit Rate and Line Control register) and two registers. Three interrupts are generated by UART1, Rx, Tx, and Modem Status Changed. Only two interrupts are generated by UART2, Rx and Tx. The Rx interrupt asserts when the FIFO becomes half full or the FIFO is non-empty longer than three character-length times and no more characters are received. The Tx interrupt asserts when the FIFO buffer reaches half empty. The Modem Status Changed interrupt for UART1 is generated when any of the modem status bits change state.

Framing and parity errors are detected as each byte is received and pushed onto the Rx FIFO. An overrun error immediately generates an Rx interrupt. All error bits can be read from the 11-bit-wide data register. The FIFO can also be programmed to be only one byte deep (such as a conventional UART with double buffering).

The CL-PS7111 also contains an IrDA SIR protocol encoder. This is a post-processing stage on the output of UART1. This encoder can be optionally switched into the Tx and Rx signals of UART1, allowing direct drive to an infrared interface. If the SIR protocol encoder is enabled, the UART Txd2 line is held in the passive state and transitions to the Modem Status Changed, or Rxd2 lines have no effect. The IrDA output pin is LEDDRV and input from the photodiode is PHDIN.

NOTE: Both UARTs operate similar to the industry standard 16C550. When the CTS deasserts on the UART, it does not stop shifting the data, relying on software to take appropriate action in response to the interrupt.

Baud rates supported for both UARTs are dependent on frequency of operation. At 18.432 MHz, the interface supports various baud rates from 115.2 kbps down. The master clock frequency is chosen so that most of the required data rates are obtainable exactly. When operating with a 13-MHz clock source, the baud rates generated have a slight error, less than or equal to 0.75%. The rates obtainable from the 13-MHz clock include 9.6, 19.2, 38, 58, and 115.2 kbps. See Table 5-4 on page 66 for available bit rates in the 13-MHz mode.

3.12 Clocks

There are two clocking options for the CL-PS7111. An on-chip oscillator and PLL provides an 18.432-MHz master bus clock frequency, using an external 3.6864-MHz crystal. Alternatively, an external 13-MHz crystal oscillator can be used.

If the 13-MHz clock option is used, connect the clock signal to the EXPCLK pin of the CL-PS7111. This mode is selected by a strapping option on the PE[2] pin. If this input is high at the rising edge of NPOR, the 13-MHz mode is selected. In this mode, EXPCLK is an input. If the external clock mode is not selected, the PLL supplies the clock during the normal mode of operation. The state of PE[2] is latched at the rising edge of the NPOR reset, and the PE[2] pin is then available for GPIO.

If the CLKENSL bit (SYSCON[25:18]) is set low, then the CLKEN/RUN pin provides the signal that starts and stops the external clock source supplied to the CL-PS7111 and the DC-DC converter. When this signal is active (high), it enables the 13-MHz clock to the CL-PS7111, and a low level disables the 13-MHz clock.

When standby mode is entered in 13-MHz mode, the 13-MHz source is gated out at the pad until it exits standby. If the CLKENSL bit is low, then the CLKEN signal will be output on the CLKEN/RUN pin and can disable an external oscillator.

If CLKENSL is set high, then standby mode is immediately exited when a wake-up event or enabled interrupt occurs. If CLKENSL is set high, then the CL-PS7111 sets CLKEN to active after an interrupt or wake-up event occurs. It then waits between 0.125 and 0.25 sec. to allow an external oscillator to stabilize before the clock is enabled through the ARM710 CPU. Only a non-masked interrupt (such as a realtime

clock match), a Port A event (corresponding to a keypress) or a wake-up asserted forces the CL-PS7111 out of standby mode. Figure 3-7 and Figure 3-8 show the CLKEN timing when CLKENSL is low.

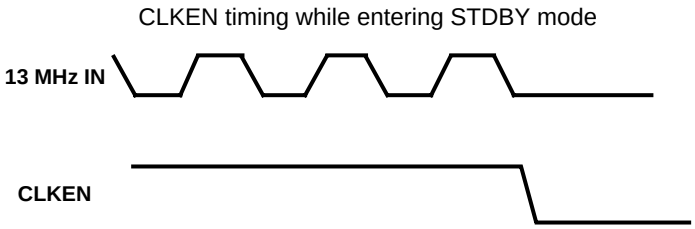


Figure 3-7. CLKEN Timing Entering Standby Mode

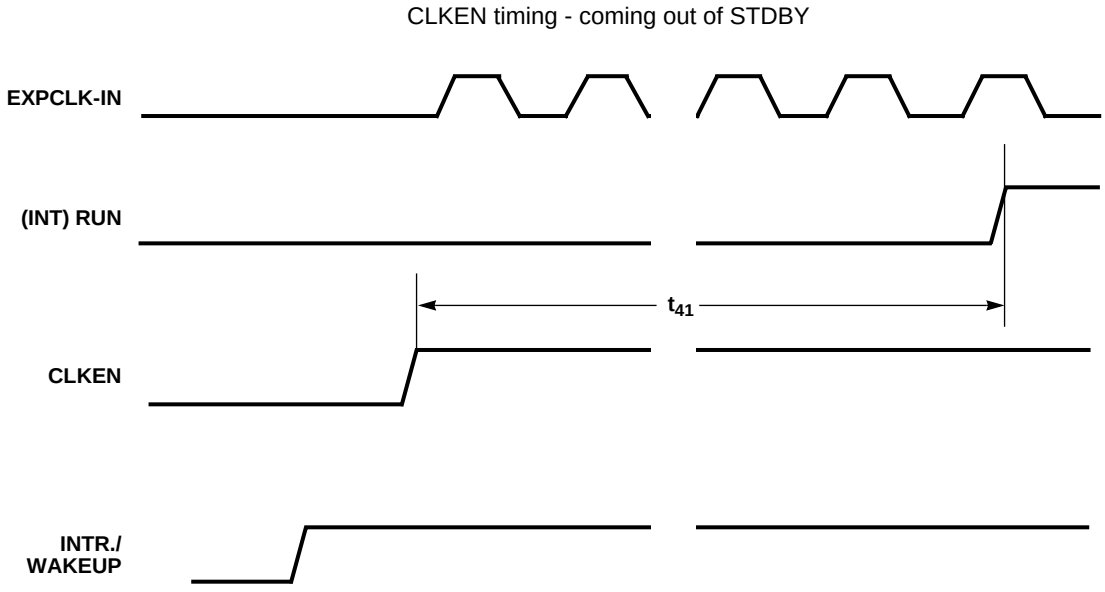


Figure 3-8. CLKEN Timing Leaving Standby Mode

3.13 Interrupt Controller

The ARM710a has two interrupt types: IRQ (interrupt request) and FIQ (fast interrupt request). The interrupt controller in the CL-PS7111 controls interrupts from 23 different sources. Nineteen interrupt sources are mapped to the IRQ input and four sources are mapped to the FIQ input. FIQs have a higher priority than IRQs: if two interrupts within the same group (IRQ or FIQ) are active, software must resolve the order in which they are serviced.

All interrupts are *level-sensitive*, that is, they must conform to the following sequence:

1) The device asserts the appropriate interrupt request line.

2) If the appropriate bit is set in the Interrupt Mask register, either FIQ or IRQ is asserted by the interrupt controller.

3) If interrupts are enabled, the processor jumps to the appropriate address.

4) Interrupt dispatch software reads the Interrupt Status register to establish the source(s) of the interrupt, and then calls the appropriate interrupt service routine(s).

5) Software in the interrupt service routine clears the interrupt source by some action specific to the device requesting the interrupt (for example, reading the UART Rx register).

6) The interrupt service routine can then re-enable interrupts. Any other pending interrupts are serviced in a similar way or returned to the interrupt dispatch code, which checks for any more pending interrupts and dispatches them accordingly.

Table 3-12 and Table 3-13 show the names and allocation of interrupts in CL-PS7111. For more information, see Section 5.12 on page 58.

Table 3-12. Interrupt Allocation in First Interrupt Register Set

Interrupt	Bit in INTMR1 and INTSR1	Name	Comment
FIQ	0	EXTFIQ	External fast interrupt input (NEXTFIQ pin).
FIQ	1	BLINT	Battery low interrupt.
FIQ	2	WEINT	Watch dog expired interrupt.
FIQ	3	MCINT	Media changed interrupt.
IRQ	4	CSINT	Codec sound interrupt.
IRQ	5	EINT1	External interrupt input 1 (NEINT1 pin).
IRQ	6	EINT2	External interrupt input 2 (NEINT2 pin).
IRQ	7	EINT3	External interrupt input 3 (EINT3 pin).
IRQ	8	TC1OI	TC1 under flow interrupt.
IRQ	9	TC2OI	TC2 under flow interrupt.
IRQ	10	RTCMI	RTC compare match interrupt.
IRQ	11	TINT	64-Hz tick interrupt.
IRQ	12	UTXINT1	Internal UART1 transmit FIFO empty interrupt.
IRQ	13	URXINT1	Internal UART1 receive FIFO full interrupt.
IRQ	14	UMSINT	Internal UART1 modem status changed interrupt.
IRQ	15	SSEOTI	Synchronous serial interface, end of transfer interrupt.

Table 3-13. Interrupt Allocation in Second Interrupt Register Set

Interrupt	Bit in INTMR2 and INTSR2	Name	Comment
IRQ	0	KBDINT	Key press interrupt
IRQ	12	UTXINT2	Internal UART2 transmit FIFO empty interrupt.
IRQ	13	URXINT2	Internal UART2 receive FIFO full interrupt.

3.13.1 Interrupt Latencies in Different States

Normal Operating States

The ARM710a macrocell checks for a low level on its FIQ/IRQ inputs at the end of each instruction. First, there is a one- or two-clock cycle synchronization penalty. For the case where the CL-PS7111 is operating at 13 MHz with a 16-bit external memory system and instruction sequence stored in one-wait-state flash memory, the worst-case interrupt latency is 251 clock cycles. This corresponds to the ARM executing an STM instruction in DRAM, and the MMU needs to fetch protection/translation information from page tables in DRAM memory. This also includes a delay for cache linefills for instruction prefetches, a data abort occurring at the end of the LDM, and the LDM being non-quad word aligned. In addition, the worst-case interrupt latency assumes that LCD DMA cycles support a panel size of 320 by 240 at 4 bits per pixel and a 60-Hz refresh rate.

This would give a worst-case interrupt latency of about 19.3 µs for the ARM710a macrocell operating at 13 MHz. For those interrupt inputs with error correction, this figure is increased by the maximum time required to pass through the deglitcher, which is approximately 60 µs (1 cycle of the 16.384-kHz clock derived from the RTC oscillator). So the absolute worst case latency is approximately 80 µs.

All the serial data transfer peripherals included in CL-PS7111 (except for the master-only SSI) have local buffering to ensure a reasonable interrupt latency response requirement for the O/S of 1 ms or less, assuming that the maximum data rates described in this specification are complied with. If the O/S cannot meet this requirement, then there will be a risk of data overflow/underflow occurring.

Idle State

When leaving idle mode as a result of an interrupt, the CPU clock is restarted after approximately two clock cycles. However, there is still potentially up to 20-µs latency as described above, unless the code is written to include at least two single cycle instructions immediately after the write to the IDLE register (in which case the latency drops to a few microseconds). This is important because idle mode will have been left as a result of a pending interrupt, which has to be synchronized by the ARM before it can be serviced.

Standby State

In standby mode, the latency time will depend on whether the system clock is shut down. If running at 18.432 MHz, then the PLL will always be shut down in standby mode in which case there will be a latency time of 0.125 to 0.25 sec. If the system is running at 13 MHz with the CLKENSL bit in SYSCON2 set to 0, then the latency will also be between 0.125 and 0.25 sec. to enable an external oscillator to stabilize. In the case of a 13-MHz system where the clock is not disabled during standby (CLKENSL = 1), then the latency will be less than 1 µs if single-cycle instructions are used after the write to the standby location.

Table 3-14 summarizes the external interrupt source latencies.

Table 3-14. External Interrupt Source Latencies

Interrupt Pin	Input State	Normal Mode Latency	Idle Mode Latency	Standby Mode Latency
NEXTFIQ	Not deglitched. Must be active for 20 µs to be detected.	Worst case latency of 20 µs.	Worst-case latency of 20 µs; if only single-cycle instructions, less than 1 µs.	Including PLL/oscillator settling time, approximately 0.25 sec. or < 1 µs if in 13-MHz mode with CLENSL set.
NEINT[1–2]	Not deglitched.	Worst case latency of 20 µs.	As above.	As above.
EINT[3]	Not deglitched.	Worst case latency of 20 µs.	As above.	As above.
MEDCHG	Deglitched by 16-kHz clock. Must be active for at least 80 µs to be detected.	Worst case latency of 80 µs.	Worst-case latency of 80 µs; if only single cycle instructions, 60 µs.	As above. Note difference if in 13-MHz mode with CLKENSL set.

For the case of the keyboard interrupt, the following options are available and are selectable according to bits 1 and 3 of the SYSCON2 register. Refer to the description of SYSCON2 in Section 5.38 on page 70 for details.

- If the KBWEN bit (SYSCON2[3]) is set low, then a keypress will cause a transition from a power saving state if the keyboard interrupt is non-masked. When KBWEN is high, a keypress will cause the device to wake up irrespective of the status of the Interrupt Mask Register.
- When the KBD6 bit (SYSCON2[1]) is low, all eight of Port A inputs are OR'ed together to produce the internal wake-up signal and keyboard interrupt request. This is the default reset state. When the KBD6 bit is high, only the lowest six bits of Port A are OR'ed together to produce the internal wake-up signal and keyboard interrupt request. The two most-significant bits of Port A are available as GPIO when this bit is set high.

If the keyboard-direct wake-up functionality is enabled (KBWEN bit is high), then the CL-PS7111 is guaranteed to exit from any power saving mode when a key is pressed, and a keyboard interrupt may be generated depending on the state of Interrupt Mask Register 2 (INTMR2[0]). If the KBWEN bit is set low then the CL-PS7111 will only wake up if INTMR2[0] is set high. In the case where KBWEN is low and the INTMR2[0] is low, it will only be possible to wake the device up using the external wake-up pin or another enabled interrupt source. The keyboard interrupt capability allows an O/S to use a polled or interrupt-driven keyboard routine, or a combination of both.

3.14 Resets

There are three asynchronous resets to the CL-PS7111: NPOR, NPWRFL, and NURESET. If any of these resets are active, a system reset is internally generated. This clears all internal registers in the CL-PS7111 to '0', except DRFPR (DRAM Refresh Period register) and RTC data and match registers, which are only cleared by an active NPOR signal. Also, FBADDR is reset to give a default frame buffer start address of 0xC000 0000. Any reset also resets the ARM710a and allows it to begin execution at the reset vector when the CL-PS7111 returns to the operating state.

Internal to the CL-PS7111, three different signals are used to reset storage elements: NPOR, NSYSRES, and NSTBY. NPOR is an external signal and NSTBY is equivalent to the external RUN signal.

NPOR (Not Power On Reset)

This is the highest-priority reset signal. When active-low, all storage elements in the CL-PS7111 are reset. NPOR active forces NSYSRES and NSTBY active. NPOR is only active when the CL-PS7111 first powers up, not during any other resets. NPOR active clears all flags in the status register, except that CLDFLG (SYSFLG1[15]) is set.

NSYSRES (Not System Reset)

NSYSRES is generated internally if NPOR, NPWRFL, or NURESET are active. NSYSRES is the second-highest-priority reset signal and asynchronously resets most internal registers in the CL-PS7111. NSYSRES active forces NSTBY and RUN low. NSYSRES resets the CL-PS7111, forcing it into the standby state with no signal from software. The ARM710a is also reset. The memory controller places all DRAMs in Self-Refresh mode, preserving the contents through a system reset. This is the reason the DRAM Refresh Period register is not cleared by a system reset.

NSTBY and RUN

The NSTBY and RUN signals are high when the CL-PS7111 is in the operating or idle states, and low when in standby state. The main system clock is valid when NSTBY is high. The NSTBY signal disables any peripheral block clocked from the master clock source (that is, everything except for the RTC).

In general, a system reset clears all registers, and NSTBY disables all peripherals that require a main clock. The following peripherals are disabled by a low level on NSTBY: two UARTs and IrDA SIR encoder, timer counters, telephony codec, and two SSIs. The following are also disabled in standby mode: LCD controller and DC-to-DC converter drive.

When operating from an external 13-MHz oscillator, which is disabled in standby mode using the CLKEN signal (that is, with CLKENSL = 0), the oscillator must be stable within 0.125 sec. from the rising edge of CLKEN signal.

3.15 Two DC-to-DC Converters

Two programmable duty ratio clock outputs are provided by the CL-PS7111. When the CL-PS7111 is operating from an 18.432-MHz master clock, these run at a frequency of 96 kHz. When in 13-MHz mode, these run at 101.6 kHz. Use these signals as drives for DC-to-DC converters in the PSU (power-supply unit) subsystem. These clocks are enabled by external input pins that are normally connected to the output from comparators monitoring the DC-to-DC converter output. The duty ratio (and the converter on-time) is programmed from 1-in-16 to 15-in-16. The sense of the DC-to-DC converter drive signal (active-high or -low) is determined by latching the state of this drive signal during power-on reset (a pull-up resistor on the drive signal results in an active-low drive output and conversely). This allows the DC-to-DC converter to generate either positive or negative voltages.

3.16 Serial Interface

The CL-PS7111 offers the serial interface options as shown in Table 3-15, in addition to the two UARTs. The codec functionality is available only in 18.432-MHz operation.

Table 3-15. Serial Interface Options

Type	Comments	Transfer Speed
Codec Interface	Designed only for use in the 18.432-MHz mode	64 kbps

The codec is enabled when SYSCON2[0] is high. On power-up, this bit is reset low so that the codec is disabled.Table 3-16 shows the pin assignments for the serial interface.

Table 3-16. Serial Interface Pin Assignments

Pin Name	Type	Codec Functionality
PCMCLK	I/O	PCMCLK serial shift clock
PCMSYNC	O	PCMSYNC output frame sync
PCMOUT	O	PCMOUT serial output data
PCMIN	I	PCMIN serial input data

3.16.1 Codec Interface

The codec interface allows a direct connection of a telephony-type codec to the CL-PS7111, providing all the necessary clocks and timing pulses and performing serialization of the data stream to/from the external codec. The interface is full-duplex and contains two separate data FIFOs (16- deep by 8-bits wide, one for receive data, another for transmit data).

Data is transferred to/from the codec at 64 kbps, either written to or read from the appropriate 16-byte FIFO. The sound interrupt is generated every 8 bytes transferred (FIFO half full/empty), which means the interrupt rate is 1 kHz with a latency of 1 ms.

NOTE: Both CDENRX and CDENTX must be enabled to receive or transmit, and upon completion of transmit the speaker amplifier should be turned off to avoid audible noise. This is required because CL-PS7111 transmits and receives data in FIFO.

3.16.2 ADC Interface — Master-Mode Only SSI (Synchronous Serial Interface)

The first synchronous serial interface allows peripheral devices (such as ADCs, that have an SPI[1] or Microwire[2] compatible interface) to be directly connected to the CL-PS7111. The clock output frequency is programmable and is only active during data transmissions to save power. There are four output frequencies available, differing slightly between 13-MHz and 18.432-MHz mode (see Table 3-17). The required frequency is selected by programming the corresponding bits (16 and 17) in the SYSCON1 register. The sample clock (SMPCLK) always runs at twice the frequency of the shift clock (ADCCLK).

Table 3-17. ADC Interface Operation Frequencies

SYSCON1[16]	SYSCON1[17]	13.0-MHz Operation ADCCLK Frequency (kHz)	18.432-MHz Operation ADCCLK Frequency (kHz)
0	0	4.2	4
0	1	16.9	16
1	0	67.7	64
1	1	135.4	128

1 SPI is a registered trademark of Motorola™.

2 Microwire™ is a registered trademark of National Semiconductor.

The output channel is fed by an 8-bit shift register, and the input channel is captured by a 16-bit shift register. The clock and synchronization pulses are activated by a write to the Output Shift register. During transfers, the SSIBUSY is set. When the transfer is complete and valid data is in the 16-bit read shift register, the SSEOTI interrupt is asserted and the SSIBUSY bit is cleared.

An additional sample clock (SMPCLK) is enabled independently and set at twice the transfer clock frequency. This interface has no local buffering capabilities and is only intended to be used with low-bandwidth interfaces (such as a touchscreen ADC interface).

4. MEMORY MAP

The lower two Gbytes of the address space is allocated to ROM and expansion. The 0.5 Gbyte of address space, 0xC000 0000–0xDFFF FFFF, is allocated to DRAM.The remaining Gbyte, minus 8K for the internal registers, is not accessible in the CL-PS7111. Program the MMU of the CL-PS7111 to generate an abort exception to access this area.

Internal peripherals addressed through a set of internal memory locations, 0x8000 0000–0x800 1FFF, are the internal registers of the CL-PS7111.

Table 4-1 shows the mapping of the 4-Gbyte address range of the ARM710a microprocessor in the CL-PS7111. Note that although 2 Kbytes of SRAM are available, the full address is decoded for the SRAM segment starting at 0x6000 0000. The mapping in Table 4-1 assumes that two CL-PS6700 PC CArd controllers are connected. If this functionality is not required, the NCS[4] and NCS[5] memory is available as general SRAM/flash/ROM/expansion space. The Boot ROM is not fully decoded; the boot code repeats within the 256-Mbyte space from 0x7000 0000–0x8000 0000. THe SRAM is fully decoded so no data is written or read from locations more than 2 Kbytes above the base address.

Table 4-1. CL-PS7111 Memory Map

Address	Contents	Size
F000.0000	Unused	256 Mbytes
E000.0000	Unused	256 Mbytes
D000.0000	DRAM Bank 1	256 Mbytes
C000.0000	DRAM Bank 0	256 Mbytes
8000.2000	Unused	~1 Gbyte
8000.0000	Internal registers	8 Kbytes
7000.0000	Boot ROM	128 bytes
6000.0000	On-chip SRAM	2 Kbytes
5000.0000	PCMCIA-1 (NCS[5])	4*64 Mbytes
4000.0000	PCMCIA-0 (NCS[4])	4*64 Mbytes
3000.0000	Expansion (NCS[3])	256 Mbytes
2000.0000	Expansion (NCS[2])	256 Mbytes
1000.0000	ROM Bank 1 (NCS[1])	256 Mbytes
0000.0000	ROM Bank 0 (NCS[0])	256 Mbytes

5. REGISTER DESCRIPTIONS

Table 5-1 shows all internal registers in the CL-PS7111, assuming the ARM710a is configured for operation with a little-endian memory system. Table 5-2 shows the differences that occur for byte accesses to ports A, B, and D with the ARM710a configured to operate in big-endian mode. All internal registers are inherently little-endian. Therefore, the system endian functionality affects the addresses required for byte accesses to internal registers. This results in a reversal of the byte address required to read or write a particular byte within a register.

There is no effect on the register addresses for word accesses. Bits A0 and A1 of the internal address bus are only decoded for ports A, B, and D (to allow reads or writes to individual ports). For all other registers, bits A0 and A1 are not decoded, so that byte reads return the whole register contents to the CL-PS7111 internal bus, from where the appropriate byte (according to the endian functionality) is read by the ARM710a. For example, to read data back as a word (irrespective of endian functionality) or a byte in little-endian mode from the DRFPR (which is only 8-bits wide) requires address 0x8000 0200. However, a byte read to obtain the register contents in big-endian mode must output address 0x8000 0203. To avoid the additional complexity, perform all internal register accesses as word operations, except for ports A to D, which are explicitly designed to operate with byte and word accesses.

8-Kbyte segments of memory in the range 8000.0000–8000.1FFF are reserved for CL-PS7111 internal use. Accesses in this range do not cause any external bus activity unless debug mode is enabled. Writes to bits that are not explicitly defined in the internal area are illegal and have no effect. Reads from bits not explicitly defined in the internal area are legal, but read undefined values. All the internal addresses are only accessed as 32-bit words, and are always on a word boundary (except for the GPIO Port registers, which can be accessed as bytes). Address bits in the range A0–A5 are not decoded (except for GPIO ports A, B, and D). This means each internal register is valid for 64 bytes (for example, the SYSFLG1 register appears at locations 8000.0140–8000.017C).

There are some gaps in the register map for backward compatibility with the CL-PS7110 device, but registers located next to a gap are still decoded only for 64 bytes. The GPIO Port registers are byte-wide, but can be accessed as a word. These registers additionally decode A0 and A1. All addresses are hexidecimal.

Table 5-1. Internal I/O Memory Locations in Little-Endian Mode

Address	Name	Default	R/W	Size	Comments	Page
8000.0000	PADR	0	RW	8	Port A Data register	47
8000.0001	PBDR	0	RW	8	Port B Data register	47
8000.0002	–		–	8	Reserved	–
8000.0003	PDDR	0	RW	8	Port D Data register	47
8000.0040	PADDR	0	RW	8	Port A Data Direction register	47
8000.0041	PBDDR	0	RW	8	Port B Data Direction register	47
8000.0042	–		–	8	Reserved	–
8000.0043	PDDDR	0	RW	8	Port D Data Direction register	47
8000.0080	PEDR	0	RW	3	Port E Data register	47

Table 5-1. Internal I/O Memory Locations in Little-Endian Mode *(cont.)*

Address	Name	Default	R/W	Size	Comments	Page
8000.00C0	PEDDR	0	RW	3	Port E Data Direction register	47
8000.0100	SYSCON1	0	RW	21	System Control register 1	48
8000.0140	SYSFLG1	0	R	32	System Status Flags register 1	50
8000.0180	MEMCFG1	0	RW	32	Expansion and ROM Memory Configuration register 1	53
8000.01C0	MEMCFG2	0	RW	32	Expansion and ROM Memory Configuration register 2	54
8000.0200	DRFPR	0	RW	8	DRAM Refresh Period register	57
8000.0240	INTSR1	0	R	32	Interrupt Status register 1	58
8000.0280	INTMR1	0	RW	32	Interrupt Mask register 1	60
8000.02C0	LCDCON	0	RW	32	LCD Control register	60
8000.0300	TC1D	0	RW	16	Read/write data to Timer Counter 1 Data register	62
8000.0340	TC2D	0	RW	16	Read/write data to Timer Counter 2 Data register	62
8000.0380	RTCDR	–	RW	32	Realtime Clock Data register	62
8000.03C0	RTCMR	–	RW	32	Realtime Clock Match register	62
8000.0400	PMPCON	0	RW	12	DC-to-DC Converter Pump Control register	63
8000.0440	CODR	0	RW	16	Codec Interface Data register	64
8000.0480	UARTDR1	0	RW	8/11	UART FIFO Data register 1	64
8000.04C0	UBRLCR1	0	RW	32	UART Bit Rate and Line Control register	65
8000.0500	SYNCIO	0	RW	16	Synchronous Serial I/O Data register only for Master SSI	67
8000.0540	PALLSW	0	RW	32	Least-significant 32-bit word of LCD Palette register	68
8000.0580	PALMSW	0	RW	32	Most-significant 32-bit word of LCD Palette register	68
8000.05C0	STFCLR	–	W	–	Write to clear all start up reason flags	69
8000.0600	BLEOI	–	W	–	Write to clear Battery Low interrupt	69
8000.0640	MCEOI	–	W	–	Write to clear Media Changed interrupt	69
8000.0680	TEOI	–	W	–	Write to clear Tick and Watchdog interrupt	69
8000.06C0	TC1EOI	–	W	–	Write to clear TC1 interrupt	69
8000.0700	TC2EOI	–	W	–	Write to clear TC2 interrupt	69
8000.0740	RTCEOI	–	W	–	Write to clear RTC Match interrupt	69
8000.0780	UMSEOI	–	W	–	Write to clear UART Modem Status Changed interrupt	69
8000.07C0	COEOI	–	W	–	Write to clear Codec Sound interrupt	69
8000.0800	HALT	–	W	–	Write to enter idle state	69
8000.0840	STDBY	–	W	–	Write to enter standby state	69

Table 5-1. Internal I/O Memory Locations in Little-Endian Mode *(cont.)*

Address	Name	Default	R/W	Size	Comments	Page
8000.0880–8000.0FFF	Reserved	–	–	–	Write has no effect; read is undefined	–
8000.1000	FRBADDR	C	RW	4	LCD Frame Buffer Start Address register	70
8000.1100	SYSCON2	0	RW	16	System Control register 2	70
8000.1140	SYSFLG2	0	R	16	System Status Flag register 2	71
8000.1240	INTSR2	0	R	24	Interrupt Status register 2	72
8000.1280	INTMR2	0	RW	16	Interrupt Mask register 2	72
8000.1480	UARTDR2	0	RW	8	UART2 Data register	64
8000.14C0	UBRLCR2	0	RW	32	UART2 Control register	65
8000.1700	KBDEOI	–	–	–	Write to clear keyboard interrupt	72
8000.1840–BFFF.FFFF	Reserved	–	–	–	This area contains test registers used during manufacturing tests. Never attempt to write to these addresses during normal operation as this can cause unexpected behavior. Reads are undefined.	–

Table 5-2. Port Byte Addresses in Big-Endian Mode

Address	Name	Default	R/W	Size	Comments
8000.0003	PADR	0	RW	8	Port A Data register
8000.0002	PBDR	0	RW	8	Port B Data register
8000.0001	–		–	8	Reserved
8000.0000	PDDR	0	RW	8	Port D Data register
8000.0043	PADDR	0	RW	8	Port A Data Direction register
8000.0042	PBDDR	0	RW	8	Port B Data Direction register
8000.0041	–		–	8	Reserved
8000.0040	PDDDR	0	RW	8	Port D Data Direction register
8000.0200	DRFPR	0	RW	8	DRAM Refresh Period register
8000.0440	CODR	0	RW	8	Codec Data I/O register
8000.0480	UARTDR1	0	RW	8	UART1 FIFO Data register
8000.1480	UARTDR2	0	RW	8	UART2 FIFO Data register

All internal registers in the CL-PS7111 are reset (cleared to ‘0’) by a system reset (NPOR, NRESET, or NPWRFL), except for DRFPR, RTCDR, and RTCMR that are only reset when NPOR becomes active. This ensures that DRAM contents and system time are preserved through a user-reset or power-fail condition.

5.1 Port A Data Register — PADR

Values written to this 8-bit read/write register are output on the Port A pins if the corresponding data direction bits are set high (port output). Values read from this register reflect the external state of Port A, not necessarily the value written to it. All bits are cleared by a system reset.

5.2 Port B Data Register — PBDR

Values written to this 8-bit read/write register are output on the Port B pins if the corresponding data direction bits are set high (port output). Values read from this register reflect the external state of Port B, not necessarily the value written to it. All bits are cleared by a system reset.

5.3 Port D Data Register — PDDR

Values written to this 8-bit read/write register are output on the Port D pins if the corresponding data direction bits are set low (port output). Values read from this register reflect the external state of Port D, not necessarily the value written to it. All bits are cleared by a system reset.

NOTE: There is no Port C on the CL-PS7111.

5.4 Port A Data Direction Register — PADDR

Bits set in this 8-bit read/write register select the corresponding pin in Port A to become an output; clearing any bit sets the pin to input. All bits are cleared by a system reset.

5.5 Port B Data Direction Register — PBDDR

Bits set in this 8-bit read/write register select the corresponding pin in Port B to become an output; clearing a bit sets the pin to input. All bits are cleared by a system reset.

5.6 Port D Data Direction Register — PDDDR

Bits cleared in this 8-bit read/write register select the corresponding pin in Port D to become an output; setting a bit sets the pin to input. All bits are cleared by a system reset so that Port D is output by default.

5.7 Port E Data Register — PEDR

Values written to this 3-bit read/write register are output on Port E pins if the corresponding data direction bits are set high (port output). Values read from this register reflect the external state of Port E, not necessarily the value written to it. All bits are cleared by a system reset.

5.8 Port E Data Direction Register — PEDDR

Bits set in this 3-bit read/write register select the corresponding pin in Port E to become an output; clearing a bit sets the pin to input. All bits are cleared by a system reset so that the default for Port E is input.

5.8.1 System Control Register 1 — SYSCON1

23	22	21	20	19	18	17	16
1	Reserved		IRTXM	WAKEDIS	EXCKEN	ADCKSEL	
15	14	13	12	11	10	9	8
SIREN	CDENRX	CDENTX	LCDEN	DBGEN	BZMOD	BZTOG	UART1EN
7	6	5	4	3	2	1	0
TC2S	TC2M	TC1S	TC1M	Keyboard Scan			

The System Control register is a 21-bit read/write register that controls the general configuration of the CL-PS7111 as well as modes for peripheral devices. All bits in this register are cleared by a system reset.

Bit **Description**

23 This bit must always be set to ‘1’.

22:21 **Reserved**

20 **IRTXM:** IrDA Tx mode bit. This bit controls the IrDA encoding strategy. Clearing this bit means each ‘0’ bit transmitted is represented as a pulse of width 3/16th of the bit rate period. Setting this bit means each ‘0’ bit is represented as a pulse of width 3/16th of the period of 115,200 bit rate clock, that is, 1.6 µs, regardless of the selected bit rate. Setting this bit reduces power consumption, but probably reduces transmission distances.

19 **WAKEDIS:** Setting this bit disables wake-up from standby mode through the WAKEUP + KBD inputs.

18 **EXCKEN:** External expansion clock enable. If this bit is set, the EXPCLK is enabled continuously; it is the same speed and phase as the CPU clock, and free-run all the time the main oscillator is running. Do not leave this bit set for power consumption reasons. If the system enters the standby state, the EXPCLK is undefined. If this bit is clear, EXPCLK is active during memory cycles only to the expansion slots that have external wait-state generation enabled.

17:16 **ADCKSEL:** Microwire®/SPI® peripheral clock speed select. This 2-bit field selects the frequency of the ADC sample clock, which is twice the frequency of the synchronous serial ADC interface clock. The following table shows the available frequencies, assuming operation at 18.432-MHz mode. The frequencies obtained at 13-MHz mode can be found on Table 3-17 on page 41.

Bit		ADC Sample Frequency (kHz) SMPCLK	ADC interface frequency (kHz) — ADCCLK
17	16		
0	0	8	4
0	1	32	16
1	0	128	64
1	1	256	128

15 **SIREN:** HP SIR protocol encoding enable. If the UART is not enabled, this bit has no effect.

Bit	Description *(cont.)*
14	**CDENRX:** Codec interface enable Rx bit. Setting this bit enables the codec interface for data reception from an external codec device. **NOTE:** Both CDENRX and CDENTX must be enabled/disabled in tandem.
13	**CDENTX:** Codec interface enable Tx bit. Setting this bit enables the codec interface for data transmission to an external codec device.
12	**LCDEN:** LCD enable bit. Setting this bit enables the LCD controller.
11	**DBGEN:** Setting this bit enables debug mode. In this mode all internal accesses are output as if they were reads or writes to expansion memory addressed by NCS5. NCS5 remains active in its standard address range. In addition, the internal interrupt request and fast interrupt request signals to the ARM710a microprocessor are output on Port E bits 1 and 2 in Debug mode. **NOTE:** These bits must be programmed as outputs before this functionality can be observed. The clock to the ARM CPU is output on Port E bit 0 in debug mode to enable individual accesses to be distinguished: NCS5 = NCS5 or internal I/O strobe PE0 = CLK PE1 = NIRQ PE2 = NFIQ
10	**BZMOD:** This bit sets the Buzzer Drive mode. 0 = the buzzer drive is connected directly to the BZTOG bit. 1 = the buzzer drive is connected to the TC1 under-flow bit.
9	**BZTOG:** Bit to directly drive buzzer.
8	**UART1EN:** Internal UART enable bit. Setting this bit enables the internal UART.
7	**TC2S:**Timer Counter 2 clock source. Setting this bit sets the TC2 clock source to 512 kHz, clearing it sets the clock source to 2 kHz (assuming an 18.432-MHz clock).
6	**TC2M:** Timer Counter 2 (TC2) mode. Setting this bit sets TC2 to Prescale mode, clearing it sets Free-running mode.
5	**TC1S:** Timer Counter 1 clock source. Setting this bit sets the TC1 clock source to 512 kHz, clearing it sets the clock source to 2 kHz (assuming an 18.432-MHz clock).
4	**TC1M:** Timer Counter 1 (TC1) mode. Setting this bit sets TC1 to Prescale mode, clearing it sets Free-running mode.

Bit Description *(cont.)*

3:0 **Keyboard Scan:** This 4-bit field that defines the state of the keyboard column drives.

Keyboard Scan	Column
0	All driven high
1	All driven low
2–7	All high impedance (tristate)
8	Column 0 only driven high, all others high impedance
9	Column 1 only driven high, all others high impedance
10	Column 2 only driven high, all others high impedance
11	Column 3 only driven high, all others high impedance
12	Column 4 only driven high, all others high impedance
13	Column 5 only driven high, all others high impedance
14	Column 6 only driven high, all others high impedance
15	Column 7 only driven high, all others high impedance

5.9 System Status Flags Register 1 — SYSFLG1

31	30	29	28	27	26	25	24
VERID		ID	BOOTBIT1	BOOTBIT0	SSIBUSY	CTXFF	CRXFE
23	22	21	20	19	18	17	16
UTXFF1	URXFE1	RTCDIV					
15	14	13	12	11	10	9	8
CLDFLG	PFFLG	RSTFLG	NBFLG	UBUSY1	DCD	DSR	CTS
7	6	5	4	3	2	1	0
DID				WUON	WUDR	DCDET	MCDR

The System Status Flags register 1 is a 32-bit read-only register that indicates various system information.

Bit Description

31:30 **VERID:** Version ID bits. These two bits determine the version identification for the CL-PS7111. Reads ‘0’ for the first version.

29 **ID:** Always reads ‘1’ for the CL-PS7111. Always reads ‘0’ for the CL-PS7110.

Bit **Description** *(cont.)*

28:27 **BOOTBIT0–1:** These bits indicate the default (power-on reset) bus width of the ROM interface. See the Memory Configuration registers on page 53 for more details on the ROM interface bus width. The state of these bits reflects the state of Port E bits 0–1 during power-on reset, as shown in the following table:

PE1 (BOOTBIT1)	PE0 (BOOTBIT0)	Boot Option
0	0	32 bit
0	1	8 bit
1	0	16 bit
1	1	Reserved

26 **SSIBUSY:** Synchronous serial interface busy. This bit is set while data is shofted in or out of the seynchronous serial interface. When this bit is clear, data is valid for reads.

25 **CTXFF:** Codec Tx FIFO full bit. This is set if the 16-byte codec Tx FIFO is full.

24 **CRXFE:** Codec Rx FIFO empty bit. This is set if the 16-byte codec Rx FIFO is empty.

23 **UTXFF1:** UART1 transmit FIFO full. The meaning of this bit depends on the state of the UFIFOEN bit in the UART1 Bit Rate and Line Control register. If the FIFO is disabled, this bit is set when the Tx Holding register is full. If the FIFO is enabled, the UTXFF1 bit is set when the Tx FIFO is full.

22 **URXFE1:** UART1 receiver FIFO empty. The meaning of this bit depends on the state of the UFIFOEN bit in the UART1 Bit Rate and Line Control register. If the FIFO is disabled, this bit is set when the Rx Holding register is empty. If the FIFO is enabled the URXFE bit is set when the Rx FIFO is empty.

21:16 **RTCDIV:** This 6-bit field reflects the number of 64-Hz ticks that have passed since the last increment of the RTC. It is the output of the divide-by-64 chain that divides the 64-Hz tick clock down to 1 Hz for the RTC. The MSB is the 32-Hz output; the LSB is the 1-Hz output.

15 **CLDFLG:** Cold start flag. This bit is set if the CL-PS7111 has been reset with a power on reset; it is cleared by writing to the STFCLR location.

14 **PFFLG:** Power fail flag. This bit is set if the system has been reset by the power fail input pin, it is cleared by writing to the STFCLR location.

13 **RSTFLG:** Reset flag. This bit is set if the RESET button is pressed, forcing the NURESET input low. It is cleared by writing to the STFCLR location.

12 **NBFLG:** New battery flag. This bit is set if a low-to-high transition has occurred on the NBATCHG input; it is cleared by writing to the STFCLR location.

11 **UBUSY1:** UART1 transmitter busy. This bit is set while the UART1 is busy transmitting data; it is guaranteed to remain set until the complete byte has been sent, including all stop bits.

10 **DCD:** This bit reflects the current status of the data carrier detect (DCD) modem-control input to the UART1.

9 **DSR:** This bit reflects the current status of the data set ready (DSR) modem-control input to the UART1.

8 **CTS:** This bit reflects the current status of the clear to send (CTS) modem-control input to the UART1.

Bit	Description *(cont.)*
7:4	**DID:** Display ID nibble. This 4-bit nibble reflects the latched state of the four LCD data lines. The state of the four LCD data lines is latched by the LCDEN bit and always reflect the last state of these lines before the LCD controller was enabled. These bits identify the LCD display panel.
3	**WUON:** This bit is set if the system is brought out of standby by a rising edge on the WAKEUP signal. This bit is cleared by a system reset or by writing to the HALT or STDBY locations.
2	**WUDR:** Wake-up direct read. This bit reflects the non-latched state of the WAKEUP signal.
1	**DCDET:** This bit is set if the main adapter is powering the system (the inverted state of the NDCDET input pin).
0	**MCDR:** Media changed direct read. This bit reflects the non-latched status of the media changed input.

5.10 Memory Configuration Register 1 — MEMCFG1

31:24	*23:16*	*15:8*	*7:0*
NCS3 configuration	NCS2 configuration	NCS1 configuration	NCS0 configuration

Expansion and ROM space is selected by one of eight chip selects. One chip select (CS6) is used internally for the on-chip SRAM, and the configuration is hardwired for 32-bit wide, minimum-wait state operation. CS7 is used for the on-chip Boot ROM, and the configuration field is hardwired for 8-bit wide, minimum-wait state operation. Data written to the configuration fields for either CS6 or CS7 are ignored. Two of the chip selects (NCS4 and NCS5) can be used to access two CL-PS6700 PCMCIA controller devices, and when either of these interfaces is enabled, the configuration field for the appropriate chip select in the MEMCFG2 register is ignored. When the PCMCIA1 or 2 control bit in the SYSCON2 register is disabled, then NCS4 and NCS5 are active as normal and can be programmed using the relevant fields of MEMCFG2, as for the other four chip selects. All of the six external chip selects are active for 256 Mbytes, and the timing and bus transfer width can be programmed individually. This is accomplished by programming the width fields contained in two 32-bit registers, MEMCFG1 and MEMCFG2. All bits in these registers are cleared by a system reset (except for the CS6 and CS7).

The Memory Configuration register 1 is a 32-bit read/write register that sets the configuration of the four expansion and ROM selects NCS0–3. Each select is configured with a 1-byte field, starting with expansion select 0.

5.10.1 Memory Configuration Register 2 — MEMCFG2

31:24	23:16	15:8	7:0
(Boot ROM, CS7)	(Local SRAM, CS6)	NCS5 configuration	NCS4 configuration

The Memory Configuration Register 2 is a 32-bit read/write register that sets the configuration of the two expansion and ROM selects NCS4–5. Each select is configured with a 1-byte field, starting with expansion select 4.

Each of the six non-reserved byte fields for chip-select configuration in the Memory Configuration registers are identical and define the number of wait states, the bus width, enable EXPCLK output during accesses and enable sequential mode access. This arrangement applies to NCS0–3, and to NCS4–5 when the PCMCIA enable bits in the SYSCON2 register are not set. The state of these bits is ignored for the Boot ROM and local SRAM fields in the MEMCFG2 register. This byte field is defined as follows:

7	6	5:4	3:2	1:0
CLKEN	SQAEN	Sequential access wait state	Random access wait state	Bus width

NOTE: IF PCMCIA is enabled, the CS4/CS5 settings in this register are ignored.

The memory area decoded by CS6 is reserved for the 2 Kbytes of on-chip SRAM and does not require a configuration field in MEMCFG2. It is automatically set up for 32 bits and no wait state. For the Boot ROM, it is automatically set up for 8 bits and no wait state.

Chip selects NCS4 and NCS5 are used to select two CL-PS6700 PCMCIA controller devices. These have a multiplexed 16-bit wide address/data interface, and the configuration bytes in the MEMCFG2 register have no meaning when these interfaces are enabled.

Bit	Description
7	**CLKENB:** Expansion clock enable. Setting this bit enables the EXPCLK to be active during accesses to the selected expansion device. This provides a timing reference for devices that need to extend bus cycles using the EXPRDY input. Back-to-back (but not necessarily Page mode) accesses result in a continuous clock. This bit only affects EXPCLK when the PLL is being used, that is, in 18.432-MHz mode. When operating in 13-MHz mode, the EXPCLK pin is an input, so it cannot be affected by this register bit. To save power internally, EXPCLK should always be set to '0' when operating in 13-MHz mode.
6	**SQAEN:** Sequential access enable. Setting this bit enables sequential accesses that are on a quad-word boundary to take advantage of faster access times from devices that support Page mode. The sequential access is faulted after four words, (to allow video refresh cycles to occur), even if the access is part of a longer sequential access. In addition, when this bit is not set, all non-sequential accesses have a single idle cycle inserted between them so that the chip select is deasserted between each access for easier debug.

Bit Description *(cont.)*

5:4 **Sequential Access Wait State:**

Bit		No. of Wait States
5	**4**	
0	0	3
0	1	2
1	0	1
1	1	0

3:2 **Random Access Wait State:**

Bit		No. of Wait States
3	**2**	
0	0	4
0	1	3
1	0	2
1	1	1

Bit Description *(cont.)*

1:0 **Bus Width:** The effect of this field is dependent on the two BOOTBIT bits, which can be read in the SYSFLG register. All bits in the Memory Configuration register are cleared by a system reset, and the state of the BOOTBIT bits is determined by Port E bits 0 and 1 on the CL-PS7111 during power-on reset. The state of PE1 and PE0 determine whether the CL-PS7111 is going to boot from either 32-, 16-, or 8-bit-wide ROMs.

See Chapter 6, "ELECTRICAL SPECIFICATIONS" for more details on bus timing.

Bit		BOOTBIT1	BOOTBIT0	Expansion Transfer Mode	Port E Bits 1 and 0 During NPOR Reset
1	0				
0	0	0	0	32-bit-wide bus access	Low, Low
0	1	0	0	16-bit-wide bus access	Low, Low
1	0	0	0	8-bit-wide bus access	Low, Low
1	1	0	0	Reserved	Low, Low
0	0	0	1	8-bit-wide bus access	Low, High
0	1	0	1	Reserved	Low, High
1	0	0	1	32-bit-wide bus access	Low, High
1	1	0	1	16-bit-wide bus access	Low, High
0	0	1	0	16-bit-wide bus access	High, Low
0	1	1	0	32-bit-wide bus access	High, Low
1	0	1	0	Reserved	High, Low
1	1	1	0	8-bit-wide bus access	High, Low

5.11 DRAM Refresh Period Register — DRFPR

7	6	5	4	3	2	1	0
RFSHEN	RFDIV						

The DRAM Refresh Period register is an 8-bit read/write register that enables refresh and selects the refresh period used by the DRAM controller for its periodic CAS-before-RAS refresh. The value in the DRAM refresh period register is *only* cleared by a power on reset, that is, the register state is maintained during a power fail or user reset.

Bit	Description
7	**RFSHEN:** DRAM refresh enable. Setting this bit enables periodic refresh cycles to be generated by the CL-PS7111 at a rate set by the RFDIV field. Setting this bit also enables Self-refresh mode when the CL-PS7111 is in the standby state.
6:0	**RFDIV:** This 7-bit field sets the DRAM refresh rate. The refresh period is derived from a 128-kHz clock as shown in Equation 5-1. Frequency (kHz) = 128/(RFDIV + 1), that is, RFDIV = (128/Refresh frequency (kHz)) – 1 **Equation 5-1** This equation is valid for both 13-MHz and 18-MHz modes. The equation for frequency gives the refresh rate for the DRAM. The maximum refresh frequency is 64 kHz, the minimum is 1 kHz. The RFDIV field should not be programmed with '0' as this results in no refresh cycles being initiated. These values are valid for both 13-MHz and 18-MHz modes of operation.

5.12 Interrupt Status Register 1 — INTSR1

15	14	13	12	11	10	9	8
SSEOTI	UMSINT	URXINT1	UTXINT	TINT	RTCMI	TC2OI	TC1OI
7	6	5	4	3	2	1	0
EINT3	EINT2	EINT1	CSINT	MCINT	WEINT	BLINT	EXTFIQ

The Interrupt Status register is a 32-bit read-only register. This register reflects the current state of the first 16 interrupt sources within the CL-PS7111. Each bit is set if the appropriate interrupt is active. The following describes the interrupt assignments.

Bit	Description
15	**SSEOTI:** Synchronous serial interface end-of-transfer interrupt. This interrupt is active after a complete data transfer to and from the external ADC has completed. It is cleared by reading the ADC data from the SYNCIO register.
14	**UMSINT:** Internal UART1 modem status changed interrupt. This interrupt is active if either of the two modem status lines (CTS or DSR) change state. It is cleared by writing to the UMSEOI location.
13	**URXINT:** Internal UART1 receive FIFO half-full interrupt. The function of this interrupt source depends on whether the UART1 FIFO is enabled. If the FIFO is disabled this interrupt is active when there is valid Rx data in the UART1 Rx Data Holding register, and is cleared by reading this data. If the FIFO is enabled this interrupt is active when the UART1 Rx FIFO is half or more full or if the FIFO is non empty and no more characters are received for a 3-character time-out period. It is cleared by reading all the data from the Rx FIFO.
12	**UTXINT1:** Internal UART1 transmit FIFO half-empty interrupt. The function of this interrupt source depends on whether the UART1 FIFO is enabled. If the FIFO is disabled (FIFOEN bit is clear in the UART1 Bit Rate and Line Control register), this interrupt is active when there is no data in the UART1 Tx Data Holding register, and cleared by writing to the UART1 Data register. If the FIFO is enabled this interrupt is active when the UART1 Tx FIFO is half or more empty, and is cleared by filling the FIFO to at least half full.
11	**TINT:** 64-Hz tick interrupt. This interrupt becomes active on every rising edge of the internal 64-Hz clock signal. This 64-Hz clock is derived from the 15-stage ripple counter that divides the 32.768-kHz oscillator input down to 1 Hz for the realtime clock. This interrupt is cleared by writing to the TEOI location.
10	**RTCMI:** RTC compare match interrupt. This interrupt becomes active on the **next** rising edge of the 1-Hz realtime clock (one second later) after the 32-bit time written to the realtime clock match register exactly matches the current time in the RTC. It is cleared by writing to the RTCEOI location.
9	**TC2OI:** TC2 under-flow interrupt. This interrupt becomes active on the **next** falling edge of the timer counter 2 clock after the timer counter has under-flowed (reached ‘0’). It is cleared by writing to the TC2EOI location.
8	**TC1OI:** TC1 under-flow interrupt. This interrupt becomes active on the **next** falling edge of the timer counter 1 clock after the timer counter has under-flowed (reached ‘0’). It is cleared by writing to the TC1EOI location.
7	**EINT3:** External interrupt input 3. This interrupt is active if the EINT3 input is active (high) it is cleared by returning EINT3 to the passive (low) state.
6	**EINT2:** External interrupt input 2. This interrupt is active if the NEINT2 input is active (low). It is cleared by returning NEINT2 to the passive (high) state.
5	**EINT1:** External interrupt input 1. This interrupt is active if the NEINT1 input is active (low). It is cleared by returning NEINT1 to the passive (high) state.

Bit	Description *(cont.)*
4	**CSINT:** Codec sound interrupt. This interrupt is active if the codec interface is enabled and the codec data FIFO has reached half full or empty (depending on the interface direction). It is cleared by writing to the COEOI location.
3	**MCINT:** Media changed interrupt. This interrupt is active after a rising edge on the NMEDCHG input pin has been detected, This input is deglitched with a 16-kHz clock and only generates an interrupt if it is active for longer than 62.5 ms. It is mapped to the FIQ input on the ARM710a microprocessor and is cleared by writing to the MCEOI location.
2	**WEINT:** Watchdog expired interrupt. This interrupt is active on a rising edge of the periodic 64-Hz tick interrupt clock if the tick interrupt is still active, that is, if a tick interrupt has not been serviced for a complete tick period. It is cleared by writing to the TEOI location. **NOTE:** Watchdog timer is turned off during STANDBY modes. Watchdog cannot be accessed or cleared by software.
1	**BLINT:** Battery low interrupt. This interrupt is active if no external supply is present (NEXTPWR is high), and the battery-OK input pin BATOK is forced low. This interrupt is deglitched with a 16-kHz clock so it only generates an interrupt if it is active for longer than 62.5 ms. It is mapped to the FIQ input on the ARM7 processor and is cleared by writing to the BLEOI location.
0	**EXTFIQ:** External fast interrupt. This interrupt is active if the NEXTFIQ input pin is forced low and is mapped to the FIQ input on the ARM7 processor.

5.13 Interrupt Mask Register 1 — INTMR1

15	14	13	12	11	10	9	8
SSEOTI	UMSINT	URXINT	UTXINT	TINT	RTCMI	TC2OI	TC1OI
7	6	5	4	3	2	1	0
EINT3	EINT2	EINT1	CSINT	MCINT	WEINT	BLINT	EXTFIQ

The Interrupt Mask register 1 is a 32-bit read/write register used to selectively enable the 16 interrupt sources within the CL-PS7111. The four shaded cells in the previous table are interrupts that generate a fast interrupt request to the ARM7 processor (FIQ), causing a jump to the processor virtual address 0000.0001C. All other interrupts generate a standard interrupt request; this causes a jump to processor virtual address 0000.00018. See Table 3-12 on page 37 for the interrupt allocation. Setting the appropriate bit in this register enables the corresponding interrupt. All bits are cleared by a system reset.

5.14 LCD Control Register — LCDCON

31	30	29:25	24:19	18:13	12:0
GSMD	GSEN	AC prescale	Pixel prescale	Line length	Video buffer size

The LCD Control register is a 32-bit read/write that controls the size of the LCD screen and the operating mode of the LCD controller operates in. Refer to Section 3.10 on page 33 for more information on video buffer mapping and the LCD controller.

NOTE: The LCDCON register should only be reprogrammed when the LCD controller is disabled.

Bit	Description
31	**GSMD:** Grayscale mode bit. Clearing this bit sets the controller to 2-bits per pixel (4 grayscales). Setting sets the controller to 4-bits per pixel (15 grayscales).
30	**GSEN:** Grayscale enable bit. Setting this bit enables grayscale output to the LCD. When this bit is cleared, each bit in the video map directly corresponds to a pixel in the display.
29:25	**AC Prescale:** The AC prescale field is a 5-bit number that sets LCD AC bias frequency. This frequency is the required AC bias frequency for a given manufacturer's LCD plate. This frequency is derived from the frequency of the line clock (CL1). The 'M' signal toggles after n+1 counts of the line clock (CL1) where n is the number programmed into the AC prescale field. This number must be chosen to match the manufacturer's recommendation (normally 13), but must not be exactly divisible by the number of lines in the display.

Bit **Description** *(cont.)*

24:19 **Pixel Prescale:** The pixel prescale field is a 6-bit field that sets the pixel rate prescale. The pixel rate is derived from a 36.864-MHz clock and is calculated with Equation 5-2.

$$\text{Pixel rate (MHz)} = 36.864 \div (\text{pixel prescale} + 1) \quad \textbf{Equation 5-2}$$

The pixel rate should be chosen to give a complete screen refresh frequency of approximately 70 Hz to avoid flicker. Frequencies above 70 Hz should be avoided as they consume additional power. The pixel prescale value can be expressed in terms of the LCD size by using Equation 5-3.

$$\text{Pixel prescale} = (526628 \div \text{Total pixels in display}) - 1 \quad \textbf{Equation 5-3}$$

The value should be rounded down to the nearest whole number. '0' is illegal and results in no pixel clock.

For example:

$$\text{A } 640 \times 240 \text{ LCD, pixel prescale} = 526628 \div (640 \times 240) - 1 = 2.428\ (2) \quad \textbf{Equation 5-4}$$

Equation 5-4 gives an actual pixel rate of 36.864E6 ÷ 2 + 1 = 12.288 MHz, which gives an actual refresh frequency of 12.288E6 ÷ (640 × 240) = 80 Hz.

NOTE: As the CL2 low pulse time is doubled after every CL1 high pulse (see Figure 6-8 on page 86), this refresh frequency is only an approximation; the accurate formula is shown in Equation 5-5.

$$12.288E6 \div ((640 \times 240) + 120) = 79.937 \text{ Hz.} \quad \textbf{Equation 5-5}$$

18:13 **Line Length:** The line length field is a 6-bit field that sets the number of pixels in one complete line. This field is calculated with Equation 5-6.

$$\text{Line length} = (\text{No. pixels in line} \div 16) - 1 \quad \textbf{Equation 5-6}$$

For example, for 640 × 240 LCD Line length = (640 ÷ 16) – 1 = 39 or 0x27 h.

NOTE: The minimum value that can be programmed into this register is '1' (that is, '0' is not a legal value).

12:0 **Video Buffer Size:** The video buffer size field is a 13-bit field that sets the total number of bits × 128 (quad words) in the video display buffer. This is calculated with Equation 5-7.

$$\text{Video buffer size} = (\text{Total bits in video buffer} / 128) - 1 \quad \textbf{Equation 5-7}$$

For example, for a 640 × 240 LCD and 4 bits per pixel the size of the video buffer = 640 × 240 × 4 = 614400 bits

$$\text{Video buffer size field} = (614400 \div 128) - 1 = 4799 \text{ or } 0x12BF \text{ h.} \quad \textbf{Equation 5-8}$$

5.15 Timer Counter 1 Data Register — TC1D

The Timer Counter 1 Data register is a 16-bit read/write register that sets and reads data to TC1. Any value written is decremented on the next rising edge of the clock.

5.16 Timer Counter 2 Data Register — TC2D

The Timer Counter 2 Data register is a 16-bit read/write register that sets and reads data to TC2. Any value written is decremented on the next rising edge of the clock.

5.17 Realtime Clock Data Register — RTCDR

The Realtime Clock Data register is a 32-bit read/write register that sets and reads the binary time in the RTC. Any value written is incremented on the next rising edge of the 1-Hz clock. All bits in the Realtime Clock Data register are only cleared by an active NPOR. This register is reset only by NPOR.

5.18 Realtime Clock Match Register — RTCMR

The Realtime Clock Match register is a 32-bit read/write register that sets and reads the binary match time to RTC. Any value written is compared to the current binary time in the RTC, if they match it asserts the RTCMI interrupt source. This register is reset only by NPOR.

5.19 Pump Control Register — PMPCON

11:8	*7:4*	*3:0*
Drive 1 pump ratio	Drive 0 from mains ratio	Drive 0 from battery ratio

The DC-to-DC Converter Pump Control register is a 12-bit read/write-only register that sets and controls the variable mark space ratio drives for two DC-to-DC converters. All bits in this register are cleared by a system reset.

Bit **Description**

3:0 **Drive 0 from Battery:** This 4-bit field controls the on time for the drive 0 DC-to-DC pump while the system is powered from batteries. Setting these bits to '0' disables this pump, setting these bits to '1' allows the pump to be driven in a 1:16 duty ratio, 2 in a 2:16 duty ratio, etc., up to a 15:16 duty ratio. An 8:16 duty ratio results in a square wave of 96 kHz when operating with an 18.432-MHz master clock, or 101.6 kHz when operating from the 13-MHz source. The NEXTPWR input is used to switch between the two on times for 'drive0'.

7:4 **Drive 0 from Mains:** This 4-bit field controls the on time for the drive 0 DC-to-DC pump while the system is powered from mains. Setting these bits to '0' disables this pump; setting these bits to '1' allows the pump to be driven in a 1:16 duty ratio, 2 in a 2:16 duty ratio, etc., up to a 15:16 duty ratio. An 8:16 duty ratio results in a square wave of 96 kHz when operating with an 18.432-MHz master clock, or 101.6 kHz when operating from the 13-MHz source. The NEXTPWR input switches between the two on times for 'drive 0'.

11:8 **Drive 1 Pump Ratio:** This 4-bit field controls the on time for the drive 1 DC-to-DC pump. Setting these bits to '0' disables this pump, setting these bits to '1' allows the pump to be driven in a 1:16 duty ratio, 2 in a 2:16 duty ratio, etc., up to a 15:16 duty ratio. An 8:16 duty ratio results in a square wave of 96 kHz when operating with an 18.432-MHz master clock, or 101.6 kHz when operating from the 13-MHz source.

The state of the output drive pins is latched during power-on reset, this latched value is used to determine the polarity of the drive output. The sense of the DC-to-DC converter control lines is summarized in the following table.

Initial State of Drive 'n' during POR	Sense of Drive 'n'	Polarity of Bias Voltage
Low	Active high	+VE
High	Active low	-VE

5.20 Codec Interface Data Register — CODR

The CODR register is a 16-bit read/write register, which is used with the codec interface when this is selected by the appropriate setting of SYSCON2[0] (SERSEL). Data written to or read from this register is pushed or popped onto the appropriate 16-byte FIFO buffer. Data from this buffer is then serialized and sent to or received from the codec sound device. When the CODEC is enabled, the codec interrupt CSINT is generated repetitively at 1/8th of the byte transfer rate and the state of the FIFOs can be read in the System Flags register. The net data transfer rate to/from the codec device is 8 Kbytes per second giving an interrupt rate of 1 kHz.

5.21 UART Data Registers — UARTDR1–2

10	*9*	*8*	*7:0*
OVERR	PARERR	FRMERR	Rx data

The UARTDR registers are an 11-bit read and 8-bit write register for all data transfers to or from the internal UARTs 1 and 2.

Data written to this register is pushed onto the 16-byte data Tx holding FIFO if the FIFO is enabled; if not, it is stored in a 1-byte holding register. This write initiates transmission from the UART.

The UART Data Read register comprises the 8-bit data byte received from the UART together with three bits of error status. Data read from this register is popped from the 16-byte data Rx FIFO if the FIFO is enabled, if not it is read from a 1-byte buffer register containing the last byte received by the UART. Data received and error status is automatically pushed onto the Rx FIFO if it is enabled. The Rx FIFO is 10 bits wide by 16 deep.

Bit	Description
10	**PARERR:** UART parity error. This bit is set if the UART detected a parity error while receiving the data byte.
9	**OVERR:** UART overrun error. This bit is set if more data is received by the UART and the FIFO is full. The Overrun Error bit is not associated with any single character and so is not stored in the FIFO, if this bit is set, the entire contents of the FIFO is invalid and should be cleared. This error bit is cleared by reading the UARTDR register.
8	**FRMERR:** UART framing error. This bit is set if the UART detected a framing error while receiving the associated data byte. Framing errors are caused by non-matching word lengths or bit rates.
7:0	**Rx Data:** This 8-bit field contains the receive data.

5.22 UART Bit Rate and Line Control Registers — UBRLCR1–2

31:19	*18:17*	*16*	*15*	*14*	*13*	*12*	*11:0*
Reserved	WRDLEN	FIFOEN	XSTOP	EVENPRT	PRTEN	BREAK	Bit rate divisor

The UART Bit Rate and Line Control registers are 19-bit read/write registers. A write to these registers sets the bit rate and mode of operation for the internal UARTs.

Bit **Description**

31:19 **Reserved**

18:17 **WRDLEN:** This 2-bit field selects the word length as shown in the following table.

Bit		Word Length
18	**17**	
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

16 **FIFOEN:** Set to enable FIFO buffering of Rx and Tx data. Clear to disable the FIFO, that is, set its depth to one byte.

15 **XSTOP:** Extra stop bit. Setting this bit causes the UART to transmit two stop bits after each data byte, clearing it transmits one stop bit after each data byte.

14 **EVENPRT:** Even parity bit. Setting this bit sets parity generation and checking to even parity, clearing it sets odd parity. This bit has no effect if the PRTEN bit is clear.

13 **PRTEN:** Parity enable bit. Setting this bit enables parity detection and generation.

12 **BREAK:** Setting this bit drives the Tx output active (high) to generate a break.

Bit Description *(cont.)*

11:0 **Bit Rate Divisor:** This 12-bit field set the bit rate. If the system is operating with an 18.432-MHz master clock, then the bit rate divider is fed by a clock frequency of 3.6864 MHz, which is then further divided internally by 16 to give the bit rate. The formula to give the divisor value for any bit rate when operating from the 18.432-MHz clock is:

$$\text{Divisor} = (230400 \div \text{bit rate}) - 1 \qquad \textbf{Equation 5-9}$$

A value of '0' in this field is illegal when in the 18.432-MHz mode. In 13-MHz mode, the clock frequency fed to the UART is 1.8571 MHz. In this mode, '0' is a legal divisor value and generates the maximum possible bit rate. The following tables show example bit rates with the corresponding divisor value.

Table 5-3. UART Bit Rates at 18.432-MHz Clock Rate

Divisor Value	Bit Rate at 18.432 MHz
0	—
1	115200
2	76800
3	57600
5	38400
11	19200
15	14400
23	9600
95	2400
191	1200
2094	110

Table 5-4. UART Bit Rates at 13-MHz Clock Rate

Divisor Value	Bit Rate at 13 MHz	Error on 13-MHz value
0	116071	0.75%
1	58036	0.75%
2	38690	0.75%
5	19345	0.75%
7	14509	0.75%
11	9673	0.75%
47	2418	0.42%
96	1196	0.28%
1054	110.02	0.18%

5.23 Synchronous Serial ADC Interface Data Register — SYNCIO

24:15	*14*	*13*	*12:8*	*7:0*
Reserved	TXFRMEN	SMCKEN	Frame length	ADC Configuration byte

SYNCIO is a 16-bit read/write register. The data written to the SYNCIO register configures the SSI, and the least-significant byte is serialized and transmitted out of the synchronous serial interface to configure an external ADC, bit D7 (the MSB) first. The transfer clock automatically starts at the programmed frequency, and a synchronization pulse is issued. The ADCIN pin is sampled on every clock edge, and the result is shifted in to the SYNCIO read register.

During data transfer the SSIBUSY bit is set high, at the end of a transfer the SSEOTI interrupt is asserted. This interrupt is cleared by reading the SYNCIO register. The data read from the SYNCIO register is the *last* sixteen bits shifted out of the ADC. The length of the data frame can be programmed by writing to the SYNCIO register, this allows many different ADCs to be accommodated. The bits in the SYNCIO register are defined as follows.

Bit	Description
24:15	**Reserved**
14	**TXFRMEN:** Setting this bit causes an ADC data transfer to be initiated; the value in the ADC configuration field is shifted out to the ADC, and depending on the frame length programmed, a number of bits is captured from the ADC. If the SYNCIO register is written to with the TXFRMEN bit low, no ADC transfer occurs, but the Frame length and SMCKEN bits are affected.
13	**SMCKEN:** Setting this bit enables a free-running sample clock at the programmed ADC clock frequency to be output on the SMPLCK pin.
12:8	**Frame Length:** The 5-bit Frame length field is the total number of shift clocks required to complete a data transfer. For many ADCs this is 25, 8 for configuration byte + 1 null bit + 16 bits.
7:0	**ADC Configuration:** 8-bit configuration data to be sent to the ADC.

5.24 Least-Significant Word-LCD Palette Register — PALLSW

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Grayscale value for pixel value 7	Grayscale value for pixel value 6	Grayscale value for pixel value 5	Grayscale value for pixel value 4	Grayscale value for pixel value 3	Grayscale value for pixel value 2	Grayscale value for pixel value 1	Grayscale value for pixel value 0

The least- and most-significant Word-LCD Palette registers make up a 64-bit read/write register, which maps the logical pixel value to a physical grayscale level. The 64-bit register is made up of 16 × 4-bit nibbles, each nibble defines the grayscale level associated with the appropriate pixel value. If the LCD controller is operating in two bits per pixel, only the lower four nibbles are valid (D[15:0] in the least-significant word). Similarly, one bit per pixel means only the lower two nibbles are valid (D[7:0] in the least-significant word). The pixel-to-grayscale level assignments are shown in the respective bit description table.

5.25 Most-Significant Word-LCD Palette Register — PALMSW

Refer to the description of PALLSW.

31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
Grayscale value for pixel value 15	Grayscale value for pixel value 14	Grayscale value for pixel value 13	Grayscale value for pixel value 12	Grayscale value for pixel value 11	Grayscale value for pixel value 10	Grayscale value for pixel value 9	Grayscale value for pixel value 8

The actual physical color and pixel duty ratio for the grayscale values are shown in Table 5-5. Note that colors 8–15 are the inverse of colors 7–0 respectively; this means that colors 7 and 8 are identical. The steps in the grayscale are nonlinear. but have been chosen to give a close approximation to perceived linear grayscales. The is due to the eye being more sensitive to changes in gray level close to 50% gray.

Table 5-5. Grayscale Value-to-Color Mapping

Grayscale Value	Duty Cycle	% Pixels Lit	% Step Change
0	0	0%	11.1%
1	1/9	11.1%	8.9%
2	1/5	20.0%	6.7%
3	4/15	26.7%	6.6%
4	3/9	33.3%	6.7%
5	2/5	40.0%	5.4%
6	4/9	44.4%	5.6%
7	1/2	50.0%	0.0%

Table 5-5. Grayscale Value-to-Color Mapping *(cont.)*

Grayscale Value	Duty Cycle	% Pixels Lit	% Step Change
8	1/2	50.0%	5.6%
9	5/9	55.6%	5.4%
10	3/5	60.0%	6.7%
11	6/9	66.7%	6.6%
12	11/15	73.3%	6.7%
13	4/5	80.0%	8.9%
14	8/9	88.9%	11.1%
15	1	100%	–

5.26 Clear All Start Up Reason Flags Location — STFCLR

A write to this location clears all the start-up reason flags in the System Flags Status register (SYSFLG).

5.27 Battery Low End-of-Interrupt — BLEOI

A write to this location clears the interrupt generated by a low battery (falling BATOK with NEXTPWR high).

5.28 Media Changed End-of-Interrupt — MCEOI

A write to this location clears the interrupt generated by a rising edge of the NMEDCHG input pin.

5.29 Tick End-of-Interrupt Location — TEOI

A write to this location clears the current pending tick interrupt and watchdog interrupt.

5.30 End--of-Interrupt Location — TC1EOI TC1

A write to this location clears the under-flow interrupt generated by TC1.

5.31 End-of-Interrupt Location — TC2EOI TC2

A write to this location clears the under-flow interrupt generated by TC2.

5.32 RTC Match End-of-Interrupt — RTCEOI

A write to this location clears the RTC match interrupt.

5.33 UART1 Modem Status Changed End-of-Interrupt — UMSEOI

A write to this location clears the modem status changed interrupt.

5.34 Codec End-of-Interrupt Location — COEOI

A write to this location clears the sound interrupt (CSINT).

5.35 Enter Idle State Location — HALT

A write to this location places the system into the *idle* state by halting the clock to the processor until an interrupt is generated. A write to this location while there is an active interrupt has no effect.

5.36 Enter Standby State Location — STDBY

A write to this location places the system into the *standby* state by halting the main oscillator. It automatically switches the DRAMs to self-refresh if the RFSHEN bit is set in the DRAM Refresh Period register. All transitions to the *standby* state are synchronized with DRAM cycles. A write to this location while there is an active interrupt has no effect.

5.37 LCD Frame Buffer Start Address — FRBADDR

This register contains the start address for the LCD Frame Buffer. (It is assumed that the frame buffer starts at location 0x0000000 within each chip-select memory region; therefore the value stored within the FRBADDR is only the value of the chip select where the frame buffer is located.) On reset, this is set to 0xC for backward compatibility with CL-PS7110. The register is 4 bits wide. This register must only be reprogrammed while the LCD is disabled (that is, setting low the LCDEN bit within SYSCON2).

5.38 System Control Register 2 — SYSCON2

15	14	13	12	11	10	9	8
Reserved	BUZFREQ	CLKENSL	OSTB	Reserved	Reserved	Reserved	UART2EN
7	6	5	4	3	2	1	0
Reserved	PCMCIA2	PCMCIA1	Reserved	KBWEN	DRAMSZ	KBD6	CODECEN

This register is an extension of SYSCON1, containing control bits for the features which are new for CL-PS7111. The bits of the second system control register are defined as shown in the above bit description table.

Bit	Description
15	**Reserved**
14	**BUZFREQ:** BUZ output select. When low, the buzzer signal generated from the on-chip timer is output. When high, a fixed-frequency clock is output (500 Hz in 18.432-MHz mode and 528 Hz in 13-MHz mode).
13	**CLKENSL:** Clock enable select. When low, the CLKEN signal is output on the RUN/CLKEN pin. When high, the run signal is output on RUN/CLKEN.
12	**OSTB:** This operating system timing bit is for use only with the 13-MHz operating mode. Normally it is set low; however, when set high it causes a 500-kHz clock to be generated for the timers instead of the 541-kHz one that would normally be available. The divider to generate this frequency is not clocked when this bit is set low.
11:9	**Reserved**
8	**UART2EN:** Internal UART2 enable bit. Setting this bit enables the internal UART2.
7	**Reserved**
6	**PCMCIA2:** Enables the interface to the CL-PS6700 device for PCMCIA slot 2. The main effect of this bit is to reassign the functionality of Port B bit 1 to the PRDY input from the CL-PS6700 devices, and to ensure that any access to the NCS4 address space is according to the CL-PS6700 interface protocol.
5	**PCMCIA1:** Enables the interface to the CL-PS6700 device for PCMCIA slot 1. The main effect of this bit is to reassign the functionality of Port B bit 0 to the PRDY input from the CL-PS6700 devices, and to ensure that any access to the NCS4 address space is according to the CL-PS6700 interface protocol.
4	**Reserved**
3	**KBWEN:** When set high, this bit enables the functionality that allows the CL-PS7111 to wake up from a power saving state into the operating state from Port A, irrespective of the status of the Interrupt Mask register.

Bit	Description *(cont.)*
2	**DRAMSZ:** Determines width of DRAM memory interface, where 0 = 32-bit DRAM bank; 1 = 16-bit DRAM bank
1	**KBD6:** The state of this bit determines how many Port A inputs are OR'ed together to create the keyboard interrupt (and the internal WAKEUP signal if this functionality is enabled by the KBWEN bit). When '0' (the reset state), all 8 Port A inputs generate a keyboard interrupt. When set high, only Port A bits 0 to 5 generate an interrupt from the keyboard. It is assumed that the keyboard row lines are connected into Port A.
0	**CODECEN:** This bit must always be set to '1'.

5.39 System Status Flags Register 2 — SYSFLG2

23	*22*	*21*	*20*	*19*	*18*	*17*	*16*
UTXFF2	URXFE2	Reserved					
15	*14*	*13*	*12*	*11*	*10*	*9*	*8*
Reserved				UBUSY2	Reserved		
7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
Reserved	CKMODE	Reserved					

This register is an extension of SYSFLG1, containing status bits for the features new to the CL-PS7111.

Bit	Description
23	**UTXFF2:** UART2 transmit FIFO full. The meaning of this bit depends on the state of the UFIFOEN bit in the UART2 bit rate and line control register. If the FIFO is disabled, this bit is set when the Tx holding register is full. If the FIFO is enabled, the UTXFF bit is set when the Tx FIFO is full.
22	**URXFE2:** UART2 receiver FIFO empty. The meaning of this bit depends on the state of the UFIFOEN bit in the UART2 bit rate and line control register. If the FIFO is disabled, this bit is set when the Rx holding register contains is empty. If the FIFO is enabled the URXFE bit is set when the Rx FIFO is empty.
21:12	**Reserved**
11	**UBUSY2:** UART2 transmitter busy. This bit is set while UART2 is busy transmitting data. It is guaranteed to remain set until the complete byte has been sent, including all stop bits.
10:7	**Reserved**
6	**CKMODE:** This bit reflects the status of the CLKSEL (Port E bit 2) input, latched during NPOR. When low, the PLL is running and the chip is operating in 18.432-MHz mode. When high, the chip is operating from an external 13-MHz clock.
5:0	**Reserved**

5.40 Interrupt Status Register 2 — INTSR2

15	14	13	12	11	10	9	8
Reserved		URXINT2	UTXINT2	Reserved			

7	6	5	4	3	2	1	0
Reserved							KBDINT

This register is an extension of INTSR1, containing status bits for the features that are new to CL-PS7111. The interrupt status register reflects the current state of the new interrupt sources within CL-PS7111. Each bit is set if the appropriate interrupt is active.

Bit	Description
15:14	**Reserved**
13	**URXINT2:** UART2 receive FIFO half-full interrupt. The function of this interrupt source depends on whether the UART2 FIFO is enabled. If the FIFO is disabled, this interrupt is active when there is valid Rx data in the UART2 Rx Data Holding register and is cleared by reading this data. If the FIFO is enabled, this interrupt is active when the UART2 Rx FIFO is half or more full, or if the FIFO is non empty and no more characters are received for a 3-character time-out period. It is cleared by reading all the data from the Rx FIFO.
12	**UTXINT2:** UART2 transmit FIFO half-empty interrupt. The function of this interrupt source depends on whether the UART2 FIFO is enabled. If the FIFO is disabled (FIFOEN bit is clear in the UART2 Bit Rate and Line Control register), this interrupt is active when there is no data in the UART2 Tx Data Holding register, and is cleared by writing to the UART2 Data register. If the FIFO is enabled, this interrupt is active when the UART2 Tx FIFO is half or more empty and is cleared by filling the FIFO to at least half full.
11:1	**Reserved**
0	**KBDINT:** Keyboard interrupt. This interrupt is generated whenever a key is pressed, from the logical OR of the first 6 or all 8 of the Port A inputs (depending on the state of the KBD6 bit in the SYSCON2 register). The interrupt request is latched and can be deasserted by writing to the KBDEOI location.

5.41 Interrupt Mask Register 2 — INTMR2

15	14	13	12	11	10	9	8
Reserved		URXINT2	UTXINT2	Reserved			

7	6	5	4	3	2	1	0
Reserved							KBDINT

This register is an extension of INTMR1, containing interrupt mask bits for the features which are new for CL-PS7111. Refer to INTSR2 for individual bit details.

5.42 Keyboard End-of-Interrupt Location — KBDEOI

A write to this location clears the KBDINT keyboard interrupt.

6. ELECTRICAL SPECIFICATIONS

Operating Voltage Range

2.7 V (± 5%) at 13.0 MHz

3.3 V (± 10%) at 18.432 MHz

Operating Temperature Range

13 MHz	Commercial temperature range	0°C to +70°C
18.432 MHz	Commercial temperature range	0°C to +70°C

6.1 Absolute Maximum Ratings

DC supply voltage	–0.5 volts to +6 volts
DC input/output voltage	–0.5 volts to VDD + 0.5 volts
DC input current	± 20 mA
Storage temperature	–40°C to +125°C
Lead temperature	+300°C

6.2 Recommended Operating Conditions

DC supply voltage	+2.55 volts to +3.6 volts
DC input/output voltage	0 to VDD
DC input current	± 15 mA
Operating temperature	0°C to +70°C

6.3 DC Characteristics

All characteristics are specified at VDD = 2.7 V (± 5%) at 13.0 MHz or 3.3 V (± 10%) at 18.432 MHz, and VSS = 0 V over an operating temperature of 0°C to +70°C. The current consumption figures relate to typical conditions at 3.3 V, 18.432-MHz operation with the PLL switched on.

Symbol	Parameter	MIN	MAX	Units	Conditions
VIH	CMOS input high voltage	0.7 × VDD	VDD + 0.3	V	
VIL	CMOS input low voltage	–0.3	0.2 × VDD	V	
VT+	Schmitt trigger positive going threshold	1.52	2.26	V	
VT-	Schmitt trigger negative going threshold	0.72	1.29	V	
VHST	Schmitt trigger hysteresis	0.64	1.13	V	VIL to VIH
VOH	CMOS output high voltage Output drive 1 and 2 Output drive 3 and 4	 VDD – 0.1 VDD – 1.0 VDD – 1.0		 V V V	 IOH = 0.8 mA IOH = 3 mA IOH = 12 mA
VOL	CMOS output low voltage Output drive 1 and 2 Output drive 3 and 4		 0.1 0.5 0.5	 V V V	 IOL = -0.8 mA IOL = -3 mA IOL = -12 mA
IIN	Input leakage current	–10	+10	µA	VIN = VDD or GND
IOZ	Output tristate leakage current[a]	–10	+10	µA	VOUT = VDD or GND
CIN	Input capacitance		5	pF	
COUT	Output capacitance		5	pF	
CI/O	Transceiver capacitance		5	pF	
$IDD_{startup}$	Start-up current consumption		50	µA	Initial 100 ms from power up, 32-kHz oscillator not stable, POR signal at VIL, all other I/O static, VIH = VDD ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{standby}$	Standby current consumption		20	µA	Just 32-kHz oscillator running, all other I/O static, VIH = VDD ± 0.1 V, VIL = GND ± 0.1 V
IDD_{idle}	Idle current consumption		6	mA	Both oscillators running, CPU static, LCD refresh active, VIH = VDD ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{operating}$	Operating current consumption		40	mA	All system active, running typical program
$VDD_{standby}$	Standby supply voltage	2.2		V	Minimum standby voltage for state retention and RTC operation only

[a] Assumes buffer has no pull-up or pull-down resistors.

6.4 AC Characteristics

All characteristics are specified at VDD = 2.7 to 3.6 volts and VSS = 0 V over an operating temperature of 0°C to +70°C. Parameters marked with an asterisk (*) are not fully tested. Characteristics marked with a pound sign (#) are significantly different for 13-MHz mode because the EXPCLK is provided as an input rather than generated internally. These timings are estimated at present.

Symbol	Parameter	13 MHz		18.432 MHz		Units
		MIN	MAX	MIN	MAX	
t_1	Falling CS to data bus High-Z	0*	35*	0*	25*	ns
t_2	Address change to valid write data	0	45	0	35	ns
t_3	DATA in to falling EXPCLK setup time	0#	–	18	–	ns
t_4	DATA in to falling EXPCLK hold time	10#	–	0	–	ns
t_5	EXPRDY to falling EXPCLK setup time	0#	–	18	–	ns
t_6	Falling EXPCLK to EXPRDY hold time	10#	50#	0	50	ns
t_7	Rising NMWE to data invalid hold time	10	–	5	–	ns
t_8	Sequential data valid to falling NMWE setup time	–10	10	–10	10	ns
t_9	Row address to falling NRAS setup time	5	–	5	–	ns
t_{10}	Falling NRAS to row address hold time	25	–	25	–	ns
t_{11}	Column address to falling NCAS setup time	2	–	2	–	ns
t_{12}	Falling NCAS to column address hold time	25	–	25	–	ns
t_{13}	Write data valid to falling NCAS setup time	2	–	2	–	ns
t_{14}	Write data valid from falling NCAS hold time	50	–	50	–	ns
t_{15}	LCD CL2 low time	80	3,475	80	3,475	ns
t_{16}	LCD CL2 high time	80	3,475	80	3,475	ns
t_{17}	LCD Rising CL2 to rising CL1 delay	0	25	0	25	ns
t_{18}	LCD Falling CL1 to rising CL2	80	3,475	80	3,475	ns
t_{19}	LCD CL1 high time	80	3,475	80	3,475	ns
t_{20}	LCD Falling CL1 to falling CL2	200	6,950	200	6,950	ns
t_{21}	LCD Falling CL1 to FRM toggle	300	10,425	300	10,425	ns
t_{22}	LCD Falling CL1 to M toggle	–10	20	–10	20	ns
t_{23}	LCD Rising CL2 to display data change	–10	20	–10	20	ns
t_{24}	Falling EXPCLK to address valid	–	33#	–	5	ns
t_{25}	Data valid to falling NMWE for non sequential access only	5	–	5	–	ns
t_{41}	CLKN rising to (internal) RUN active, clock must be on stable	1				ms

Symbol	Parameter	13 MHz		18.432 MHz		Units
		MIN	MAX	MIN	MAX	
t_{42}	CLKN rising to (internal) RUN active, clock must be on stable			0.125		s
t_{NCSRD}	Negative strobe (NCS0–5) zero wait state read access time	120		70		ns
t_{NCSWR}	Negative strobe (NCS0–5) zero wait state write access time	120		70		ns
t_{EXBST}	Sequential expansion burst mode read access time	55		35		ns
t_{RC}	DRAM cycle time	230	–	150	–	ns
t_{RAC}	Access time from RAS	110	–	70	–	ns
t_{RP}	RAS precharge time	110	–	70	–	ns
t_{CAS}	CAS pulse width	30	–	20	–	ns
t_{CP}	CAS precharge in Page mode	20	–	12	–	ns
t_{PC}	Page mode cycle time	70	–	45	–	ns
t_{CSR}	CAS set-up time for auto refresh	20	–	15	–	ns
t_{RAS}	RAS pulse width	110	–	80 *	–	ns

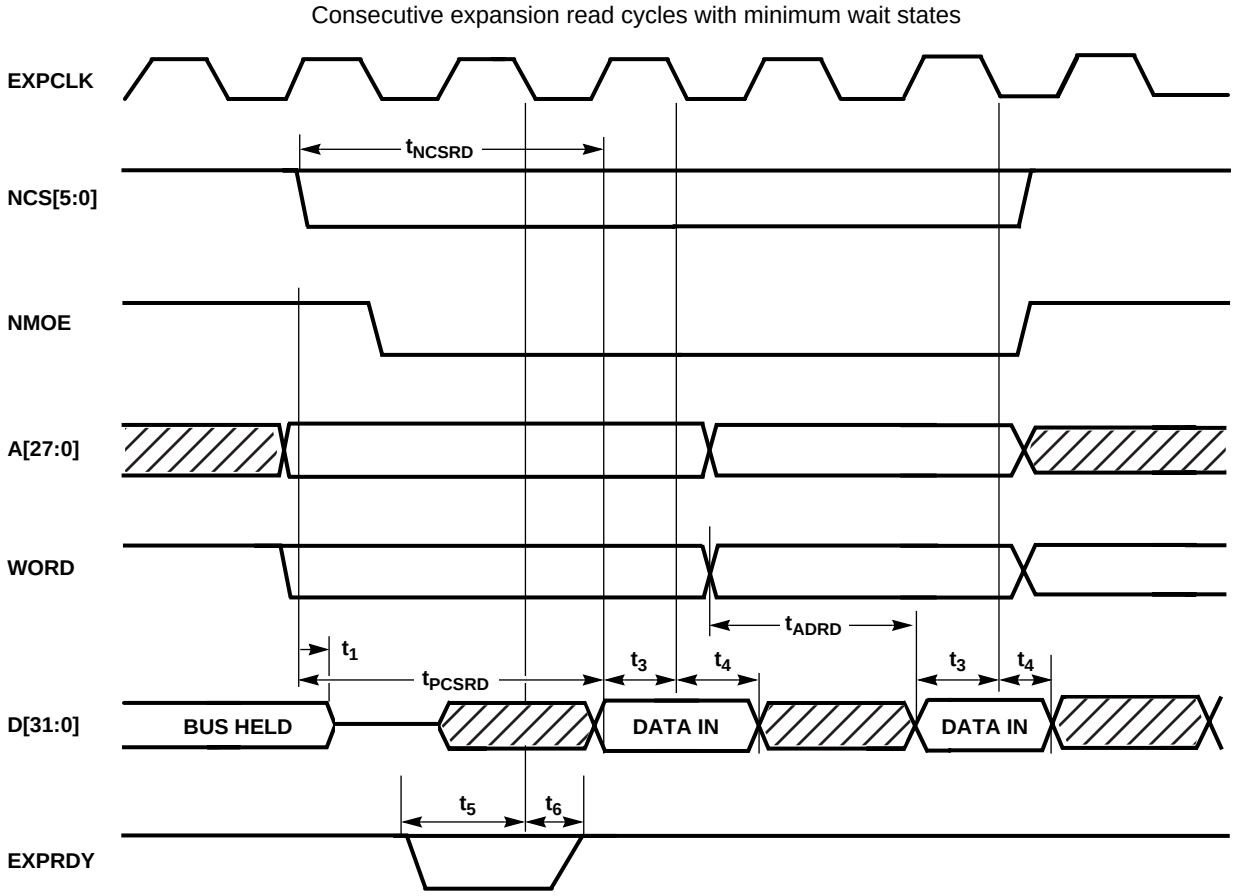


Figure 6-1. Expansion and ROM Read Timing

NOTES:

1) t_{EXRD} = maximum 70 ns and 120 ns for minimum wait states and a main oscillator frequency of 18.432 MHz and 13.0 MHz respectively. This time can be extended by integer multiples of the clock period (54 ns), by either driving EXPRDY low and or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer; if low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY but is shown for clarity.

2) Consecutive reads with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states, and no idle cycles are inserted between successive non sequential ROM/expansion cycles. This improves performance, so the SQAEN should always be set where possible.

Sequential page mode read cycles with minimum wait states

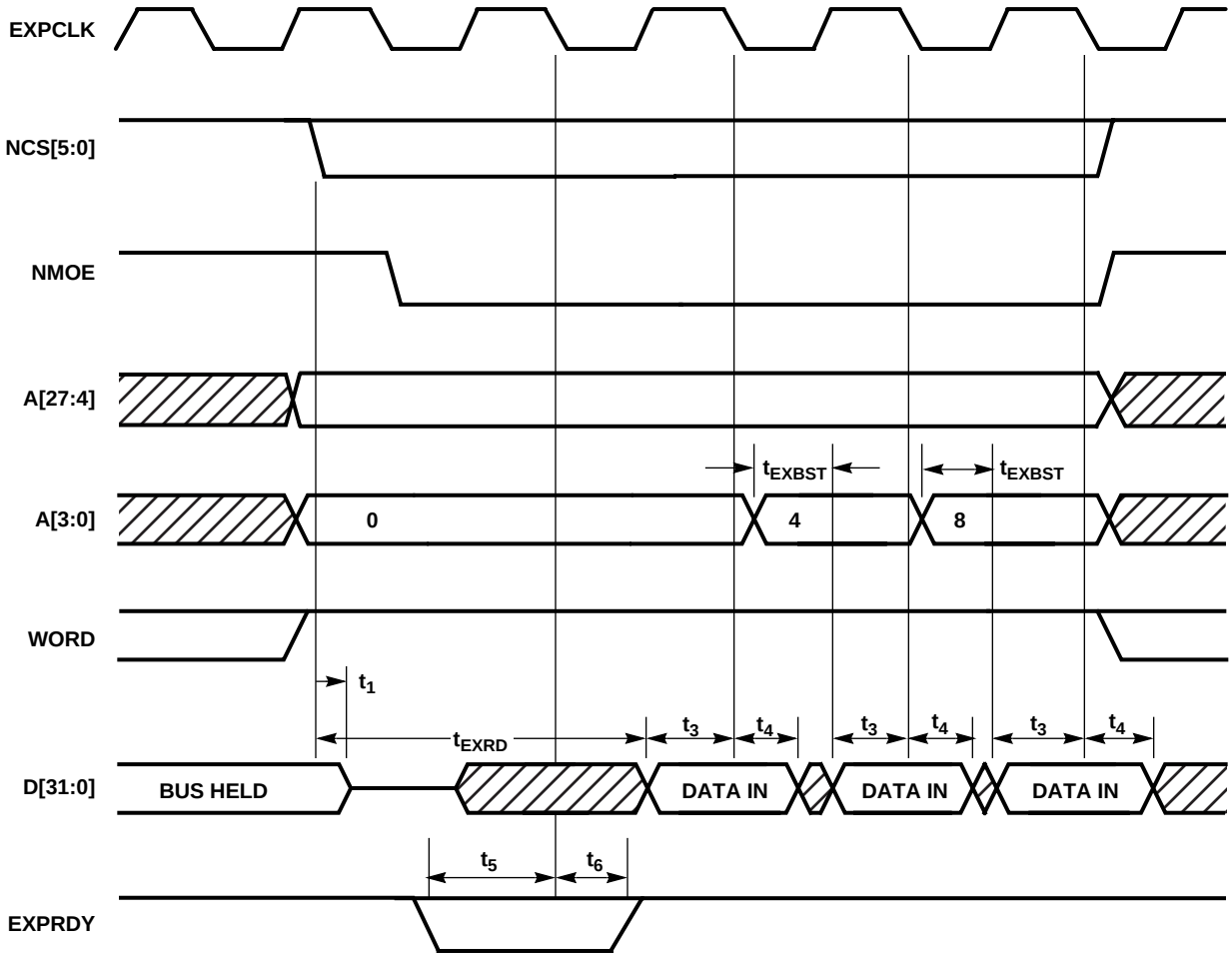


Figure 6-2. Expansion and ROM Sequential Read Timing

NOTES:

1) t_{EXBST} = 35 ns at 18.432 MHz and 55 ns maximum at 13.0 MHz for zero wait state page mode access. This time can be extended by integer multiples of the clock period by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer, if low at this point the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY but is shown for clarity.

2) Consecutive reads with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states, and no idle cycles are inserted between successive non sequential ROM/expansion cycles. This improves performance, so the SQAEN should always be set where possible.

Consecutive expansion write cycles with minimum wait states

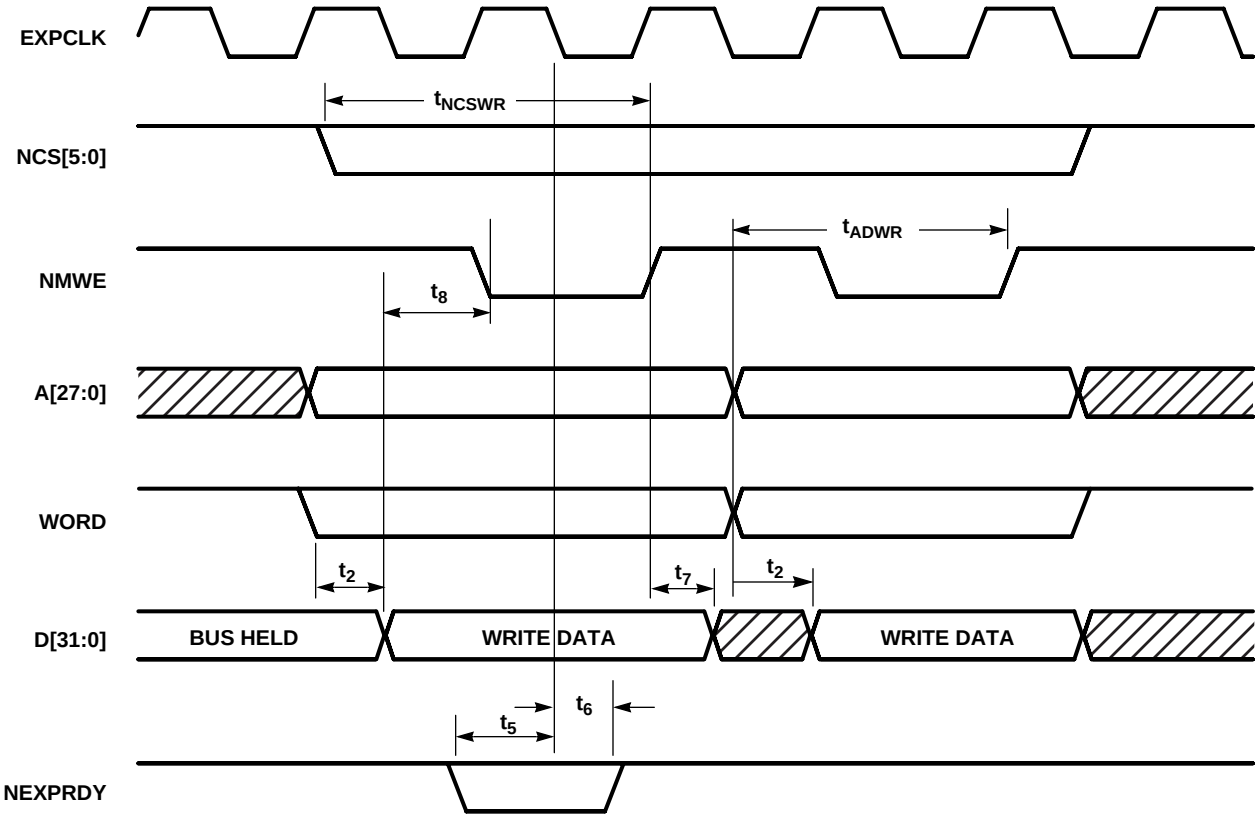


Figure 6-3. Expansion and ROM Write Timing

NOTES:

1) t_{EXWRT} = MAX 70 ns at 18.432 MHz and 120 ns at 13.0 MHz for minimum wait states. This time can be extended by integer multiples of the clock period (54 ns at 18.432 MHz and 77 ns at 13.0 MHz) by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer; if low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY but is shown for clarity.

2) Consecutive writes with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states. No idle cycles are inserted between sequential and non sequential accesses. In addition, the write data set-up time to falling NMWE (T8) cannot be guaranteed to be positive in this case; for I/O devices where this would cause a problem, the SQAEN bit should not be set.

DRAM word read followed by page mode read (MCLK shown for reference only)

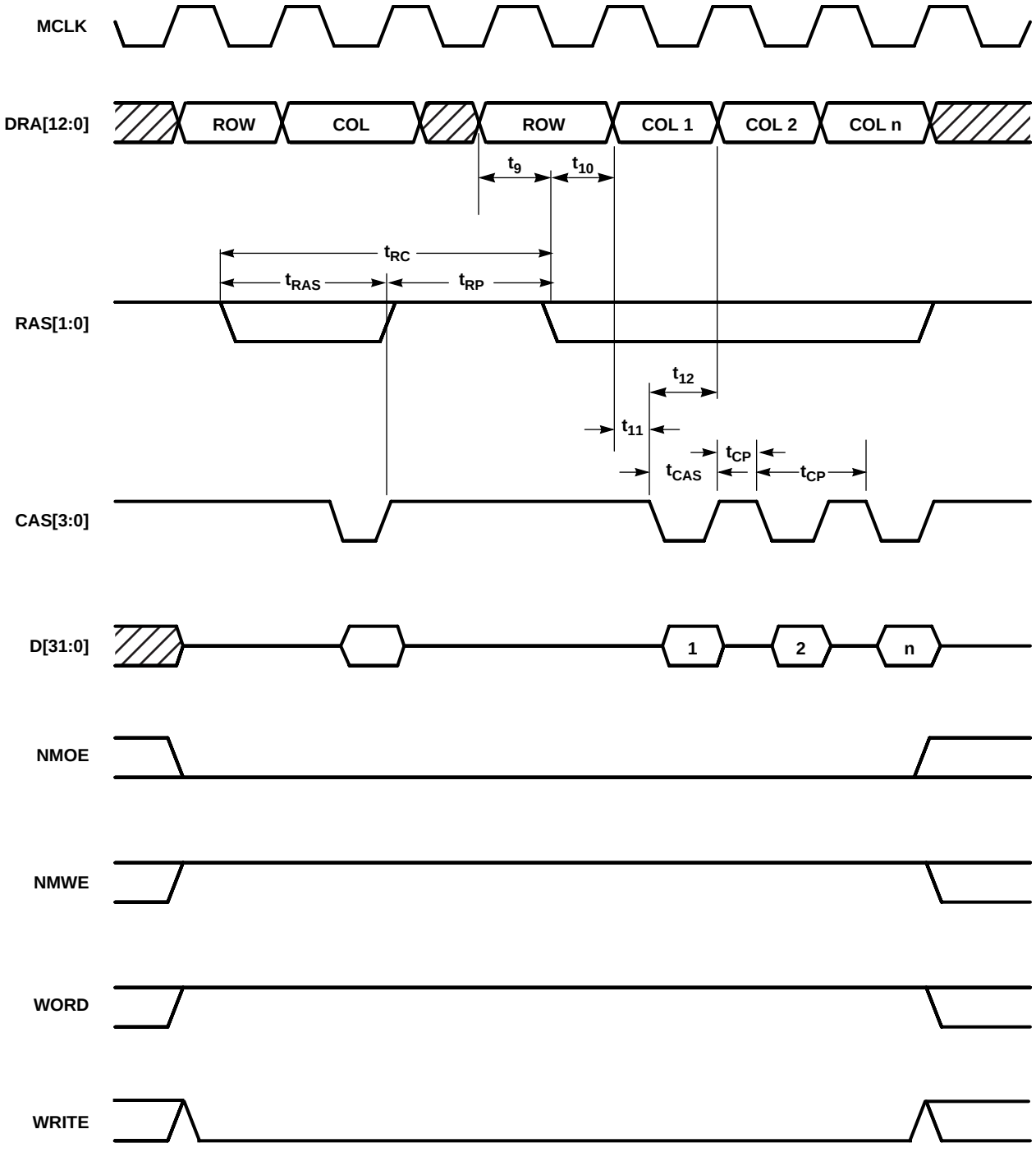


Figure 6-4. DRAM Read Cycles

NOTES:

1) t_{RC} (read cycle time) = 150 ns maximum at 18.432 MHz and 230 ns at 13.0 MHz

2) t_{RAC} (access time from RAS) = 80 ns maximum at 18.432 MHz and 110 ns at 13.0 MHz

3) t_{RP} (RAS precharge time) = 70 ns maximum at 18.432 MHz and 110 ns at 13.0 MHz

4) t_{CAS} (CAS pulse width) = 20 ns maximum at 18.432 MHz and 30 ns at 13.0 MHz

5) t_{CP} (CAS precharge in Page mode) = 12 ns maximum at 18.432 MHz and 20 ns at 13.0 MHz

6) t_{PC} (Page mode cycle time) = 45 ns minimum at maximum at 18.432 MHz and 70 ns at 13.0 MHz

7) Word reads shown, for byte reads only one of CAS[3:0] is active, CAS0 for byte 0, etc.

Word write followed by sequential word write to DRAM (MCLK shown for reference only)

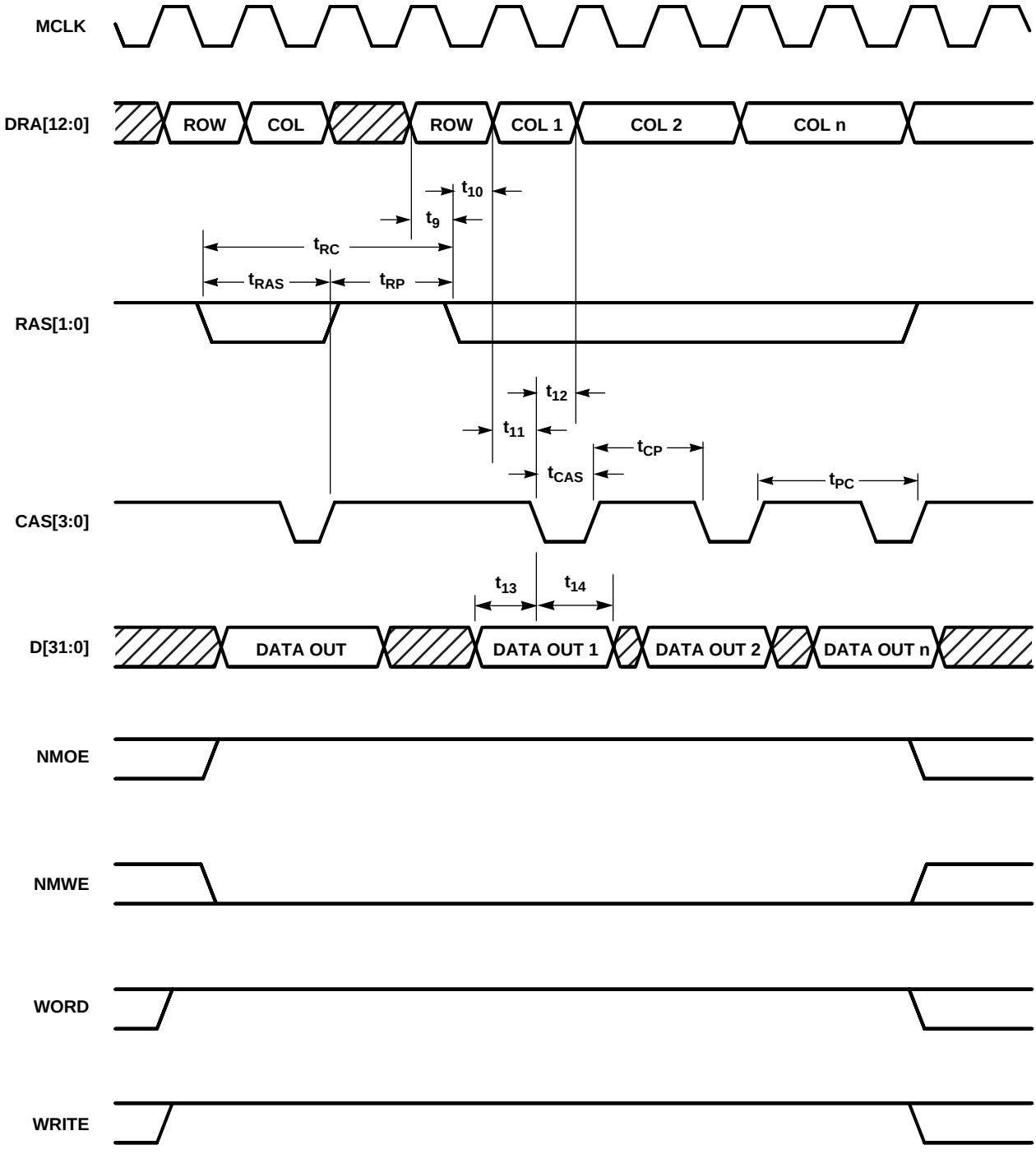


Figure 6-5. DRAM Write Cycles

NOTES:

1) t_{RC} (Write cycle time) = 160 ns maximum at MCLK = 18.432 MHz, and 230 ns at 13.0 MHz

2) t_{RAC} (Write access time from RAS) = 70 ns maximum at MCLK = 18.432 MHz, and 110 ns at 13.0 MHz

3) t_{RP} (RAS precharge time) = 70 ns minimum at MCLK = 18.432 MHz, and 110 ns at 13.0 MHz

4) t_{CAS} (CAS pulse width) = 20 ns maximum at MCLK = 18.432 MHz, and 30 ns at 13.0 MHz

5) t_{CP} (CAS precharge in Page mode) = 66 ns maximum at MCLK = 18.432 MHz, and 140 ns at 13.0 MHz

6) t_{PC} (Page mode cycle time) = 100 ns maximum at MCLK = 18.432 MHz, and 140 ns at 13.0 MHz

7) Word writes shown, for byte writes only one of CAS[3:0] is active, CAS0 for byte 0, etc.

Video quad word read (MCLK shown for reference only)

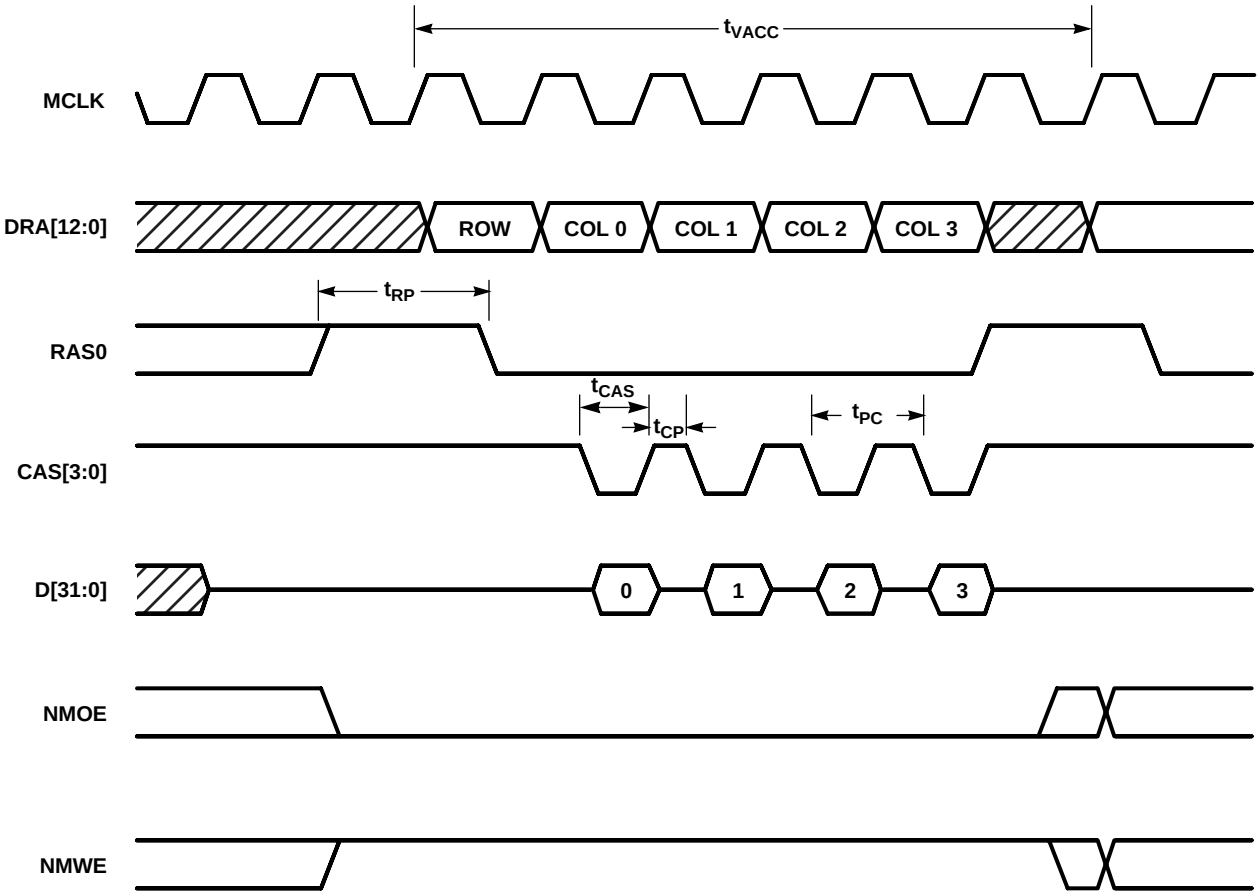


Figure 6-6. Video Quad Word Read from DRAM

NOTES:

1) Timings are the same as Page mode word reads.

2) t_{VACC} (video access cycle time) = 326 ns at MCLK = 18.432 MHz, and 462 ns at 13.0 MHz

DRAM CAS before RAS refresh cycle (MCLK shown for reference only)

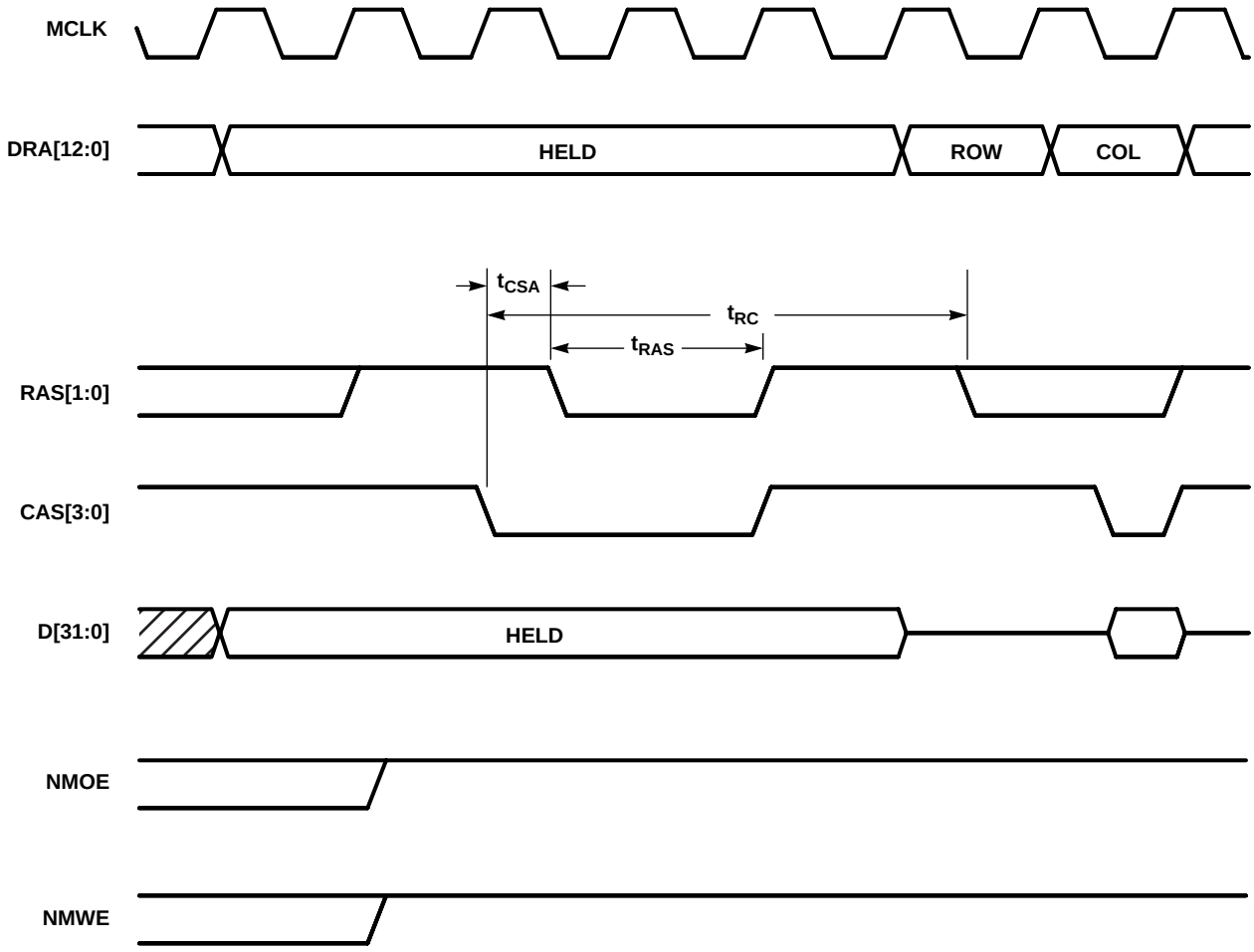


Figure 6-7. DRAM CAS-Before-RAS Refresh Cycle

NOTES:

1) t_{CSA} (CAS set-up time) = 15 ns minimum at MCLK = 18.432 MHz, and 20 ns at 13.0 MHz

2) t_{RAS} (RAS pulse width) = 80 ns minimum at MCLK = 18.432 MHz, and 110 ns at 13.0 MHz

3) t_{RC} (cycle time) = 160 ns minimum at MCLK = 18.432 MHz, and 230 ns at 13.0 MHz

4) When DRAMs are placed in self-refresh (entering standby) the same timings apply, but t_{RAS} is extended indefinitely.

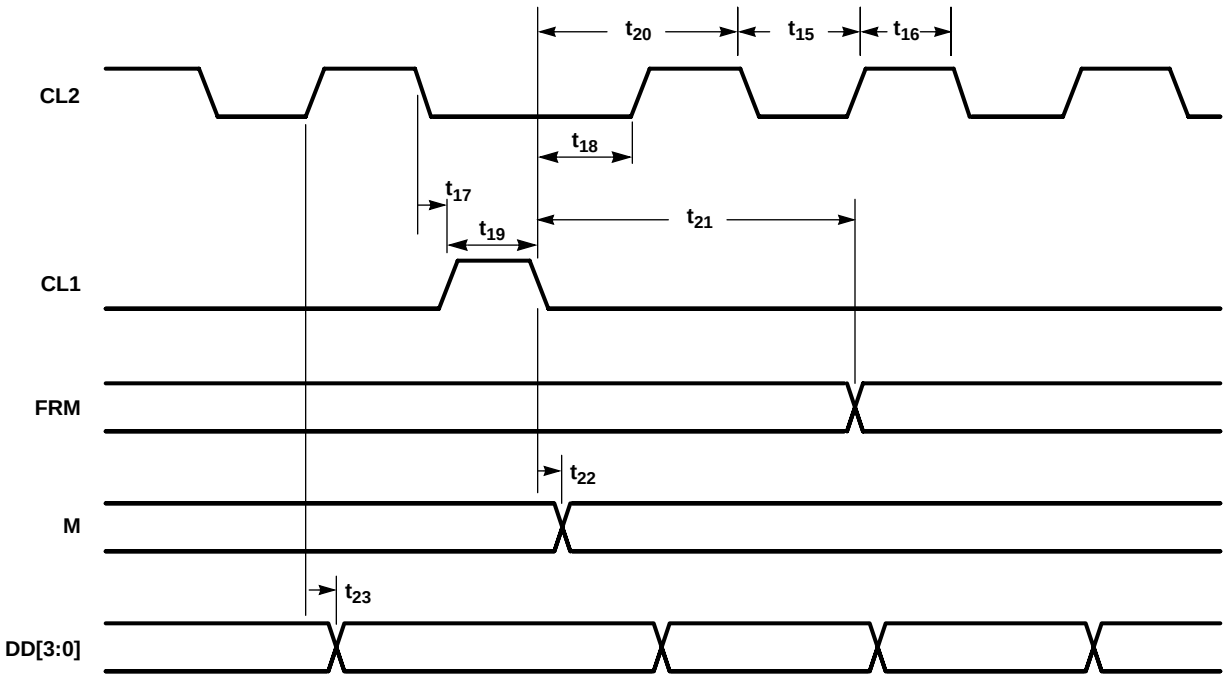


Figure 6-8. LCD Controller Timing

NOTES:

1) This diagram shows the end of a line.

2) If FRM is high during the CL1 pulse, this marks the first line in the display.

3) CL2 low time is doubled during the CL1 high pulse.

6.5 I/O Buffer Characteristics

All I/O buffers on the CL-PS7111 are CMOS threshold input bidirectional buffers except the oscillator and power pads. The output buffer is only enabled during pin test mode for signals that are normally inputs. All output buffers are disabled during System Test (High-Z) mode. All buffers have a standard CMOS threshold input stage apart from the Schmitt inputs and CMOS, slew-rate-controlled output stages to reduce system noise. Table 6-1 defines the I/O buffer output characteristics, which apply across the full range of voltage and temperature (2.7 V and 0 to +70ºC).

Table 6-1. I/O Buffer Output Characteristics

Buffer Type	Drive Current	Propagation Delay (MAX)	Rise Time (MAX)	Fall Time (MAX)	Load
I/O strength 1	± 3 mA	15 ns	20 ns	15 ns	50 pF
I/O strength 2	± 12 mA	12 ns	16 ns	13 ns	50 pF

NOTES:

1) All propagation delays are specified at 50% VDD to 50% VDD; all rise times are specified as 10% VDD to 90% VDD, and all fall times are specified as 90% VDD to 10% VDD.

2) Pull-up current = 50 µA typical at VDD = 3.3 volts.

6.6 Test Modes

The CL-PS7111 supports a number of hardware-activated test modes; these are activated by the pin combinations shown in Table 6-2. All latched signals only alter test modes while NPOR is low, and their state is latched on the rising edge of NPOR. This allows these signals to be used normally during various test modes (for example, the NURESET input can be used normally when the device is set into Functional Test (EPB) mode).

Table 6-2. CL-PS7111 Hardware Test Modes

Test Mode	Latched MEDCHG	Latched PE0	Latched NURESET	NTEST0	NTEST1
Normal operation (32-bit boot)	0	0	X	1	1
Normal operation (8-bit boot)	0	1	X	1	1
Alternative test ROM boot	1	X	X	1	1
Oscillator/PLL bypass	X	X	X	1	0
Functional Test (EPB)	X	X	1	0	1
Oscillator/PLL Test	X	X	0	0	1
Pin Test	X	X	1	0	0
System Test (all High-Z)	X	X	0	0	0

Within each test mode a selection of pins are used as multiplexed outputs or inputs to provide/monitor the test signals unique to that mode.

6.6.1 Oscillator and PLL Bypass Mode

This mode is selected by NTEST0 = 1, NTEST1 = 0.

In this mode all the internal oscillators and PLL are disabled and the appropriate crystal oscillator pins become the direct external oscillator inputs bypassing the oscillator and PLL. MOSCIN must be driven by a 36.864-MHz clock source and RTCOUT by a 32.768-kHz source. In addition the OSCEN (oscillator enable) signal is multiplexed out on the PD[0] pin and can be used to control the external oscillator. The functionality of the CL-PS7111 is not affected in any other way during this test mode.

6.6.2 Functional (EPB) Test Mode

This mode is selected by NTEST0 = 0, NTEST1 = 1, Latched NURESET = 1.

The functional EPB (embedded peripheral bus) Test mode is used for running test patterns, both through the EPB external test interface and other patterns, and is used to test individual peripherals and the ARM710a microprocessor. The PLL is automatically bypassed in this mode. In this mode various pins are used as control inputs or outputs, as listed in Table 6-3. Note that in EPB test mode, the chip only wakes up from the standby state using the external wake-up input. In this mode, the OR function of the Port A inputs which can be used to wake-up the chip is not available.

Table 6-3. EPB Test Mode Signal Assignment

Signal	I/O	Pin	Function
TSTA	I	PA0	EPB test control A
TSTB	I	PA1	EPB test control B
TSTSTART	I	PA2	Fast start speed up RTC divider chain
TSTDIRCLK	I	PA3	Insertion point for EPB test clock
TSTVCOUNT	I	PA4	Video Address counter increments faster
TACK	O	word	EPB test acknowledge output

6.6.3 Oscillator and PLL Test Mode

This mode is selected by NTEST0 = 0, NTEST1 = 1, Latched NURESET = 0.

This test mode enables the main oscillator and output various buffered clock and test signals derived from the main oscillator, PLL, and 32-kHz oscillator. All internal logic in the CL-PS7111 is static and isolated from the oscillators with the exception of the 6-bit ripple counter used to generate 576-kHz and the real-time clock divide chain. Port A is used to drive the inputs of the PLL directly and the various clock and PLL outputs are monitored on the COL pins. Table 6-4 defines the CL-PS7111 signal pins used in this test mode. This mode is only intended to allow tests of the oscillators and PLL.

Table 6-4. Oscillator and PLL Test Mode Signals

Signal	I/O	Pin	Function
TSEL[a]	I	PA5	PLL test select
XTALON[a]	I	PA4	Enable to oscillator circuit

Table 6-4. Oscillator and PLL Test Mode Signals *(cont.)*

PLLON[a]	I	PA3	Enable to PLL circuit
DN0	I	PA2	Selects other frequencies from PLL with DN0
DN1[a]	I	PA1	Selects other frequencies from PLL with DN1
PLLBP	I	PA0	Bypasses PLL
RTCCLK	O	COL0	Output of RTC oscillator
CLK1	O	COL1	1-Hz clock from RTC divide chain
OSC36	O	COL2	36-MHz PLL main output
CLK576K	O	COL4	576 kHz divided-down as above
VTEST	O	COL5	Analog output of VCO loop filter
VREF	O	COL6	VCO output for test

[a] These inputs are INVERTED before being passed to the PLL to ensure that the default state of the port (all '0') maps onto the correct default state of the PLL (TSEL = 1, XTALON = 1, PLLON = 1, D0 = 0, D1 = 1, PLLBP = 0). This state produces the correct frequencies as shown. Any other combinations are for testing the oscillator and PLL and should not be used in the circuit.

6.6.4 Pin Test Mode

This mode is selected by NTEST0 = 0, NTEST1 = 0, Latched NURESET = 1.

This test mode allows a simple ICT or MDA tester to check if all pins on the CL-PS7111 are correctly soldered to the PCB. This mode does this by back-driving each pin in turn and checking the response on one designated pin (the COL7 pin).

A parity bit is generated and output on the COL7 pin; this parity bit is the XOR of the input from every CL-PS7111 signal pin except for the two test inputs. The input pad of each signal is fed into this XOR gate regardless of signal type. Externally driving (back-driving) any signal pin from its reset state causes a transition of the COL7 pin. Table 6-4 defines the rest state for all CL-PS7111 output pins. As Pin Test mode is entered, the states of all CL-PS7111 inputs are latched, and forced back out on the pins. Thus ALL pins (except the two test pins) are configured as outputs in this mode. This ensures only a 'good' solder joint passes the pin test. When not in Pin Test mode, the XOR chain is disabled and cannot toggle to save power.

It is essential in Pin Test mode that the NURESET pin is kept in the default (HIGH) state except when it is being tested itself. This ensures that NPOR can be safely included in the pin test chain without affecting the test mode.

6.6.5 High-Z (System) Test Mode

This mode selected by NTEST0 = 0, NTEST1 = 0, Latched NURESET = 0.

This test mode asynchronously disables all output buffers on the CL-PS7111, removing the CL-PS7111 signal from the PCB so that other devices on the PCB can be tested. The internal state of the CL-PS7111 is not altered directly by this test mode.

6.6.6 Software-Selectable Test Functionality

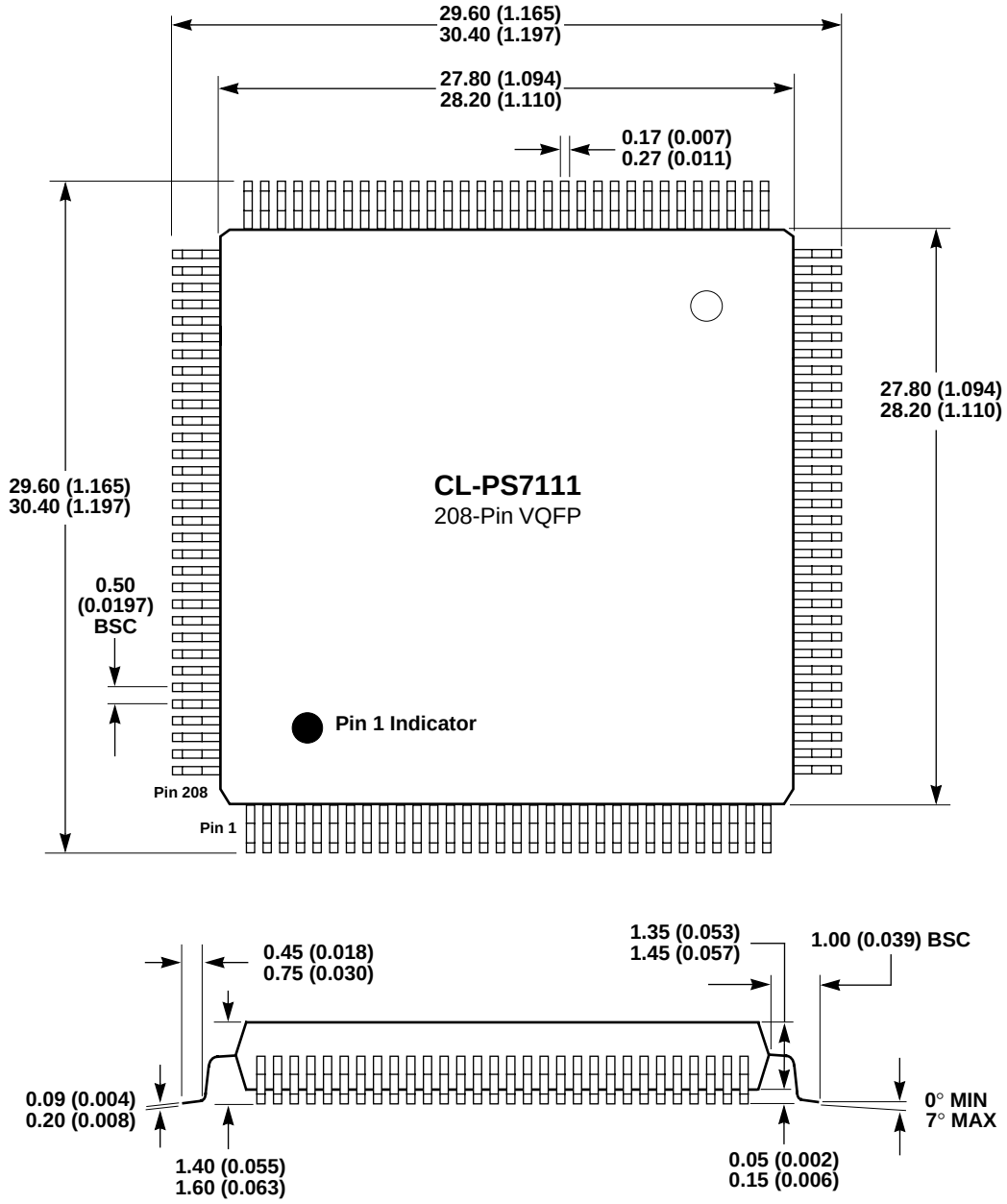
When bit 11 of the SYSCON register is set HIGH, all internal EPB accesses are output on the main address and data buses as though they were external accesses to the address space addressed by CS5. Hence CS5 handles a dual role: It is active as the strobe for internal accesses and for any accesses to the standard address range for CS5. Additionally, in this mode, the internal signals are multiplexed out of the device on port pins, as shown in Table 6-5.

Table 6-5. Software Selectable Test Functionality

Signal	I/O	Pin	Function
CLK	O	PE0	Waited clock to CPU
NIRQ	O	PE1	NIRQ interrupt to CPU
NFIQ	O	PE2	NFIQ interrupt to CPU

7. PACKAGE SPECIFICATIONS

7.1 208-Pin VQFP Package Outline Drawing

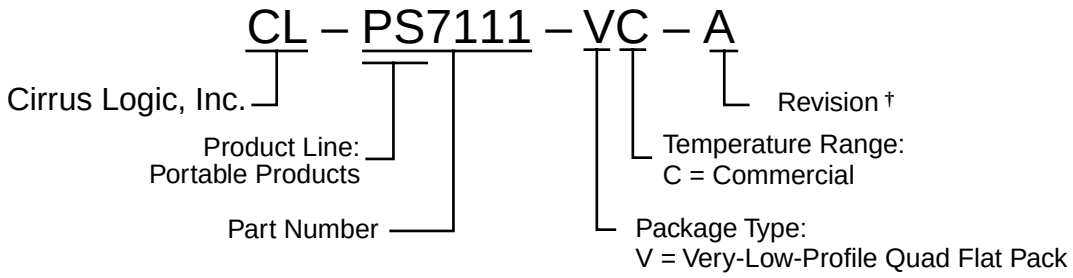


NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

8. ORDERING INFORMATION EXAMPLE

The order number for the device is:



† Contact Cirrus Logic for up-to-date information on revisions.

Appendix A

BOOT CODE

```
;(C) Copyright 1995-1996 , Cirrus Logic, Inc. All Rights Reserved.
;
        TTL         CL-PS7111 Sample program
;       version1.0 (initial version) ;ks
;       boot from uart1
        AREA    |C$$code|,CODE,READONLY
        ENTRY
HwBaseAddress                   EQU                     0x80000000
;
HwControl                       EQU                     0x00000100
HwControl2                      EQU                     0x00001100
HwControlUartEnable             EQU                     0x00000100
;
HwStatus                        EQU                     0x00000140
HwStatus2                       EQU                     0x000001140
HwStatusUartRxFifoEmpty         EQU                     0x00400000
;
HwUartData                      EQU                     0x00000480
HwUartData2                     EQU                     0x00001480
HwUartDataFrameErr              EQU                     0x0100
HwUartDataParityErr             EQU                     0x0200
HwUartDataOverrunErr            EQU                     0x0400
HwUartControl                   EQU                     0x000004C0
HwUartControl2                  EQU                     0x000014C0
HwUartControlRate               EQU                     0x00000FFF
HwUartControlRate115200         EQU                     0x001
```

```
HwUartControlRate76800          EQU                 0x002
HwUartControlRate57600          EQU                 0x003
HwUartControlRate38400          EQU                 0x005
HwUartControlRate19200          EQU                 0x00B
HwUartControlRate14400          EQU                 0x00F
HwUartControlRate9600           EQU                 0x017
HwUartControlRate4800           EQU                 0x02F
HwUartControlRate2400           EQU                 0x05F
HwUartControlRate1200           EQU                 0x0BF
HwUartControlRate600            EQU                 0x17F
HwUartControlRate300            EQU                 0x2FF
HwUartControlRate150            EQU                 0x5FF
HwUartControlRate110            EQU                 0x82E
HwUartControlRate115200_13      EQU                 0x000
HwUartControlRate57600_13       EQU                 0x001
HwUartControlRate38400_13       EQU                 0x002
HwUartControlRate19200_13       EQU                 0x005
HwUartControlRate14400_13       EQU                 0x007
HwUartControlRate9600_13        EQU                 0x00b
HwUartControlRate4800_13        EQU                 0x017
HwUartControlRate2400_13        EQU                 0x02F
HwUartControlRate1200_13        EQU                 0x060
HwUartControlRate600_13         EQU                 0x0c0
HwUartControlRate300_13         EQU                 0x182
HwUartControlRate150_13         EQU                 0x305
HwUartControlRate110_13         EQU                 0x41E
HwUartControlBreak              EQU                 0x00001000
HwUartControlParityEnable       EQU                 0x00002000
HwUartControlPartiyEvenOrOdd    EQU                 0x00004000
 HwUartControlTwoStopBits       EQU                 0x00008000
HwUartControlFifoEnable         EQU                 0x00010000
HwUartControlDataLength         EQU                 0x00060000
HwUartControlDataLength5        EQU                 0x00000000
```

```
HwUartControlDataLength6        EQU                     0x00020000
HwUartControlDataLength7        EQU                     0x00040000
HwUartControlDataLength8        EQU                     0x00060000
;       9600baud, 8bits/ch no parity, 1 stop bit
UartValue           EQU  HwUartControlRate9600+HwUartControlDataLength8
UartValue_13        EQU  HwUartControlRate9600_13+HwUartControlDataLength8
BufferAddress       EQU         0x10000000              ;start address sram
snooze buffer
Codeexeaddr         EQU         0x10000000              ;
Count               EQU         0x00000800              ;2k bytes
startflag           EQU                                 '<'
endflag             EQU                                 '>'
CLKMOD              EQU                                 0x40;clock mode 1 = 13
MHz


;       ARM equates

ArmIrqDisable           EQU     0x00000080
ArmFiqDisable           EQU     0x00000040

ArmUserMode_26          EQU     0x00
ArmFIQMode_26           EQU     0x01
ArmIRQMode_26           EQU     0x02
ArmSVCMode_26           EQU     0x03
ArmAbortMode_26         EQU     0x07
ArmUndefMode_26         EQU     0x0b
;
ArmUserMode             EQU     0x10
ArmFIQMode              EQU     0x11
ArmIRQMode              EQU     0x12
ArmSVCMode              EQU     0x13
ArmAbortMode            EQU     0x17
ArmUndefMode            EQU     0x1B
ArmMaskMode             EQU     0x1F
```

```
;
ArmMmuCP                CP      0xF
;
ArmMmuId                CN      0x00
;
ArmMmuControl           CN      0x01
ArmMmuControlMmuEnable          EQU     0x00000001
ArmMmuControlAlignFaultEnable   EQU     0x00000002
ArmMmuControlCacheEnable        EQU     0x00000004
ArmMmuControlWriteBufferEnable  EQU     0x00000008
ArmMmuControl32BitCodeEnable    EQU     0x00000010
ArmMmuControl32BitDataEnable    EQU     0x00000020
ArmMmuControlMandatory          EQU     0x00000040
ArmMmuControlBigEndianEnable    EQU     0x00000080
ArmMmuControlSystemEnable       EQU     0x00000100
ArmMmuControlRomEnable          EQU     0x00000200
;
ArmMmuPageTableBase     CN      0x02
;
ArmMmuDomainAccess      CN      0x03
 ;
ArmMmuFlushTlb          CN      0x05
;
ArmMmuPurgeTlb          CN      0x06
;
ArmMmuFlushIdc          CN      0x07


;InitialMmuConfig EQU    ArmMmuControl32BitCodeEnable
+ArmMmuControl32BitDataEnable +ArmMmuControlMandatory
+ArmMmuControlBigEndianEnable

InitialMmuConfig EQU    ArmMmuControl32BitCodeEnable
+ArmMmuControl32BitDataEnable +ArmMmuControlMandatory  ;leave as little  endian
11/6/96 ks
```

```
;       set little endian,32bit code, 32bit data

        LDR   r0, =InitialMmuConfig
        MCR   ArmMmuCP,0,r0,ArmMmuControl,c0
;       set the cpu to SVC32 mode

        MRS   r0,CPSR                                   ;read psw
        BIC   r0, r0,#ArmMaskMode;remove the mode
        ORR   r0, r0,#ArmSVCMode;set to supervisory 32 bit mode
        MSR   CPSR,r0
;
;       initialize HW control
UARTEnable
        ldr     r12,=HwBaseAddress
        mov     r0,#HwControlUartEnable        ;Enable UART
        str     r0,[r12,#HwControl]
        ldr     r1,=HwStatus2
        add     r1,r1,r12
        ldr     r2,[r1];read system flag2
        tst     r2,#CLKMOD
        ldreq   r0,=UartValue;load 18 mhz value if bit not set
        ldrne   r0,=UartValue_13;load 13 mhz value if bit set

        str     r0,[r12,#HwUartControl];initialise Uart
;       Send ready signal

        ldr     r0,=startflag
        strb    r0,[r12,#HwUartData];send ready
;       receive the data

        ldr     r3,=count
        ldr     r2,=BufferAddress
```

```
01
;       wait for byte available
        ldr     r1,[r12,#HwStatus];spin, if Rx FIFO is empty
        tst     r1,#HwStatusUartRxFifoEmpty
        bne     %b01
;    read the data, store it and accumulate checksum
        ldrb    r0,[r12,#HwUartData]                    ;read data
        strb    r0,[r2],#1                              ;save it in memory
        subs    r3,r3,#1                                ;decrement count
        bne     %b01                                    ;do more if count has not
expired
;       all received, send end flag
        ldr     r0,=endflag
        strb    r0,[r12,#HwUartData]                    ;send reply
        ldr     r15,=codeexeaddr                        ;jump to execution
address
        LTORG


        END
```

Bit Index

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