TMS320VC33
DIGITAL SIGNAL PROCESSOR

SPRS087 – FEBRUARY 1999

- High-Performance Floating-Point Digital Signal Processor (DSP):
  - TMS320VC33-150
    13-ns Instruction Cycle Time
    150 MFLOPS, 75 MIPS
  - TMS320VC33-120)
    17-ns Instruction Cycle Time
    120 MFLOPS, 60 MIPS
- 32-Bit High-Performance CPU
- 16-/32-Bit Integer and 32-/40-Bit Floating-Point Operations
- Four Precoded Page Strobes to Simplify Interface to I/O and Memory Devices
- 32-Bit Instruction Word, 24-Bit Addresses
- Two 1K × 32-Bit Single-Cycle Dual-Access On-Chip RAM Blocks
- Two 16K × 32-Bit Single-Cycle Dual-Access On-Chip RAM Blocks
- Total of 1.1-Mbit On-Chip SRAM
- Boot-Program Loader
- x(TBD) PLL Clock Generator
- On-Chip Memory-Mapped Peripherals:
  - One Serial Port
  - Two 32-Bit Timers
  - One-Channel Direct Memory Access (DMA) Coprocessor for Concurrent I/O and CPU Operation
- Fabricated Using the 0.18-micron (l_{eff}-effective gate length) TImeline™ Technology by Texas Instruments (TI™)
- 144-Pin Thin Quad Flat Pack (TQFP) (PGE Suffix)
- Eight Extended-Precision Registers
- Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)
- Two Low-Power Modes
- Two- and Three-Operand Instructions
- Parallel Arithmetic/Logic Unit (ALU) and Multiplier Execution in a Single Cycle
- Block-Repeat Capability
- Zero-Overhead Loops With Single-Cycle Branches
- Conditional Calls and Returns
- Interlocked Instructions for Multiprocessing Support
- Bus-Control Registers Configure Strobe-Control Wait-State Generation
- 3.3-V I/O Supply Voltage
- 1.8-V Core Supply Voltage
- Very Low Power: < 200 mW @ 150 MFLOPS

PRODUCT PREVIEW

description

The TMS320VC33 DSP is a 32-bit, floating-point processor manufactured in 0.18-micron four-level-metal CMOS (TImeline) technology. The TMS320VC33 is part of the TMS320C3x generation of DSPs from Texas Instruments.

The TMS320C3x's internal busing and special digital-signal-processing instruction set have the speed and flexibility to execute up to 150 million floating-point operations per second (MFLOPS). The TMS320C3x optimizes speed by implementing functions in hardware that other processors implement through software or microcode. This hardware-intensive approach provides performance previously unavailable on a single chip.

The TMS320C3x can perform parallel multiply and ALU operations on integer or floating-point data in a single cycle. Each processor also possesses a general-purpose register file, a program cache, dedicated ARAUs, internal dual-access memories, one DMA channel supporting concurrent I/O, and a short machine-cycle time. High performance and ease of use are results of these features.

description (continued)

General-purpose applications are greatly enhanced by the large address space, multiprocessor interface, internally and externally generated wait states, one external interface port, two timers, one serial port, and multiple-interrupt structure. The TMS320C3x supports a wide variety of system applications from host processor to dedicated coprocessor.

High-level-language support is easily implemented through a register-based architecture, large address space, powerful addressing modes, flexible instruction set, and well-supported floating-point arithmetic.

TMS320VC33 pinout (top view)

The TMS320VC33 device is packaged in 144-pin thin quad flatpacks (PGE Suffix).

TMS320VC33 PGE PACKAGE
(TOP VIEW)

PRODUCT PREVIEW

TMS320VC33 Terminal Assignments (Alphabetical)

The alphabetical list of terminal assignments is to be supplied.

TMS320VC33 Terminal Assignments (Numerical)

The numerical list of terminal assignments is to be supplied.

TMS320VC33 Terminal Functions

TERMINAL NAME	TERMINAL QTY	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE‡		
PRIMARY-BUS INTERFACE						
D31–D0	32	I/O/Z	32-bit data port	S	H	R
A23–A0	24	O/Z	24-bit address port	S	H	R
R/$\overline{W}$	1	O/Z	Read/write. R/$\overline{W}$ is high when a read is performed and low when a write is performed over the parallel interface.	S	H	R
$\overline{STRB}$	1	O/Z	Strobe. For all external-accesses	S	H	
$\overline{PAGE0}$ – $\overline{PAGE3}$	1	I/O/Z	Page strobes. Four decoded page strobes for external access			
$\overline{RDY}$	1	I	Ready. $\overline{RDY}$ indicates that the external device is prepared for a transaction completion.			
$\overline{HOLD}$	1	I	Hold. When $\overline{HOLD}$ is a logic low, any ongoing transaction is completed. A23–A0, D31–D0, $\overline{STRB}$, and R/$\overline{W}$ are placed in the high-impedance state and all transactions over the primary-bus interface are held until $\overline{HOLD}$ becomes a logic high or until the NOHOLD bit of the primary-bus-control register is set.			
$\overline{HOLDA}$	1	O/Z	Hold acknowledge. $\overline{HOLDA}$ is generated in response to a logic low on $\overline{HOLD}$. $\overline{HOLDA}$ indicates that A23–A0, D31–D0, $\overline{STRB}$, and R/$\overline{W}$ are in the high-impedance state and that all transactions over the bus are held. $\overline{HOLDA}$ is high in response to a logic high of $\overline{HOLD}$ or the NOHOLD bit of the primary-bus-control register is set.	S		
CONTROL SIGNALS						
$\overline{RESET}$	1	I	Reset. When $\overline{RESET}$ is a logic low, the device is in the reset condition. When $\overline{RESET}$ becomes a logic high, execution begins from the location specified by the reset vector.			
$\overline{INT3}$–$\overline{INT0}$	4	I	External interrupts			
$\overline{IACK}$	1	O/Z	Interrupt acknowledge. $\overline{IACK}$ is generated by the IACK instruction. $\overline{IACK}$ can be used to indicate the beginning or the end of an interrupt-service routine.	S		
MCBL/$\overline{MP}$	1	I	Microcomputer Bootloader/microprocessor mode-select			
$\overline{SHZ}$	1	I	Shutdown high impedance. When active, $\overline{SHZ}$ shuts down the device and places all pins in the high-impedance state. $\overline{SHZ}$ is used for board-level testing to ensure that no dual-drive conditions occur. **CAUTION:** A low on $\overline{SHZ}$ corrupts the device memory and register contents. Reset the device with $\overline{SHZ}$ high to restore it to a known operating condition.			
XF1, XF0	2	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instruction.	S		R
SERIAL PORT 0 SIGNALS						
CLKR0	1	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver.	S		R
CLKX0	1	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter.	S		R
DR0	1	I/O/Z	Data-receive. Serial port 0 receives serial data on DR0.	S		R
DX0	1	I/O/Z	Data-transmit output. Serial port 0 transmits serial data on DX0.	S		R
FSR0	1	I/O/Z	Frame-synchronization pulse for receive. The FSR0 pulse initiates the data-receive process using DR0.	S		R
FSX0	1	I/O/Z	Frame-synchronization pulse for transmit. The FSX0 pulse initiates the data-transmit process using DX0.	S		R

† I = input, O = output, Z = high-impedance state
‡ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active

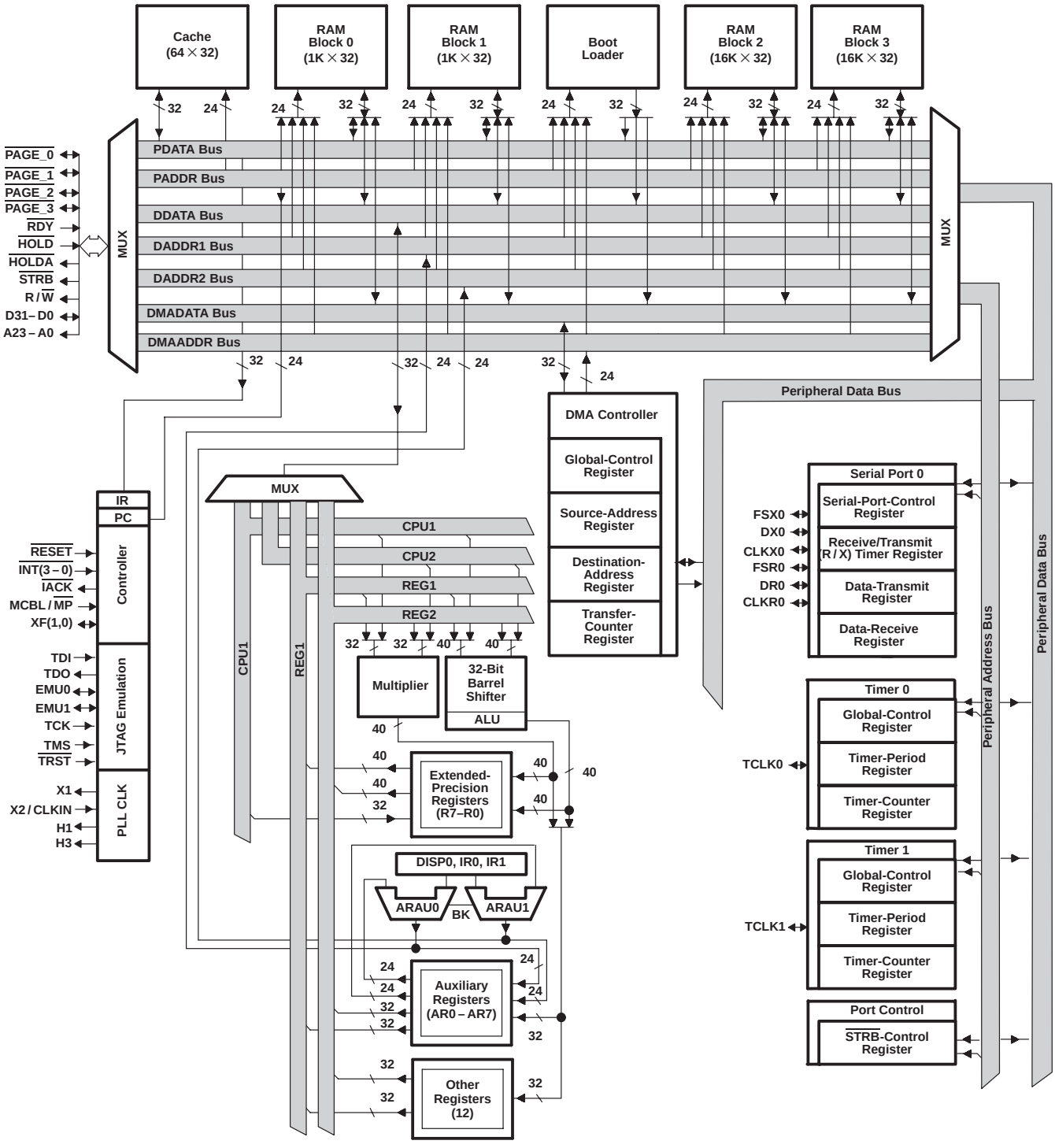
TMS320VC33 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL QTY	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE‡	
TIMER SIGNALS					
TCLK0	1	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S	R
TCLK1	1	I/O/Z	Timer clock 1. As an input, TCLK0 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S	R
SUPPLY AND OSCILLATOR SIGNALS					
H1	1	O/Z	External H1 clock. H1 has a period equal to twice CLKIN.	S	
H3	1	O/Z	External H3 clock. H3 has a period equal to twice CLKIN.	S	
V_{DDL}	10	I	$+V_{DD}$. Dedicated 1.8-V power supply for the core CPU. All must be connected to a common supply plane.§		
V_{DDP}	10	I	$+V_{DD}$. Dedicated 3.3-V power supply for the I/O pins. All must be connected to a common supply plane.§		
V_{SS}	24	I	Ground. All grounds must be connected to a common ground plane.		
X1	1	O	Output from the internal-crystal oscillator. If a crystal is not used, X1 should be left unconnected.		
X2/CLKIN	1	I	Internal-oscillator input from a crystal or a clock		
JTAG EMULATION					
EMU1–EMU0	2	I	Emulation pins 0 and 1		
TDI	1	I	Test data input		
TDO	1	O	Test data output		
TCK	1	I	Test clock		
TMS	1	I	Test mode select		
$\overline{TRST}$	1	I	Test reset		

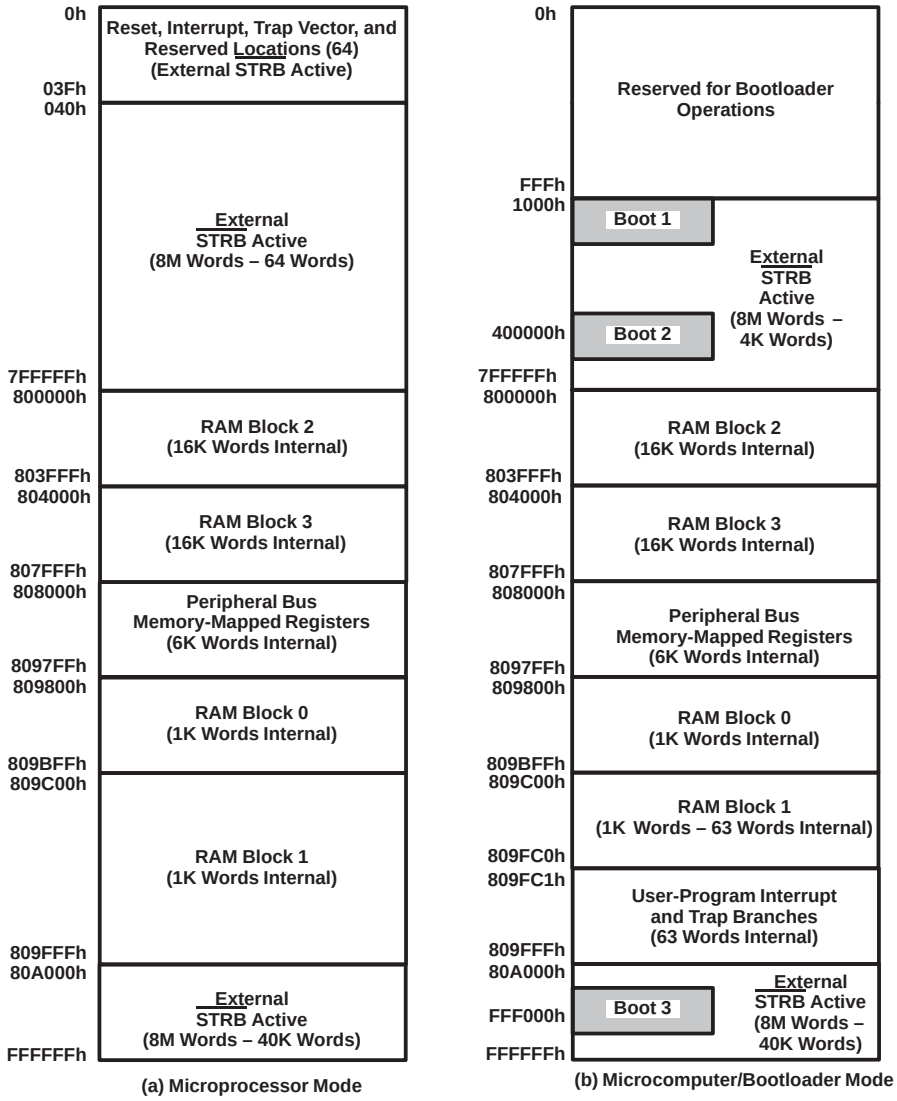
† I = input, O = output, Z = high-impedance state
‡ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active
§ Recommended decoupling. Four 0.1 μF for V_{DDL} and eight 0.1 μF for V_{DDP}.

NOTES: 1. A test mode for measuring leakage currents in the TMS320C33 is implemented. This test mode powers down the clock oscillator circuit resulting in currents below 10 μA. The test mode is entered by asserting SHZ low, which tri–states all output pins and then holds both H1 and H3 at logic high. The test mode is not intended for application use because it does not preserve the processor state.
2. Since SHZ is a synchronized input and the clock is disabled, exiting the test mode occurs only when at least one of the H1/H3 pins is pulled low. Reset cannot be used to wake up in test mode since the SHZ pin is sampled and the clocks are not running.
3. On power up, the processor can be in an indeterminate state. If the state is SHZ mode and H1 and H3 are both held logic high by pull–ups, then shutdown will occur. Normally, if H1 and H3 do not have pull–ups, the rise time lag due to capacitive loading on a tri–state pin is enough to ensure a clean start. However, a slowly rising supply and board leakages to V_{CC} may be enough to cause a bad start. Therefore, a pulldown resistor on either H1 or H3 is recommended for proper wakeup.

functional block diagram



memory map

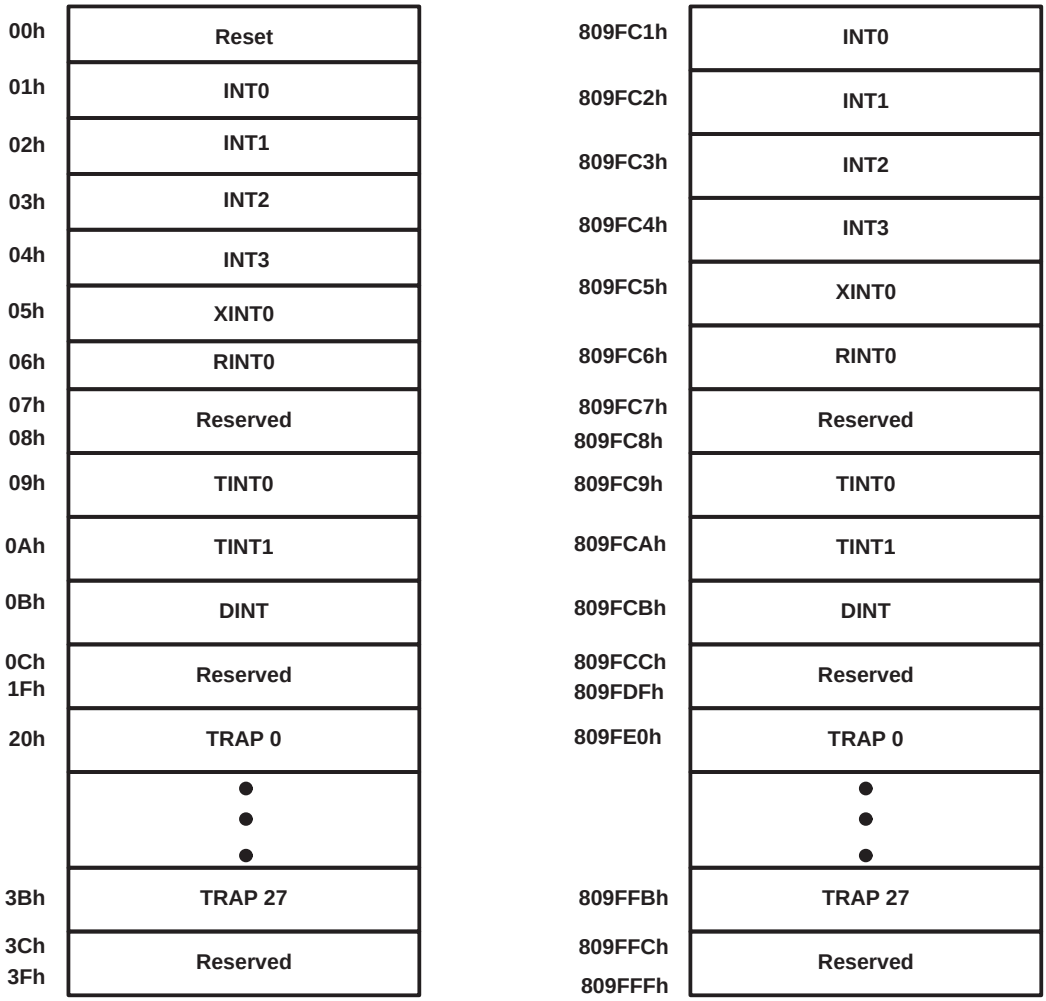


NOTE A: $\overline{\text{STRB}}$ is active over all external memory ranges. $\overline{\text{PAGE\_0}}$ to $\overline{\text{PAGE\_3}}$ are configured as external bus strobes. These are simple decoded strobes that have no configuration registers and are active only during external bus activity over the following ranges:

Name	Active range
$\overline{\text{PAGE\_0}}$	000000h – 03FFFFh
$\overline{\text{PAGE\_1}}$	040000h – 07FFFFh
$\overline{\text{PAGE\_2}}$	080000h – 0BFFFFh
$\overline{\text{PAGE\_3}}$	0C0000h – 0FFFFFh
$\overline{\text{STRB}}$	000000h – 0FFFFFh

Figure 1. TMS320C33 Memory Maps

memory map (continued)



(a) Microprocessor Mode

(b) Microcomputer / Bootloader Mode

Figure 2. Reset, Interrupt, and Trap Vector/Branches Memory-Map Locations

memory map (continued)

808000h	DMA Global Control
808004h	DMA Source Address
808006h	DMA Destination Address
808008h	DMA Transfer Counter
808020h	Timer 0 Global Control
808024h	Timer 0 Counter
808028h	Timer 0 Period Register
808030h	Timer 1 Global Control
808034h	Timer 1 Counter
808038h	Timer 1 Period Register
808040h	Serial Global Control
808042h	FSX/DX/CLKX Serial Port Control
808043h	FSR/DR/CLKR Serial Port Control
808044h	Serial R/X Timer Control
808045h	Serial R/X Timer Counter
808046h	Serial R/X Timer Period Register
808048h	Data-Transmit
80804Ch	Data-Receive
808064h	Primary-Bus Control

NOTE A: Shading denotes reserved address locations.

Figure 3. Peripheral Bus Memory-Mapped Registers

clock generator

The clock generator provides clocks to the ’VC33 device, and consists of an internal oscillator and a phase-locked loop (PLL) circuit. The clock generator requires a reference clock input, which can be provided by using a crystal resonator with the internal oscillator, or from an external clock source. The PLL circuit generates the device clock by multiplying the reference clock frequency by a scale factor, allowing use of a clock source with a lower frequency than that of the CPU.The PLL is an adaptive circuit that, once synchronized, locks onto and tracks an input clock signal.

clock generator (continued)

When the PLL is initially started, it enters a transitional mode during which the PLL acquires lock with the input signal. Once the PLL is locked, it continues to track and maintain synchronization with the input signal.

This clock generator allows system designers to select the clock source. The sources that drive the clock generator are:

- A crystal resonator circuit. The crystal resonator circuit is connected across the X1 and X2/CLKIN pins of the ’VC33 to enable the internal oscillator.
- An external clock. The external clock source is directly connected to the X2/CLKIN pin, and X1 is left unconnected.

The PLL features a fixed rate clock scaler and the capability to directly enable and disable the PLL. The PLL can be configured in one of two clock modes:

- PLL mode. The input clock (X2/CLKIN) is multiplied by a ratio of TBD:1.
- DIV (divider) mode. The input clock is divided by 2. Note that when DIV mode is used, the PLL can be completely disabled in order to minimize power dissipation.

absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{DDP} (see Note 4) . . . . . –0.3 V to 4 V
Supply voltage range, V_{DDL} (see Note 4) . . . . . –0.3 V to 2 V
Input voltage range, V_I . . . . . –0.3 V to 4.5 V
Output voltage range, V_O . . . . . –0.3 V to 4.5 V
Continuous power dissipation (worst case) (see Note 5) . . . . . 500 mW (for TMS320VC33-150)
Operating case temperature range, T_C PQL (commercial) . . . . . 0°C to 85°C
PQA (industrial) . . . . . – 40°C to 125°C
Storage temperature range, T_{stg} . . . . . – 55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 4. All voltage values are with respect to V_{SS}.
5. Actual operating power is less. This value was obtained under specially produced worst-case test conditions for the TMS320C33, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to the external bus at the maximum possible rate with a maximum capacitive load of 40 pF. See normal (I_{CC}) current specification in the electrical characteristics table and also read *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

recommended operating conditions (see Note 6)

		MIN	NOM	MAX	UNIT
V_{DDL}	Supply voltage for the core CPU	1.71	1.8	1.89	V
V_{DDP}	Supply voltage for the I/O pins	3.13	3.3	3.47	V
V_{SS}	Supply ground		0		V
V_{IH}	High-level input voltage	1.8		V_{DD} + 0.3	V
V_{IL}	Low-level input voltage	– 0.3‡		0.6	V
I_{OH}	High-level output current			– 300	µA
I_{OL}	Low-level output current			2	mA
T_C	Operating case temperature (commercial)	0		85	°C
	Operating case temperature (industrial)				°C
V_{TH}	High-level input voltage for CLKIN	2.2		V_{DD} + 0.3	V

NOTE 6: All voltage values are with respect to V_{SS}. CLKIN can be driven by a CMOS clock.

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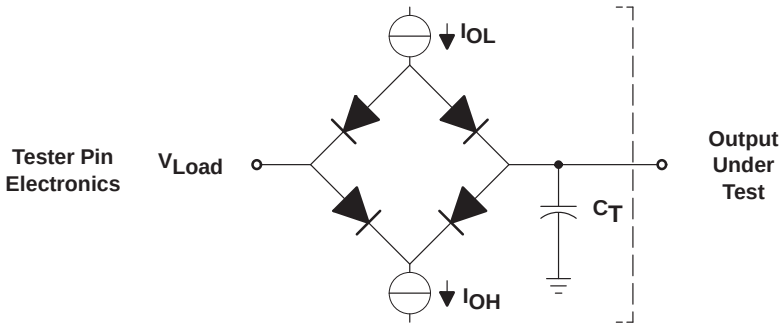
electrical characteristics over recommended ranges of supply voltage (unless otherwise noted) (see Note 6)†

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = MIN, I_{OH} = MAX			2.4			V
V_{OL}	Low-level output voltage	V_{DD} = MIN, I_{OH} = MAX					0.4	V
I_Z	High-impedance current	V_{DD} = MAX			– 5		+5	µA
I_I	Input current	$V_I = V_{SS}$ to V_{DD}			– 5		+ 5	µA
I_{IP}	Input current (with internal pullup)	Inputs with internal pullups§			– 600		10	µA
I_{DDP}	Supply current, pins¶#	T_A = 25°C, DV_{DD} = MAX	f_x = 120 MHz	'VC33-120		20	120	mA
			f_x = 150 MHz	'VC33-150		25	150	
I_{DDL}	Supply current, core CPU¶#	T_A = 25°C, CV_{DD} = MAX	f_x = 120 MHz	'VC33-120		40	50	mA
			f_x = 150 MHz	'VC33-150		45	60	
I_{DD}	Supply current, I_{DPP} plus I_{DDC} (PLL enabled)	Standby, IDLE2 Clocks shut off				5		µA
	Supply current, I_{DPP} plus I_{DDC} (PLL disabled)					500		
C_i	Input capacitance	All inputs except CLKIN					10	pF
		CLKIN					25	
C_o	Output capacitance						10	pF

† All input and output voltage levels are TTL compatible.
‡ For 'VC33, all typical values are at DV_{DD} = 3.3, CV_{DD} = 1.8 V, T_A (air temperature) = 25°C.
§ Pins with internal pullup devices: TDI, TCK, and TMS. Pin with internal pulldown device: $\overline{TRST}$.
¶ Actual operating current is less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern at the maximum rate possible. See *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).
# f_x is the PLL output clock frequency.
NOTE 6: All voltage values are with respect to V_{SS}. CLKIN can be driven by a CMOS clock.

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 1.5 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{LOAD} = 1.5 V
C_T = 40-pF typical load-circuit capacitance

Figure 4. TMS320VC33 Test Load Circuit

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols used herein were created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows, unless otherwise noted:

A	A23–A0	H	H1 and H3
ASYNCH	Asynchronous reset signals	HOLD	$\overline{\text{HOLD}}$
C	CLKX0	HOLDA	$\overline{\text{HOLDA}}$
CI	CLKIN	IACK	$\overline{\text{IACK}}$
CLKR	CLKR0	INT	$\overline{\text{INT3}}$–$\overline{\text{INT0}}$
CONTROL	Control signals	RDY	$\overline{\text{RDY}}$
D	D31–D0	RW	R/$\overline{\text{W}}$
DR	DR	RESET	$\overline{\text{RESET}}$
DX	DX	S	$\overline{\text{STRB}}$
FS	FSX/R	SCK	CLKX/R
FSX	FSX0	SHZ	$\overline{\text{SHZ}}$
FSR	FSR0	TCLK	TCLK0, TCLK1, or TCLKx
GPI	General-purpose input	XF	XF0, XF1, or XFx
GPIO	General-purpose input/output; peripheral pin	XFIO	XFx switching from input to output
GPO	General-purpose output		

timing

Timing specifications apply to the TMS320VC33.

X2/CLKIN, H1, and H3 timing

The following table defines the timing parameters for the X2/CLKIN, H1, and H3 interface signals. The numbers shown in Figure 5 and Figure 6 correspond with those in the NO. column of the table below.

timing parameters for X2/CLKIN, H1, H3 (see Figure 5 and Figure 6)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{f(CI)}$	Fall time, CLKIN					ns
2	$t_{w(CIL)}$	Pulse duration, CLKIN low $t_{c(CI)}$ = min					ns
3	$t_{w(CIH)}$	Pulse duration, CLKIN high $t_{c(CI)}$ = min					ns
4	$t_{r(CI)}$	Rise time, CLKIN					ns
5	$t_{c(CI)}$	Cycle time, CLKIN					ns
6	$t_{f(H)}$	Fall time, H1 and H3					ns
7	$t_{w(HL)}$	Pulse duration, H1 and H3 low					ns
8	$t_{w(HH)}$	Pulse duration, H1 and H3 high					ns
9	$t_{r(H)}$	Rise time, H1 and H3					ns
10	$t_{d(HL-HH)}$	Delay time. from H1 low to H3 high or from H3 low to H1 high					ns
11	$t_{c(H)}$	Cycle time, H1 and H3					ns

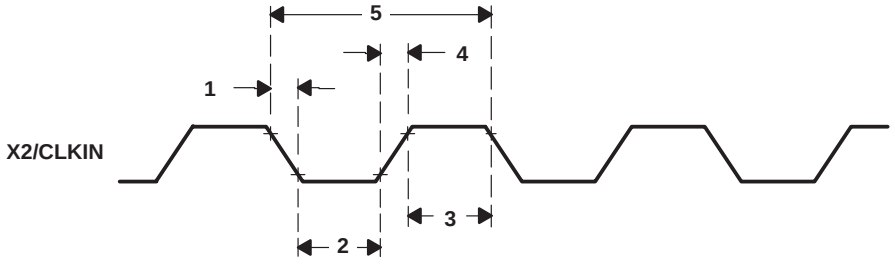


Figure 5. Timing for X2/CLKIN

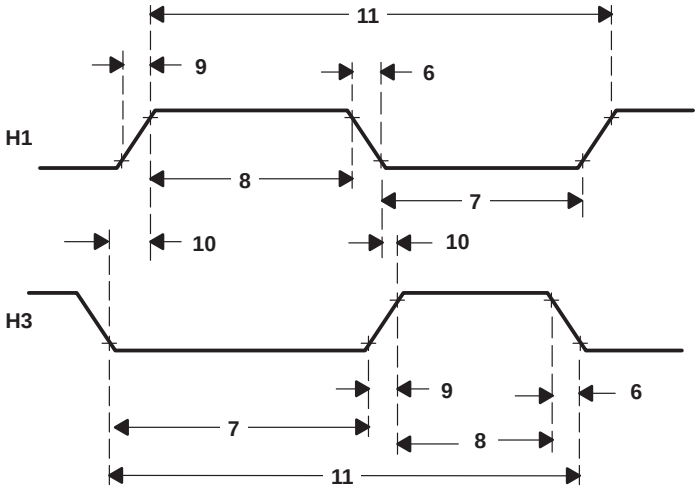


Figure 6. Timing for H1 and H3

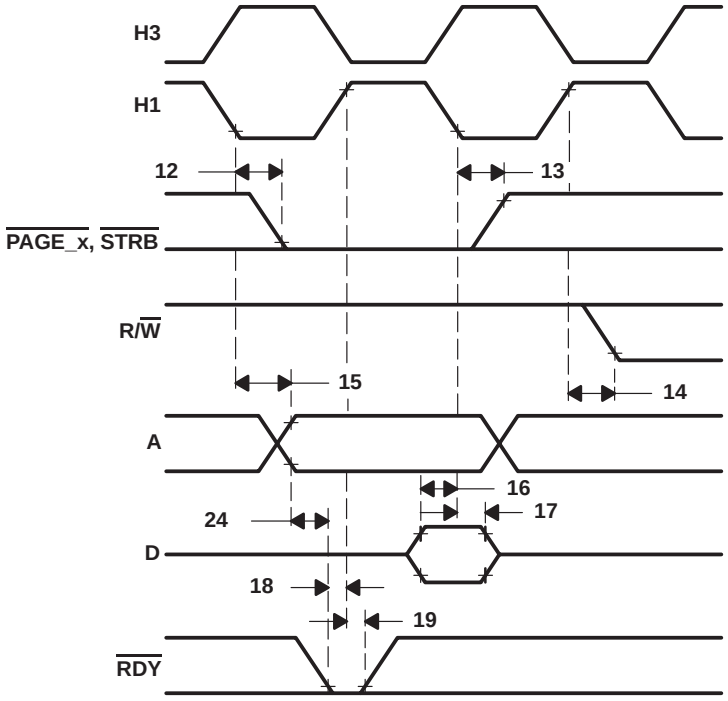
memory read/write timing

The following table defines memory read/write timing parameters for $\overline{\text{STRB}}$. The numbers shown in Figure 7 and Figure 8 correspond with those in the NO. column of the table below.

timing parameters for memory ($\overline{\text{STRB}}$ = 0) read/write (see Figure 7 and Figure 8)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
12	$t_{d(H1L-SL)}$	Delay time, H1 low to $\overline{\text{STRB}}$ low					ns
13	$t_{d(H1L-SH)}$	Delay time, H1 low to $\overline{\text{STRB}}$ high					ns
14	$t_{d(H1H-RWL)R}$	Delay time, H1 high to R/$\overline{\text{W}}$ low (read)					ns
15	$t_{d(H1L-A)}$	Delay time, H1 low to A valid					ns
16	$t_{su(D-H1L)R}$	Setup time, D before H1 low (read)					ns
17	$t_{h(H1L-D)R}$	Hold time, D after H1 low (read)					ns
18	$t_{su(RDY-H1H)}$	Setup time, $\overline{\text{RDY}}$ before H1 high					ns
19	$t_{h(H1H-RDY)}$	Hold time, $\overline{\text{RDY}}$ after H1 high					ns
20	$t_{d(H1H-RWH)W}$	Delay time, H1 high to R/$\overline{\text{W}}$ high (write)					ns
21	$t_{v(H1L-D)W}$	Valid time, D after H1 low (write)					ns
22	$t_{h(H1H-D)W}$	Hold time, D after H1 high (write)					ns
23	$t_{d(H1H-A)W}$	Delay time, H1 high to A valid on back-to-back write cycles (write)					ns
24	$t_{d(A-RDY)}$	Delay time, $\overline{\text{RDY}}$ from A valid					ns
24A	T_{aa}	Address valid to data valid (read)					ns

memory read/write timing (continued)



NOTE B: STRB remains low during back-to-back read operations.

Figure 7. Timing for Memory (STRB = 0 and PAGE_x = 0) Read

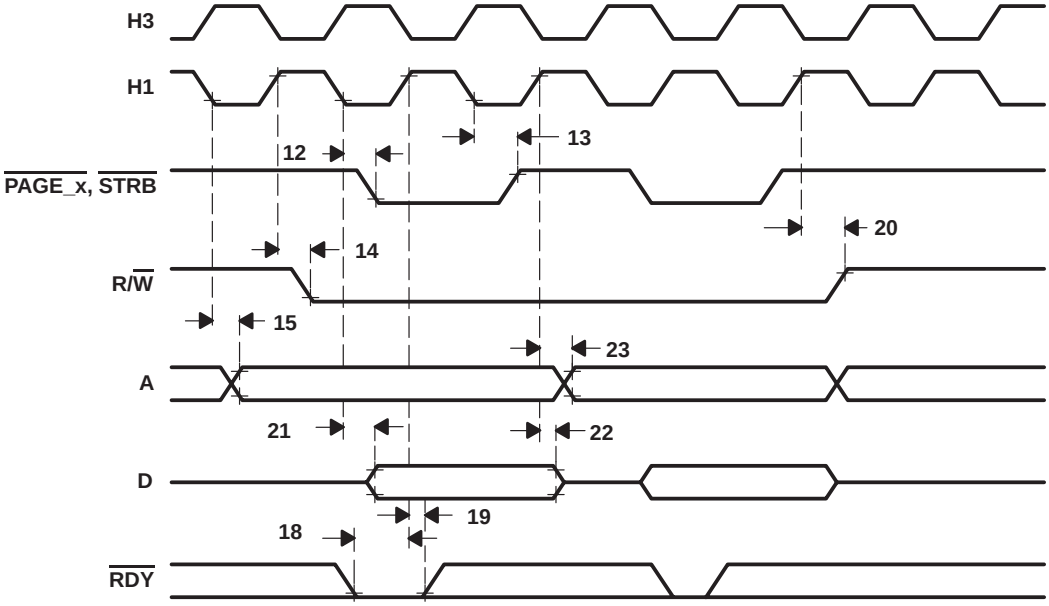


Figure 8. Timing for Memory (STRB = 0 and PAGE_x = 0) Write

XF0 and XF1 timing when executing LDFI or LDII

The following tables define the timing parameters for XF0 and XF1 during execution of LDFI or LDII. The numbers shown in Figure 9 correspond with those in the NO. column of the tables below.

timing parameters for XF0 and XF1 when executing LDFI or LDII for TMS320VC33 (see Figure 9)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
25	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low					ns
26	$t_{su(XF1-H1L)}$	Setup time, XF1 before H1 low					ns
27	$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low					ns

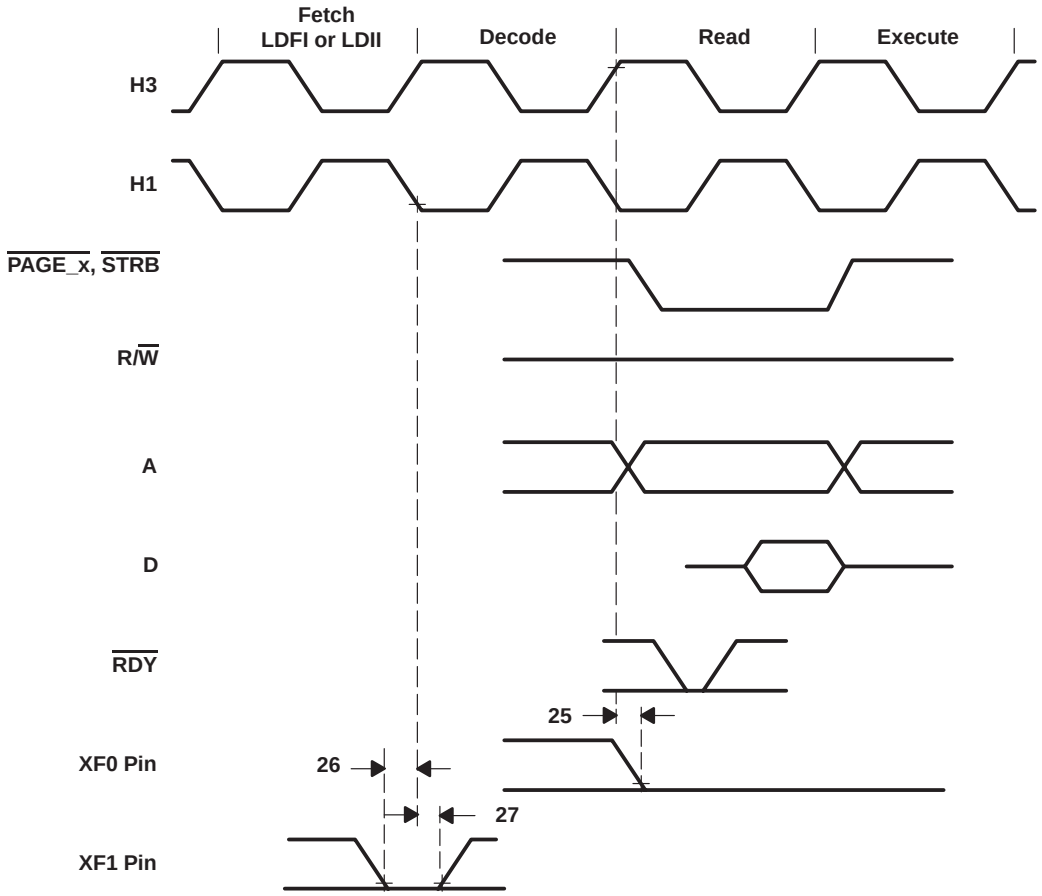


Figure 9. Timing for XF0 and XF1 When Executing LDFI or LDII

XF0 timing when executing STFI and STII†

The following table defines the timing parameters for the XF0 pin during execution of STFI or STII. The number shown in Figure 10 corresponds with the number in the NO. column of the table below.

timing parameters for XF0 when executing STFI or STII (see Figure 10)

NO.		'VC33-120		'VC33-150		UNIT
		MIN	MAX	MIN	MAX	
28	$t_{d(H3H-XF0H)}$ Delay time, H3 high to XF0 high†					ns

† XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is also driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store will not be driven until the store can execute.

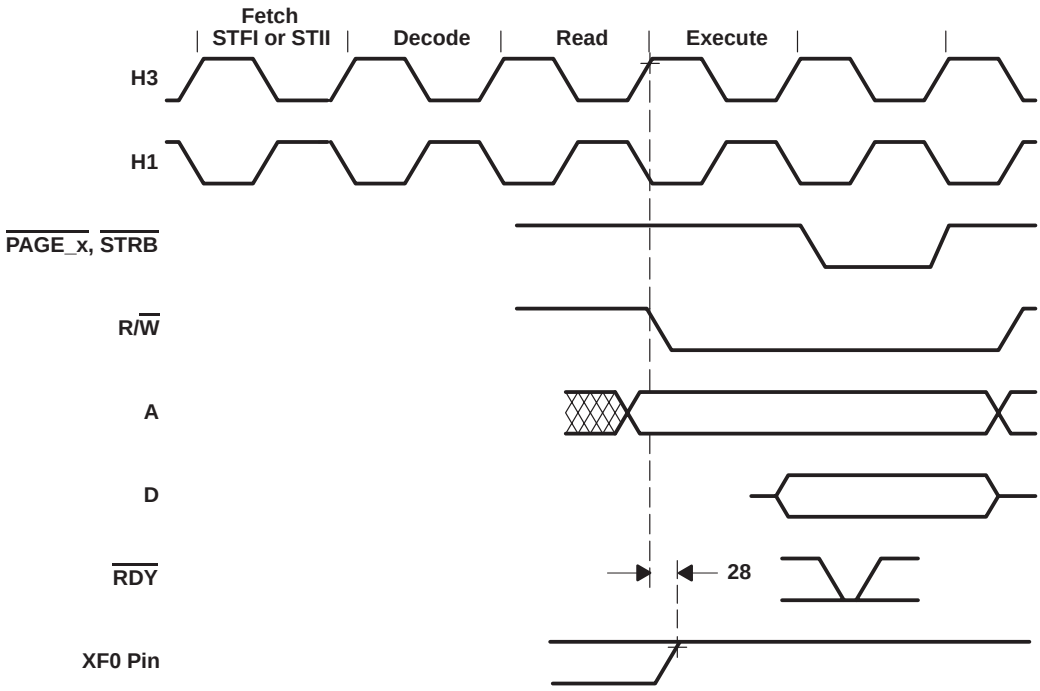


Figure 10. Timing for XF0 When Executing an STFI or STII

XF0 and XF1 timing when executing SIGI

The following tables define the timing parameters for the XF0 and XF1 pins during execution of SIGI. The numbers shown in Figure 11 correspond with those in the NO. column of the tables below.

timing parameters for XF0 and XF1 when executing SIGI (see Figure 11)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
29	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low					ns
30	$t_{d(H3H-XF0H)}$	Delay time, H3 high to XF0 high					ns
31	$t_{su(XF1-H1L)}$	Setup time, XF1 before H1 low					ns
32	$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low					ns

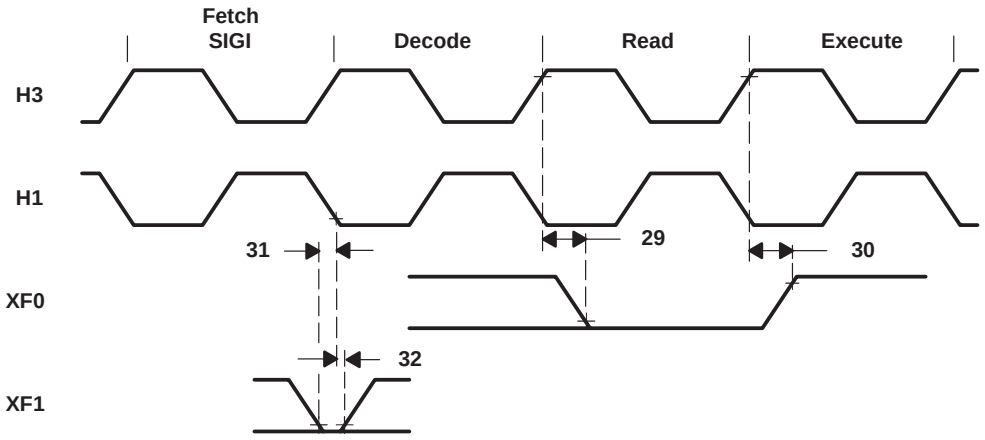


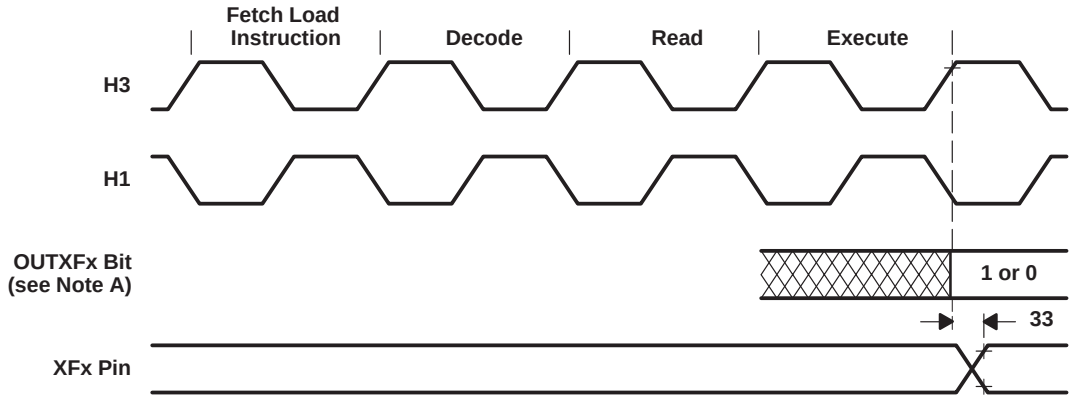
Figure 11. Timing for XF0 and XF1 When Executing SIGI

loading when XF is configured as an output

The following table defines the timing parameter for loading the XF register when the XFx pin is configured as an output. The number shown in Figure 12 corresponds with the number in the NO. column of the table below.

timing parameters for loading the XF register when configured as an output pin (see Figure 12)

NO.		'VC33-120		'VC33-150		UNIT
		MIN	MAX	MIN	MAX	
33	$t_{v(H3H-XF)}$ Valid time, H3 high to XFx					ns



NOTE A: OUTXFx represents either bit 2 or 6 of the IOF register.

Figure 12. Timing for Loading XF Register When Configured as an Output Pin

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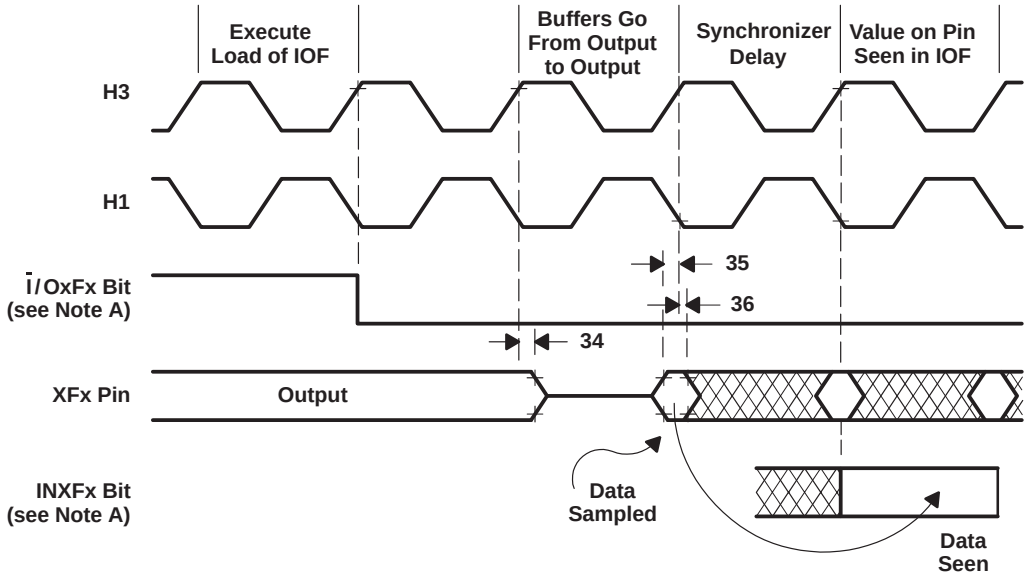
changing XFx from an output to an input

The following table defines the timing parameters for changing the XFx pin from an output pin to an input pin. The numbers shown in Figure 13 correspond with those in the NO. column of the table below.

timing parameters of XFx changing from output to input mode (see Figure 13)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
34	$t_{h(H3H-XF)}$	Hold time, XFx after H3 high					ns
35	$t_{su(XF-H1L)}$	Setup time, XFx before H1 low					ns
36	$t_{h(H1L-XF)}$	Hold time, XFx after H1 low					ns



NOTE A: I/OxFx represents either bit 1 or bit 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of the IOF register.

Figure 13. Timing for Change of XFx From Output to Input Mode

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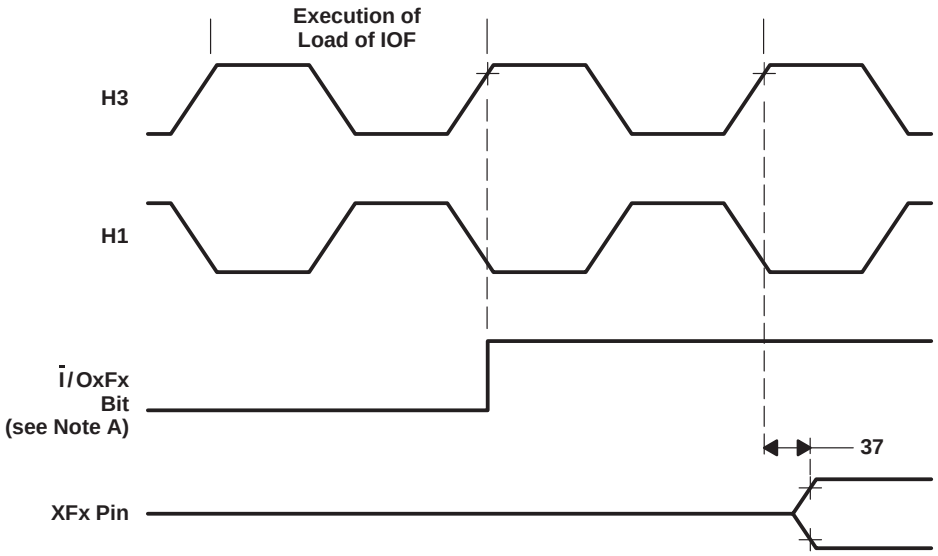
changing XFx from an input to an output

The following table defines the timing parameter for changing the XFx pin from an input pin to an output pin. The number shown in Figure 14 corresponds with the number in the NO. column of the table below.

timing parameters of XFx changing from input to output mode (see Figure 14)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
37	$t_{d(H3H-XFIO)}$	Delay time, H3 high to XFx switching from input to output					ns



NOTE A: I/OxFx represents either bit 1 or bit 5 of the IOF register.

Figure 14. Timing for Change of XFx From Input to Output Mode

reset timing

RESET is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 15 occurs; otherwise, an additional delay of one clock cycle is possible.

The asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.

The following table defines the timing parameters for the RESET signal. The numbers shown in Figure 15 correspond with those in the NO. column of the following table.

Resetting the device initializes the bus control register to seven software wait states and therefore results in slow external accesses until these registers are initialized.

HOLD is an asynchronous input and can be asserted during reset.

timing parameters for $\overline{\text{RESET}}$ for the TMS320VC33 (see Figure 15)

NO.			’VC33-120		’VC33-150		UNIT
			MIN	MAX	MIN	MAX	
38	$t_{su(RESET-CIL)}$	Setup time, $\overline{\text{RESET}}$ before CLKIN low					ns
39	$t_{d(CLKINH-H1H)}$	Delay time, CLKIN high to H1 high					ns
40	$t_{d(CLKINH-H1L)}$	Delay time, CLKIN high to H1 low					ns
41	$t_{su(RESETH-H1L)}$	Setup time, $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles					ns
42	$t_{d(CLKINH-H3L)}$	Delay time, CLKIN high to H3 low					ns
43	$t_{d(CLKINH-H3H)}$	Delay time, CLKIN high to H3 high					ns
44	$t_{dis(H1H-DZ)}$	Disable time, H1 high to D (high impedance)					ns
45	$t_{dis(H3H-AZ)}$	Disable time, H3 high to A (high impedance)					ns
46	$t_{d(H3H-CONTROLH)}$	Delay time, H3 high to control signals high					ns
47	$t_{d(H1H-RWH)}$	Delay time, H1 high to R/$\overline{\text{W}}$ high					ns
48	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high					ns
49	$t_{dis(RESETL-ASYNCH)}$	Disable time, $\overline{\text{RESET}}$ low to asynchronous reset signals disabled (high impedance)					ns

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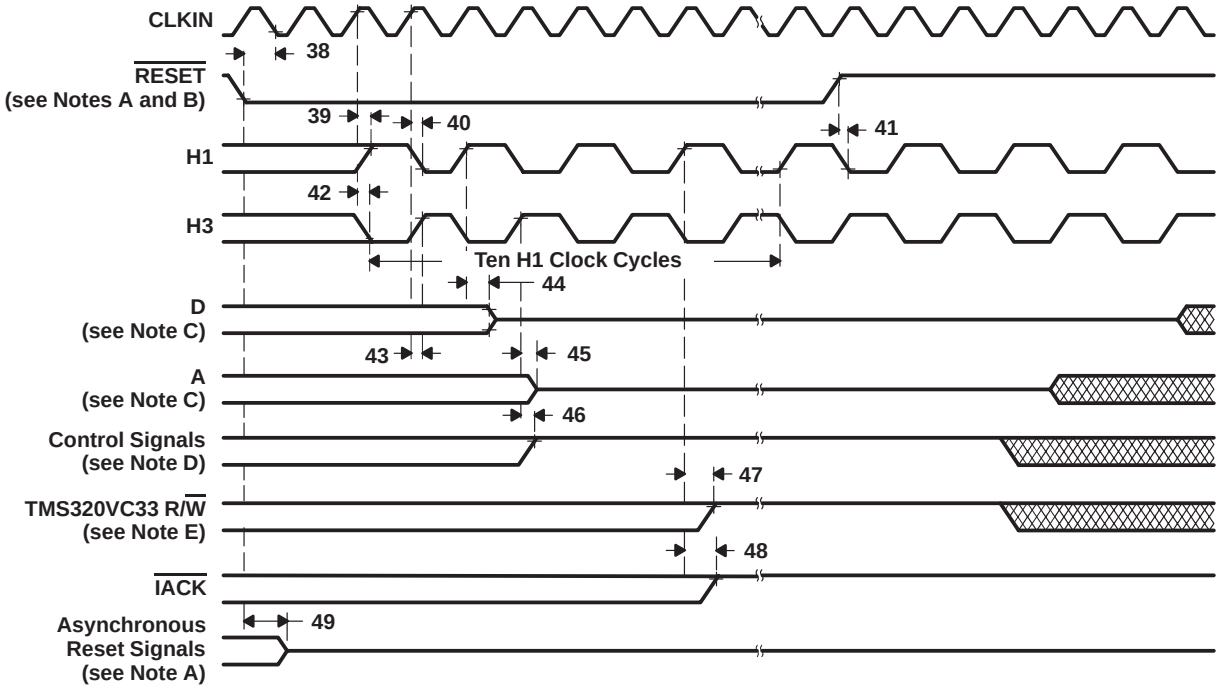
timing parameters for $\overline{\text{RESET}}$ for the TMS32V0C33 (continued)



NOTES: A. Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.
B. $\overline{\text{RESET}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle is possible.
C. In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In microcomputer mode, the reset vector is fetched twice, with no software wait states.
D. Control signals include $\overline{\text{STRB}}$ and $\overline{\text{PAGE\_x}}$.
E. The R/$\overline{\text{W}}$ outputs are placed in a high-impedance state during reset and can be provided with a resistive pullup, nominally 18–22 kΩ, if undesirable spurious writes are caused when these outputs go low.

Figure 15. Timing for $\overline{\text{RESET}}$

interrupt response timing

The following table defines the timing parameters for the $\overline{\text{INT}}$ signals. The numbers shown in Figure 16 correspond with those in the NO. column of the table below.

timing parameters for $\overline{\text{INT3}}$–$\overline{\text{INT0}}$ response (see Figure 16)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
50	$t_{su(INT-H1L)}$	Setup time, $\overline{\text{INT3}}$– $\overline{\text{INT0}}$ before H1 low					ns
51	$t_{w(INT)}$	Pulse duration, interrupt to ensure only one interrupt					ns

The interrupt ($\overline{\text{INT}}$) pins are asynchronous inputs that can be asserted at any time during a clock cycle. The TMS320C3x interrupts are level-sensitive, not edge-sensitive. Interrupts are detected on the falling edge of H1. Therefore, interrupts must be set up and held to the falling edge of H1 for proper detection. The CPU and DMA respond to detected interrupts on instruction-fetch boundaries only.

For the processor to recognize only one interrupt on a given input, an interrupt pulse must be set up and held to:

- A minimum of one H1 falling edge
- No more than two H1 falling edges

The TMS320C3x can accept an interrupt from the same source every two H1 clock cycles.

If the specified timings are met, the exact sequence shown in Figure 16 occurs; otherwise, an additional delay of one clock cycle is possible.

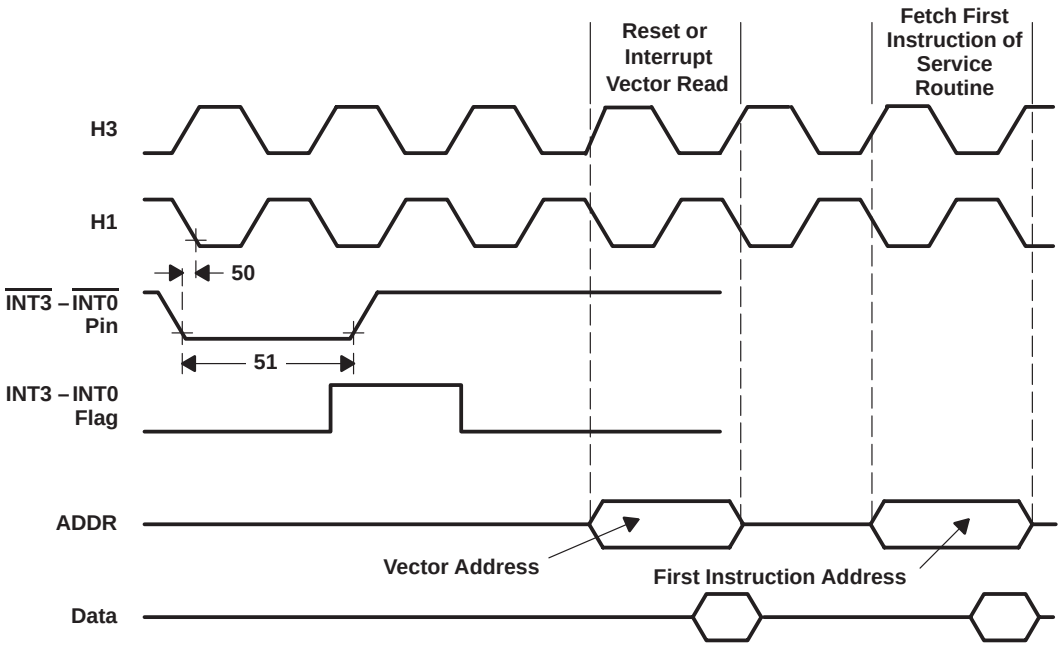


Figure 16. Timing for $\overline{\text{INT3}}$–$\overline{\text{INT0}}$ Response

interrupt-acknowledge timing

The $\overline{\text{IACK}}$ output goes active on the first half-cycle (HI rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (HI rising) of the read phase of the IACK instruction.

The following table defines the timing parameters for the $\overline{\text{IACK}}$ signal. The numbers shown in Figure 17 correspond with those in the NO. column of the table below.

timing parameters for $\overline{\text{IACK}}$ (see Figure 17)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
52	$t_{d(H1H-IACKL)}$	Delay time, H1 high to $\overline{\text{IACK}}$ low					ns
53	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high					ns

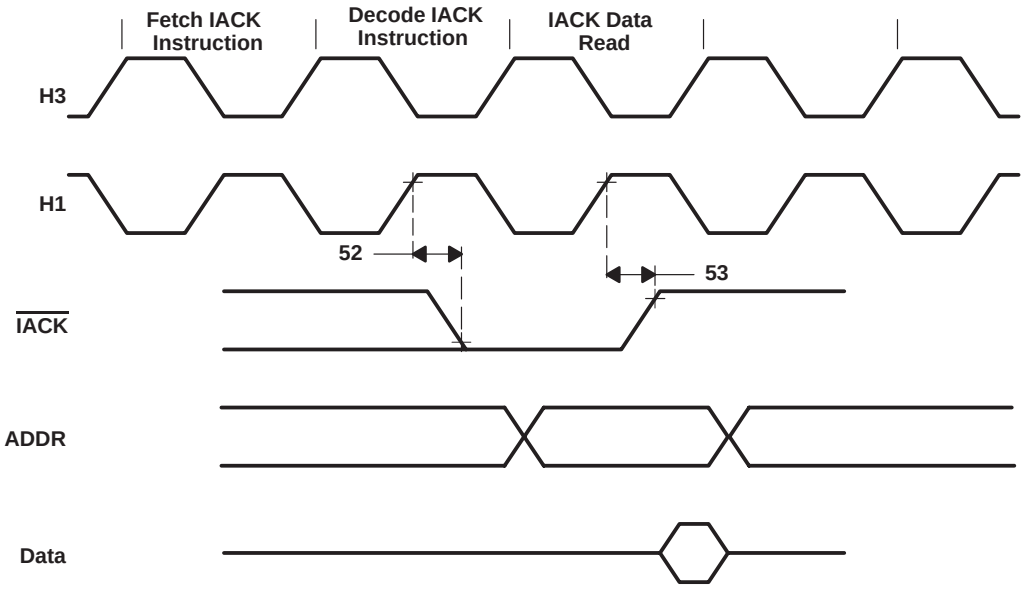


Figure 17. Timing for $\overline{\text{IACK}}$

serial-port timing parameters for TMS320VC33-120 (see Figure 18 and Figure 19)

NO.				’VC33-120		UNIT
				MIN	MAX	
54	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R				ns
55	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext			ns
			CLKX/R int			
56	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext			ns
			CLKX/R int			
57	$t_{r(SCK)}$	Rise time, CLKX/R				ns
58	$t_{f(SCK)}$	Fall time, CLKX/R				ns
59	$t_{d(C-DX)}$	Delay time, CLKX to DX valid	CLKX ext			ns
			CLKX int			
60	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext			ns
			CLKR int			
61	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext			ns
			CLKR int			
62	$t_{d(C-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext			ns
			CLKX int			
63	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext			ns
			CLKR int			
64	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext			ns
			CLKX/R int			
65	$t_{su(FSX-C)}$	Setup time, external FSX before CLKX	CLKX ext			ns
			CLKX int			
66	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext			ns
			CLKX int			
67	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX				ns
68	$t_{d(CH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit				ns

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serial-port timing parameters for TMS320VC33-150 (see Figure 18 and Figure 19)

NO.				’VC33-150		UNIT
				MIN	MAX	
54	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R				ns
55	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext			ns
			CLKX/R int			
56	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext			ns
			CLKX/R int			
57	$t_{r(SCK)}$	Rise time, CLKX/R				ns
58	$t_{f(SCK)}$	Fall time, CLKX/R				ns
59	$t_{d(C-DX)}$	Delay time, CLKX to DX valid	CLKX ext			ns
			CLKX int			
60	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext			ns
			CLKR int			
61	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext			ns
			CLKR int			
62	$t_{d(C-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext			ns
			CLKX int			
63	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext			ns
			CLKR int			
64	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext			ns
			CLKX/R int			
65	$t_{su(FSX-C)}$	Setup time, external FSX before CLKX	CLKX ext			ns
			CLKX int			
66	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext			ns
			CLKX int			
67	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX				ns
68	$t_{d(CH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit				ns

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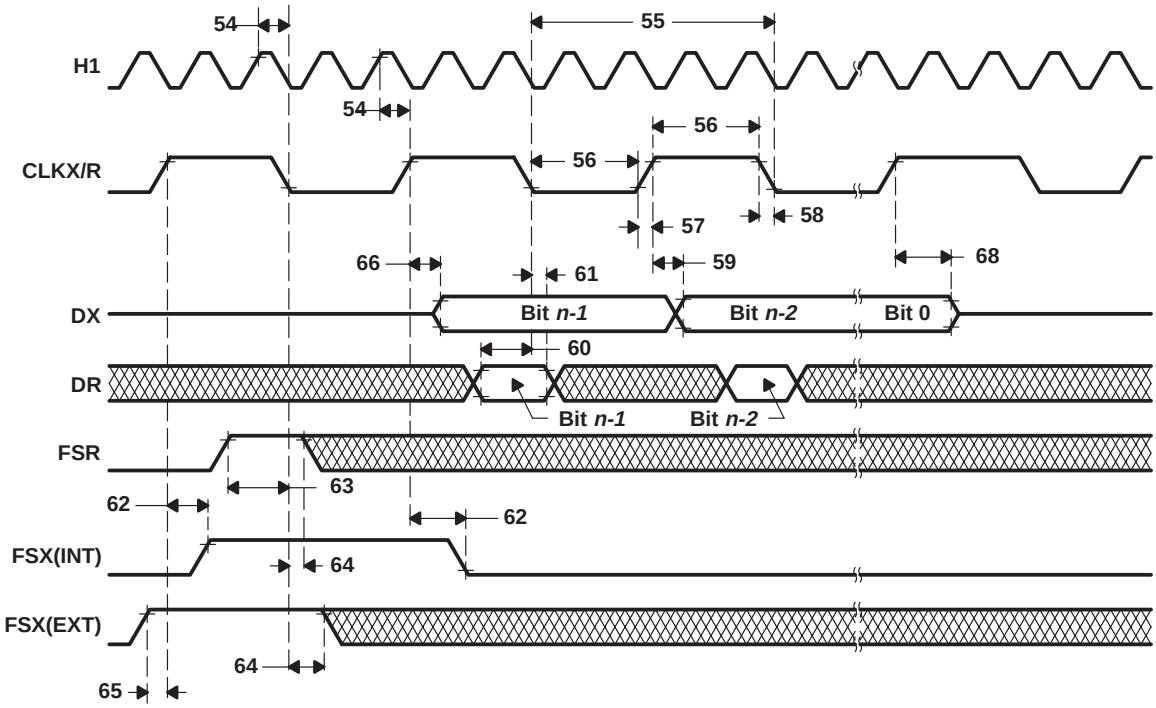
data-rate timing modes

Unless otherwise indicated, the data-rate timings shown in Figure 18 and Figure 19 are valid for all serial-port modes, including handshake. For a functional description of serial-port operation refer to subsection 8.2.12 of the *TMS320C3x User's Guide* (literature number SPRU031).

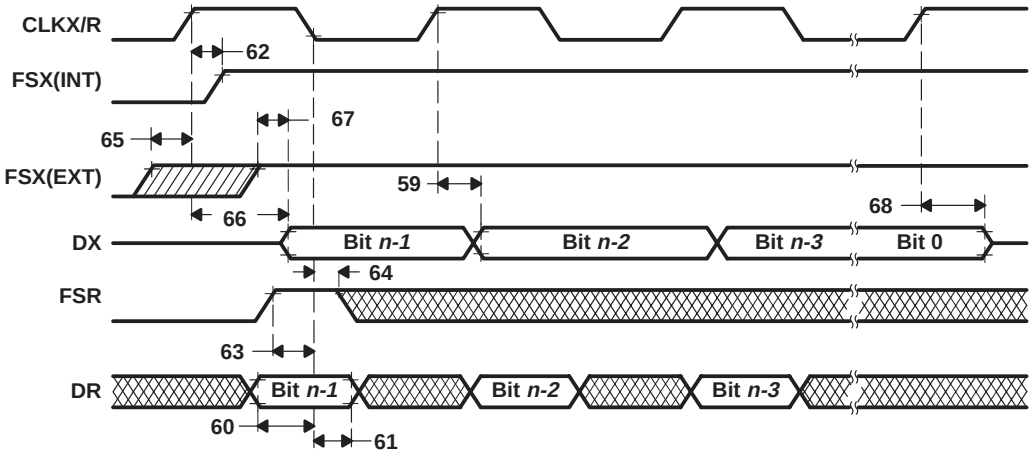
The serial-port timing parameters for seven 'C3x devices are defined in the preceding "serial-port timing parameters" tables. The numbers shown in Figure 18 and Figure 19 correspond with those in the NO. column of each table.



NOTES: A. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.

Figure 18. Timing for Fixed Data-Rate Mode

data-rate timing modes (continued)



NOTES: A. Timing diagrams show operation with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.
C. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

Figure 19. Timing for Variable Data-Rate Mode

$\overline{\text{HOLD}}$ timing

$\overline{\text{HOLD}}$ is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 27 occurs; otherwise, an additional delay of one clock cycle is possible.

The table, “timing parameters for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$”, defines the timing parameters for the $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ signals. The numbers shown in Figure 20 correspond with those in the NO. column of the table.

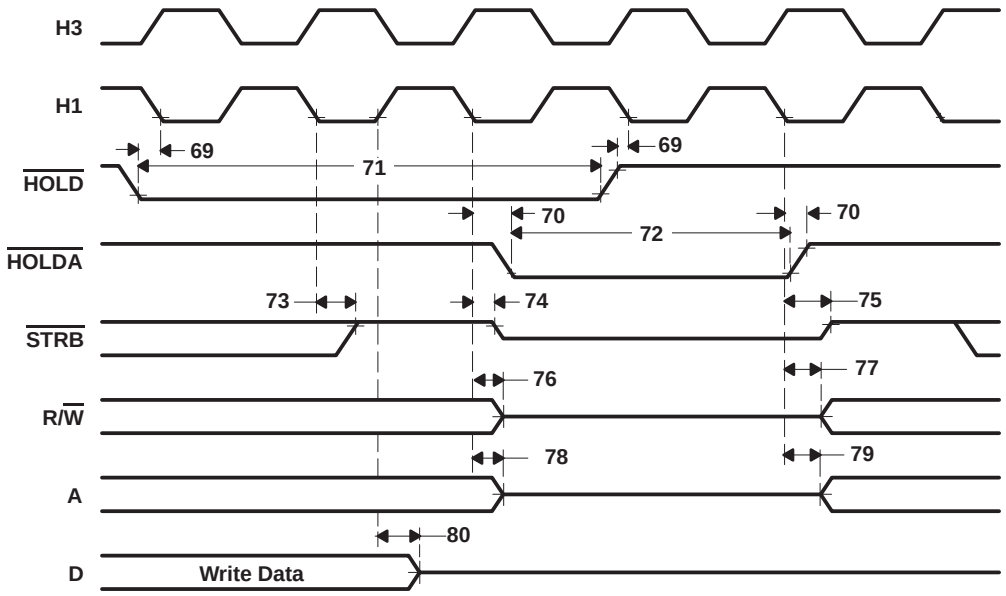
The NOHOLD bit of the primary-bus control register overrides the $\overline{\text{HOLD}}$ signal. When this bit is set, the device comes out of hold and prevents future hold cycles.

Asserting $\overline{\text{HOLD}}$ prevents the processor from accessing the primary bus. Program execution continues until a read from or a write to the primary bus is requested. In certain circumstances, the first write is pending, thus allowing the processor to continue until a second write is encountered.

timing parameters for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ (see Figure 20)

NO.			’VC33-120		’VC33-150		UNIT
			MIN	MAX	MIN	MAX	
69	$t_{su(HOLD-H1L)}$	Setup time, $\overline{\text{HOLD}}$ before H1 low					ns
70	$t_{v(H1L-HOLDA)}$	Valid time, $\overline{\text{HOLDA}}$ after H1 low					ns
71	$t_{w(HOLD)}$	Pulse duration, $\overline{\text{HOLD}}$ low					ns
72	$t_{w(HOLDA)}$	Pulse duration, $\overline{\text{HOLDA}}$ low					ns
73	$t_{d(H1L-SH)H}$	Delay time, H1 low to $\overline{\text{STRB}}$ high for a $\overline{\text{HOLD}}$					ns
74	$t_{dis(H1L-S)}$	Disable time, H1 low to $\overline{\text{STRB}}$ to the high-impedance state					ns
75	$t_{en(H1L-S)}$	Enable time, H1 low to $\overline{\text{STRB}}$ enabled (active)					ns
76	$t_{dis(H1L-RW)}$	Disable time, H1 low to R/$\overline{\text{W}}$ to the high-impedance state					ns
77	$t_{en(H1L-RW)}$	Enable time, H1 low to R/$\overline{\text{W}}$ enabled (active)					ns
78	$t_{dis(H1L-A)}$	Disable time, H1 low to address to the high-impedance state					ns
79	$t_{en(H1L-A)}$	Enable time, H1 low to address enabled (valid)					ns
80	$t_{dis(H1H-D)}$	Disable time, H1 high to data to the high-impedance state					ns

$\overline{\text{HOLD}}$ timing (continued)



NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

Figure 20. Timing for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$

general-purpose I/O timing

Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The contents of the internal control registers associated with each peripheral define the modes for these pins.

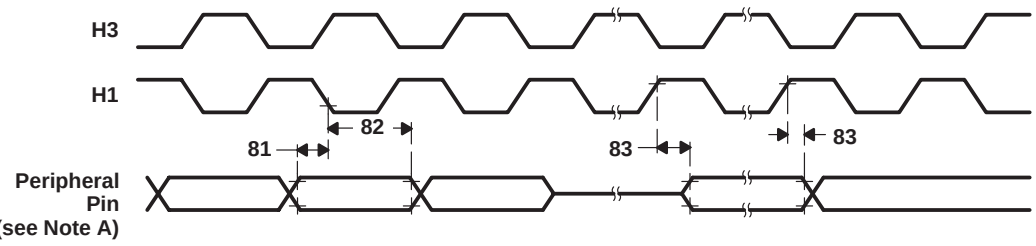
peripheral pin I/O timing

The table, timing parameters for peripheral pin general-purpose I/O, defines peripheral pin general-purpose I/O timing parameters. The numbers shown in Figure 21 correspond with those in the NO. column of the table below.

timing parameters for peripheral pin general-purpose I/O (see Note 7 and Figure 21)

NO.			’VC33-120		’VC33-150		UNIT
			MIN	MAX	MIN	MAX	
81	$t_{su(GPIO-H1L)}$	Setup time, general-purpose input before H1 low					ns
82	$t_{h(H1L-GPIO)}$	Hold time, general-purpose input after H1 low					ns
83	$t_{d(H1H-GPIO)}$	Delay time, general-purpose output after H1 high					ns

NOTE 7: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 21. Timing for Peripheral Pin General-Purpose I/O

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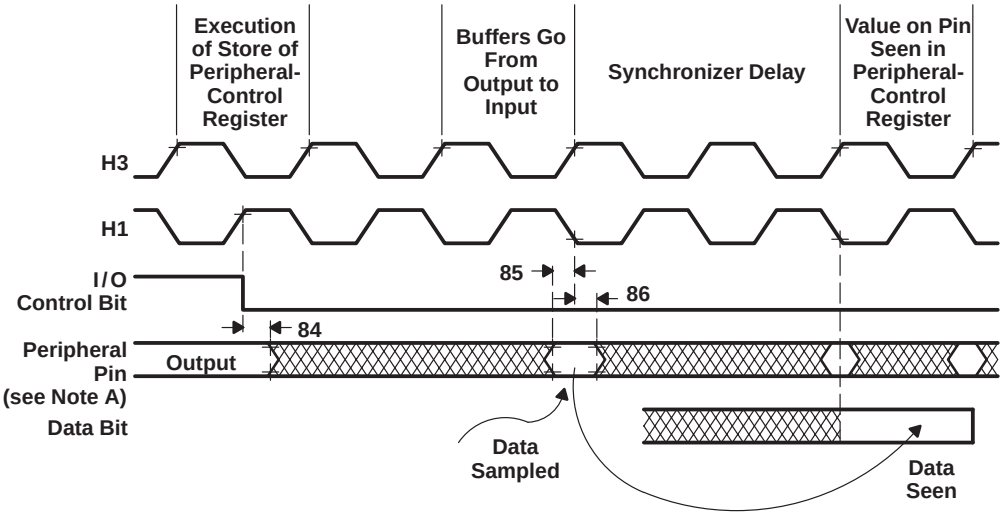
changing the peripheral pin I/O modes

The following tables show the timing parameters for changing the peripheral pin from a general-purpose output pin to a general-purpose input pin and vice versa. The numbers shown in Figure 22 and Figure 23 correspond to those shown in the NO. column of the tables below.

timing parameters for peripheral pin changing from general-purpose output to input mode (see Note 7 and Figure 22)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
84	$t_{h(H1H)}$	Hold time, peripheral pin after H1 high					ns
85	$t_{su(GPIO-H1L)}$	Setup time, peripheral pin before H1 low					ns
86	$t_{h(H1L-GPIO)}$	Hold time, peripheral pin after H1 low					ns

NOTE 7: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



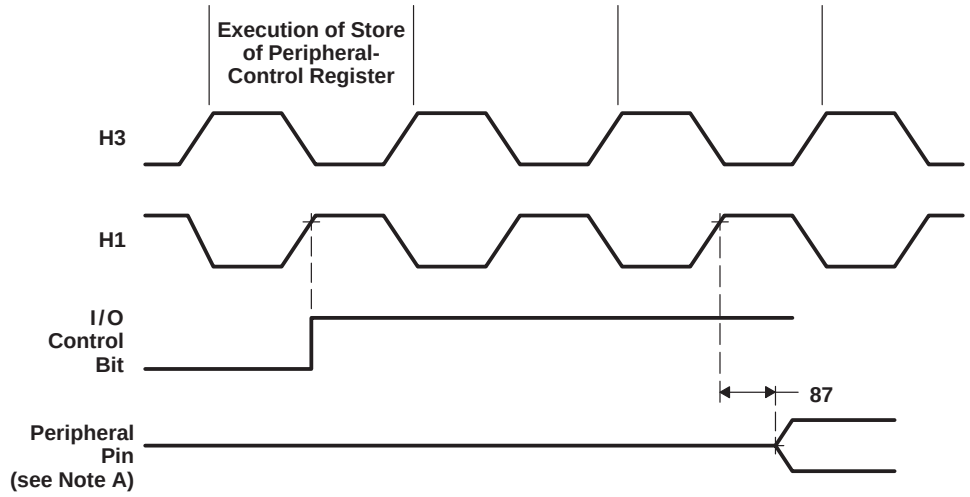
NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 22. Timing for Change of Peripheral Pin From General-Purpose Output to Input Mode

timing parameters for peripheral pin changing from general-purpose input to output mode (see Note 7 and Figure 23)

NO.			'VC33-120		'VC33-150		UNIT
			MIN	MAX	MIN	MAX	
87	$t_{d(H1H-GPIO)}$	Delay time, H1 high to peripheral pin switching from input to output					ns

NOTE 7: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 23. Timing for Change of Peripheral Pin From General-Purpose Input to Output Mode

timer pin timing

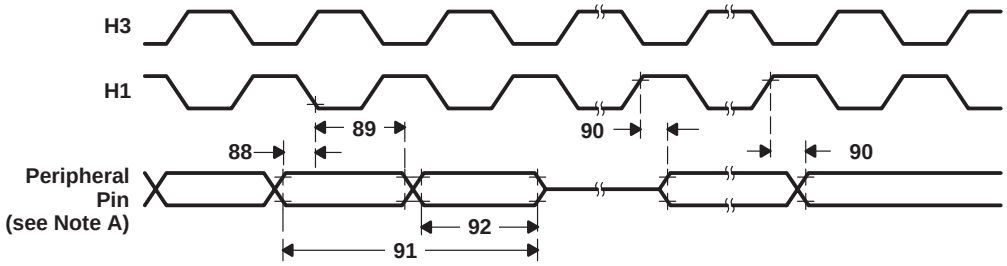
Valid logic-level periods and polarity are specified by the contents of the internal control registers.

The following tables define the timing parameters for the timer pin. The numbers shown in Figure 24 correspond with those in the NO. column of the tables below.

timing parameters for timer pin for TMS320VC33-120 (see Figure 24) †

NO.	DESCRIPTION‡		’VC33-120		’VC33-150		UNIT
			MIN	MAX	MIN	MAX	
88	$t_{su(TCLK-H1L)}$	Setup time, TCLK external before H1 low					ns
89	$t_{h(H1L-TCLK)}$	Hold time, TCLK external after H1 low					ns
90	$t_{d(H1H-TCLK)}$	Delay time, H1 high to TCLK internal valid					ns
91	$t_{c(TCLK)}$	TCLK ext					ns
		TCLK int					
92	$t_{w(TCLK)}$	TCLK ext					ns
		TCLK int					

† Timing parameters 88 and 89 are applicable for a synchronous input clock. Timing parameters 91 and 92 are applicable for an asynchronous input clock.



NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

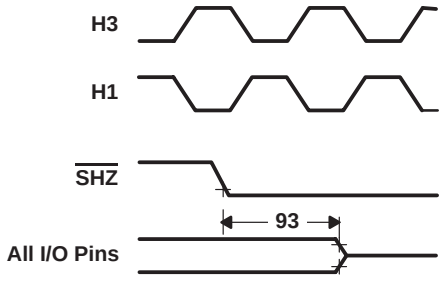
Figure 24. Timing for Timer Pin

$\overline{\text{SHZ}}$ pin timing

The following table defines the timing parameter for the $\overline{\text{SHZ}}$ pin. The number shown in Figure 25 corresponds with that in the NO. column of the table below.

timing parameters for $\overline{\text{SHZ}}$ (see Figure 25)

NO.			'VC33 MIN	'VC33 MAX	UNIT
93	$t_{dis(SHZ)}$	Disable time, $\overline{\text{SHZ}}$ low to all O, I/O pins disabled (high impedance)			ns



NOTE A: Enabling $\overline{\text{SHZ}}$ destroys TMS320C3x register and memory contents. Assert $\overline{\text{SHZ}}$ = 1 and reset the TMS320C3x to restore it to a known condition.

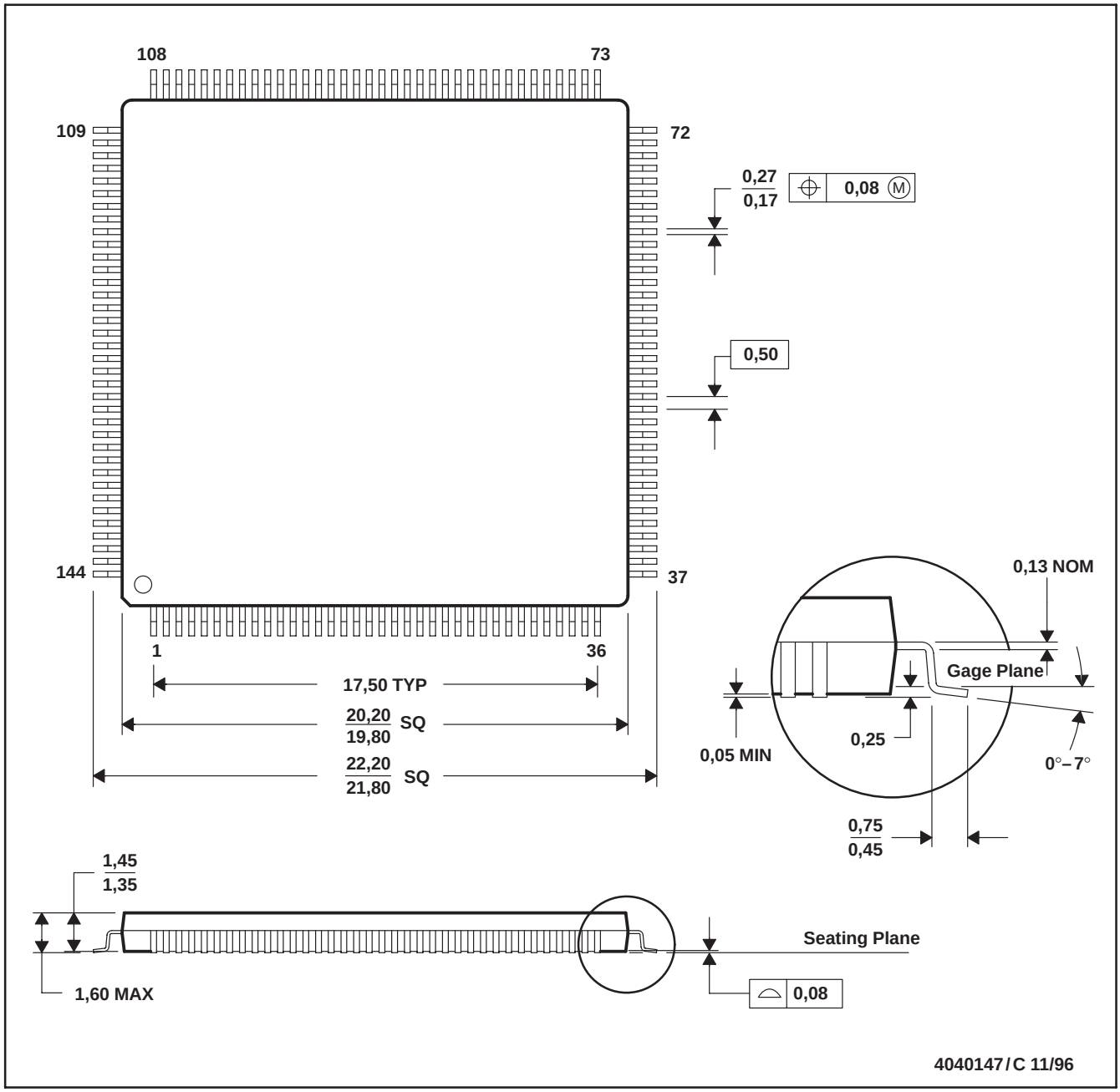
Figure 25. Timing for $\overline{\text{SHZ}}$

PRODUCT PREVIEW

MECHANICAL DATA

TMS320VC33 144-Pin Plastic Thin Quad Flatpack (TQFP)

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\Theta JA}$	56
$R_{\Theta JC}$	5

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