# MSM58321

## REAL TIME CLOCK/CALENDAR

### DESCRIPTION

The MSM 58321 is a metal gate CMOS Real Time Clock/Calendar with a battery backup function for use in bus-oriented microprocessor applications.
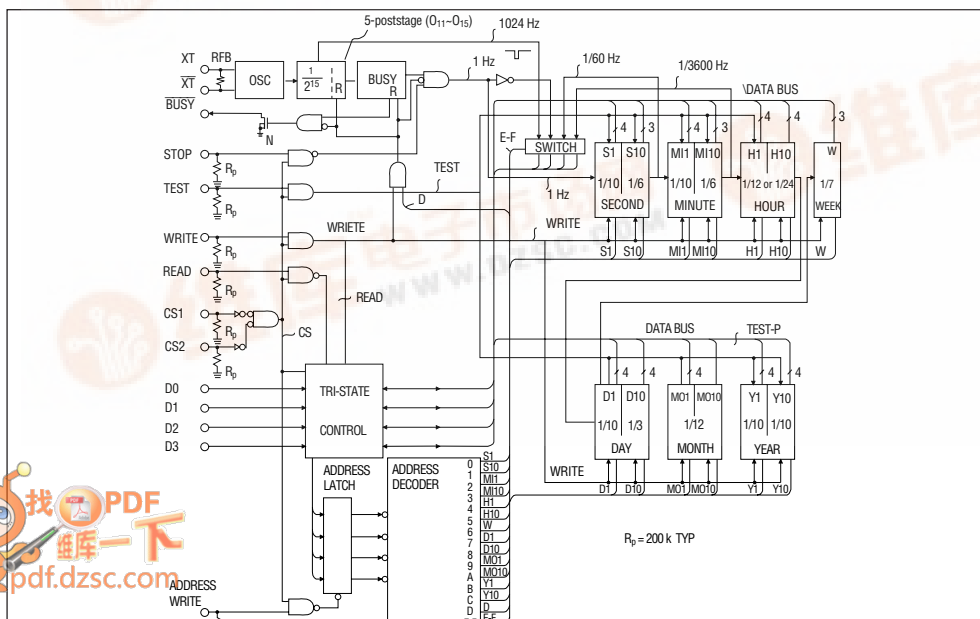
The 4-bit bidirectional bus line method is used for the data I/O circuit; the clock is set, corrected, or read by accessing the memory.

The time is read with 4-bit DATA I/O, AD-DRESS WRITE, READ, and $\overline{BUSY}$; it is written with 4-bit DATA I/O, ADDRESS WRITE, WRITE, and $\overline{BUSY}$.
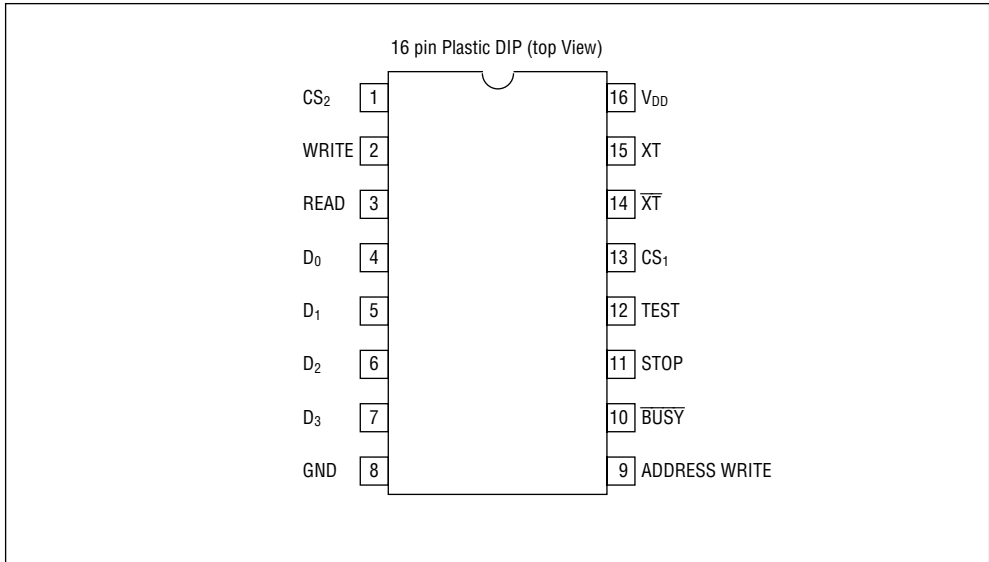
### FEATURES

- 7 Function-Second, Minute, Hour, Day, Day-of-Week, Month, Year
- Automatic leap year calender
- 12/24 hour format
- Frequency divider 5-poststage reset
- Reference signal output

- 32.768 kHz crystal controlled operation
- Single 5V power supply
- Back-up battery operation to $V_{DD}$ = 2.2V
- Low power dissipation
   90 µW max. at $V_{DD}$ = 3V
   2.5 mW max. at $V_{DD}$ = 5V
- 16 pin plastic DIP (DIP 16-P-300)

### FUNCTIONAL BLOCK DIAGRAM

# PIN CONFIGURATION

16 pin Plastic DIP (top View)

| | | | |
|---|---|---|---|
| $CS_2$ | 1 | 16 | $V_{DD}$ |
| WRITE | 2 | 15 | XT |
| READ | 3 | 14 | $\overline{XT}$ |
| $D_0$ | 4 | 13 | $CS_1$ |
| $D_1$ | 5 | 12 | TEST |
| $D_2$ | 6 | 11 | STOP |
| $D_3$ | 7 | 10 | $\overline{BUSY}$ |
| GND | 8 | 9 | ADDRESS WRITE |

# REGISTER TABLE

| Address | Address input | | | | Register Name | Data input/ output | | | | Count value | | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $D_0$ $(A_0)$ | $D_1$ $(A_1)$ | $D_2$ $(A_2)$ | $D_3$ $(A_3)$ | | $D_0$ | $D_1$ | $D_2$ | $D_3$ | | | | |
| 0 | 0 | 0 | 0 | 0 | $S_1$ | * | * | * | * | 0 | to | 9 | |
| 1 | 1 | 0 | 0 | 0 | $S_{10}$ | * | * | * | | 0 | to | 5 | |
| 2 | 0 | 1 | 0 | 0 | $MI_1$ | * | * | * | * | 0 | to | 9 | |
| 3 | 1 | 1 | 0 | 0 | $MI_{10}$ | * | * | * | | 0 | to | 5 | |
| 4 | 0 | 0 | 1 | 0 | $H_1$ | * | * | * | * | 0 | to | 9 | |
| 5 | 1 | 0 | 1 | 0 | $H_{10}$ | * | * | * | ⊙ | 0~1 or 0~2 | | | D2 = 1 specifies PM, D2 = 0 specifies AM, D3 = 1 specifies 24-hour timer, and D3 = 0 specifies 12-hour timer. When D3 = 1 is written, the D2 bit is reset inside the IC. |
| 6 | 0 | 1 | 1 | 0 | W | * | * | * | | 0 | to | 6 | |
| 7 | 1 | 1 | 1 | 0 | $D_1$ | * | * | * | * | 0 | to | 9 | |
| 8 | 0 | 0 | 0 | 1 | $D_{10}$ | * | * | ⊙ | ⊙ | 0 | to | 3 | The D2 and D3 bits in D10 are used to select a leap year. |
| 9 | 1 | 0 | 0 | 1 | $MO_1$ | * | * | * | * | 0 | to | 9 | |
| A | 0 | 1 | 0 | 1 | $MO_{10}$ | * | | | | 0 | to | 1 | |
| B | 1 | 1 | 0 | 1 | $Y_1$ | * | * | * | * | 0 | to | 9 | |
| C | 0 | 0 | 1 | 1 | $Y_{10}$ | * | * | * | * | 0 | to | 9 | |
| D | 1 | 0 | 1 | 1 | | | | | | | | | A selector to reset 5 poststages in the $1/2^{15}$ frequency divider and the BUSY circuit. They are reset when this code is latched with ADDRESS LATCH and the WRITE input goes to 1. |
| E–F | 0/1 | 1 | 1 | 1 | | | | | | | | | A selector to obtain reference signal output. Reference signals are output to D0 – D3 when this code is latched with ADDRESS LATCH and READ input goes to 1. |

Leap year table (Remarks for addresses 8–C):

| Calendar | $D_2$ | $D_3$ | Remainder obtained by dividing the year number by 4 |
|---|---|---|---|
| Gregorian calendar | 0 | 0 | 0 |
| | 1 | 0 | 3 |
| | 0 | 1 | 2 |
| | 1 | 1 | 1 |

**Note:**

(1) There are no bits in blank fields for data input/output. 0 signals are output by reading and data is not stored by writing because there are no bits.

(2) The bit with marked ⊙ is used to select the 12/24-hour timer and the bits marked ⊙ are used to select a leap year. These three bits can be read or written.

(3) When signals are input to bus lines D0 – D3 and ADDRESS WRITE goes to 1 for address input, ADDRESS information is latched with ADDRESS LATCH.

# ELECTRICAL CHARACTERISTICS
## Absolute Maximum Ratings

| Rating | Symbol | Condition | Value | Unit |
|---|---|---|---|---|
| Power voltage | $V_{DD}$ | Ta = 25°C | −0.3 to 6.5 | V |
| Input voltage | $V_I$ | Ta = 25°C | −0.3 to $V_{DD}$+0.3 | V |
| Output voltage | $V_O$ | Ta = 25°C | −0.3 to $V_{DD}$+0.3 | V |
| Storage temperature | $T_{stg}$ | − | −55 to +150 | °C |

## Operating Conditions

| Rating | Symbol | Condition | Value | Unit |
|---|---|---|---|---|
| Power voltage | $V_{DD}$ | − | 4.5 to 6 | V |
| Date hold voltage | $V_{DH}$ | − | 2.2 to 6 | V |
| Crystal frequency | $f(XT)$ | − | 32.768 | kHz |
| Operating temperature | $T_{OP}$ | − | −30 to +85 | °C |

**Note:**   The data hold voltage guarantees the clock operations, though it does not guarantee operations outside the IC and data input/output.

## DC Characteristics

$(V_{DD} = 5V \pm 5\%, Ta = -30 \sim +85°C)$

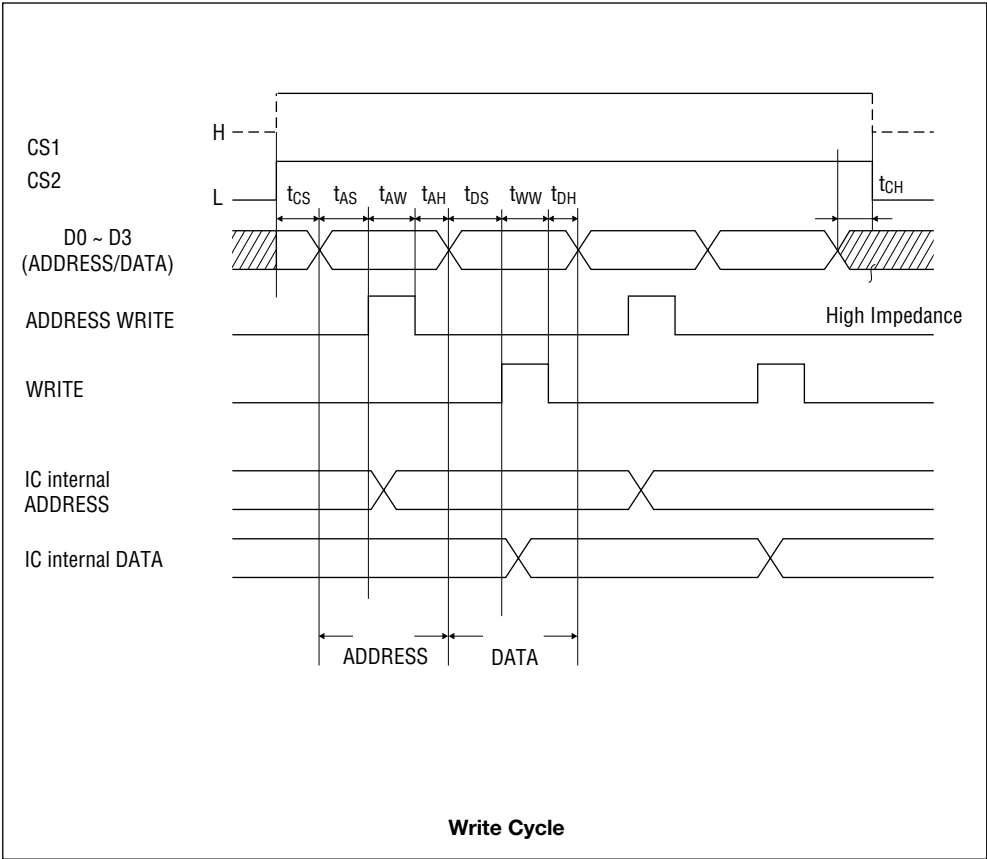| Rating | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| H input voltage | $V_{IH1}$ | − Note 1 | 3.6 | − | − | V |
|  | $V_{IH2}$ | − Note 2 | $V_{DD}$−0.5 | − | − |  |
| L input voltage | $V_{IL}$ | − | − | − | 0.8 | V |
| L output voltage | $V_{OL}$ | $I_O$ = 1.6 mA | − | − | 0.4 | V |
| L output current | $I_{OL}$ | $V_O$ = 0.4 V | 1.6 | − | − | mA |
| H input current | $I_{IH1}$ | $V_I$ = $V_{DD}$ Note3 | 10 | 30 | 80 | µA |
|  | $I_{IH2}$ | $V_I$ = $V_{DD}$ Note4 | − | − | 1 |  |
| L input current | $I_{IL}$ | $V_I$ = 0V | − | − | −1 | µA |
| Input capacity | $C_I$ | $f$ = 1 MHz | − | 5 | − | pF |
| Current consumption | $I_{DD}$ | $f$ = 32.768 kHz $V_{DD}$=5V/$V_{DD}$ = 3V | − | 100/15 | 500/30 | µA |

**Note:**   1. $CS_2$, WRITE, READ, ADDRESS WRITE, STOP, TEST, $D_0 \sim D_3$
2. $CS_1$
3. $CS_1$, $CS_2$, WRITE, READ, ADDRESS WRITE, STOP, TEST
4. $D_0 \sim D_3$

## Switching Characteristics

### (1) WRITE mode

$(V_{DD} = 5V \pm 5\%, Ta = 25°C)$

| Rating | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| CS setup time | $t_{CS}$ | – | 0 | – | – | µs |
| CS hold time | $t_{CH}$ | – | 0 | – | – | µs |
| Address setup time | $t_{AS}$ | – | 0 | – | – | µs |
| Address write pulse width | $t_{AW}$ | – | 0.5 | – | – | µs |
| Address hold time | $t_{AH}$ | – | 0.1 | – | – | µs |
| Data setup time | $t_{DS}$ | – | 0 | – | – | µs |
| Write pulse width | $t_{WW}$ | – | 2 | – | – | µs |
| Data hold time | $t_{DH}$ | – | 0 | – | – | µs |



**Write Cycle**

**Note:** ADDRESS WRITE and WRITE inputs are activated by the level, not by the edge.

## (2) READ mode

$(V_{DD} = 5V \pm 5\%, Ta = 25°C)$

| Rating | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| CS setup time | $t_{CS}$ | – | 0 | – | – | μs |
| CS hold time | $t_{CH}$ | – | 0 | – | – | μs |
| Address setup time | $t_{AS}$ | – | 0 | – | – | μs |
| Address write pulse width | $t_{AW}$ | – | 0.5 | – | – | μs |
| Address hold time | $t_{AH}$ | – | 0.1 | – | – | μs |
| Read access time | $t_{RA}$ | – | – | – | see Note 1 | μs |
| Read delay time | $t_{DD}$ | – | – | – | 1 | μs |
| Read inhibit time | $t_{RI}$ | – | 0 | – | – | μs |

**Note 1.**   $t_{RA} = 1 \text{ μs} + CR \ln \left( \dfrac{V_{DD}}{V_{DD} - V_{IH} \text{ min}} \right)$



**Read Cycle**

**Note:** ADDRESS WRITE and READ inputs are activated by the level, not by the edge.

## (3) WRITE & READ mode

($V_{DD}$ = 5V ±5%, Ta = 25°C)

| Rating | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| CS setup time | $t_{CS}$ | – | 0 | – | – | μs |
| CS hold time | $t_{CH}$ | – | 0 | – | – | μs |
| Address setup time | $t_{AS}$ | – | 0 | – | – | μs |
| Address write pulse width | $t_{AW}$ | – | 0.5 | – | – | μs |
| Address hold time | $t_{AH}$ | – | 0.1 | – | – | μs |
| Data setup time | $t_{DS}$ | – | 0 | – | – | μs |
| Write pulse width | $t_{WW}$ | – | 2 | – | – | μs |
| Data hold time | $t_{DH}$ | – | 0 | – | – | μs |
| Read access time | $t_{RA}$ | – | – | – | see Note 1 | μs |
| Read delay time | $t_{DD}$ | – | – | – | 1 | μs |
| Read inhibit time | $t_{RI}$ | – | 0 | – | – | μs |

**Note 1.**　　$t_{RA} = 1\ \mu s + CR \ln \left( \dfrac{V_{DD}}{V_{DD} - V_{IH}\ min} \right)$
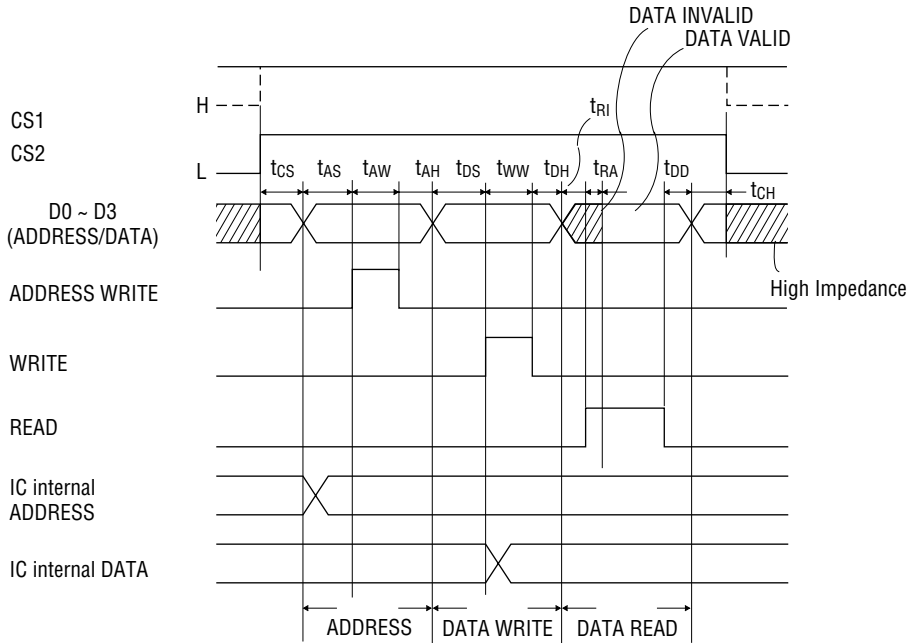


**Read & Write Cycle**

## PIN DESCRIPTION

| Name | Pin No. | Description |
|------|---------|-------------|
| CS$_2$ | 1 | Chip select pins.  These pins enable the interface with the external circuit when both of these pins are set at H level simultaneously. |
| CS$_1$ | 13 | If one of these pins is set at L level, STOP, TEST, WRITE, READ, ADDRESS WRITE pins and D$_0$ ~ D$_3$ pins are inactivated.<br>Since the threshold voltage VT for the CS$_1$ pin is higher than that for other pins, it shuold be connected to the detector of power circuit and peripherals and CS$_2$ is to be connected to the microcontroller. |
| WRITE | 2 | WRITE pin is used to write data; it is activated when it is at the H level.  Data bus data inside the IC is loaded to the object digit while this WRITE pin is at the H level, not at the WRITE input edge.  Refer to Figure 1 below. |
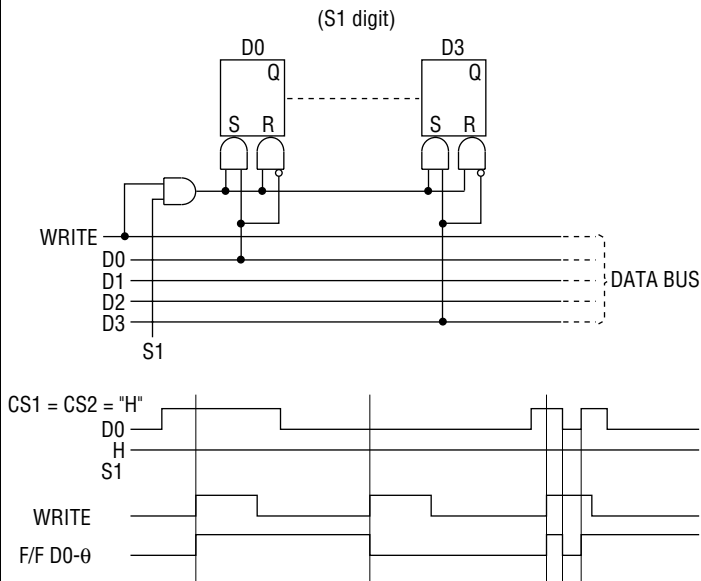


**Figure 1**

| Name | Pin No. | Description |
|------|---------|-------------|
| READ | 3 | READ pin is used to read data; it is activated when it is at the H level. Address contents are latched with ADDRESS LATCH inside the IC at the $D_0 \sim D_3$ and ADDRESS WRITE pins to select the object digit, then an H-level signal is input to the READ pin to read data.<br>If a count operation is continued by setting the STOP input to the L level, read operation must be performed, in principle, while the $\overline{BUSY}$ output is at the H level. While the $\overline{BUSY}$ output is at the L level, count operations are performed by digit counters and read data is not guaranteed, therefore, read operations are inhibited in this period. Figure 2 shows a time chart of the $\overline{BUSY}$ output, 1 Hz signal inside the IC, and READ input.<br>A read operation is stopped temporarily within a period of 244 µs from the $\overline{BUSY}$ output trailing edge and it is restarted when the $\overline{BUSY}$ output goes to the H level again. |
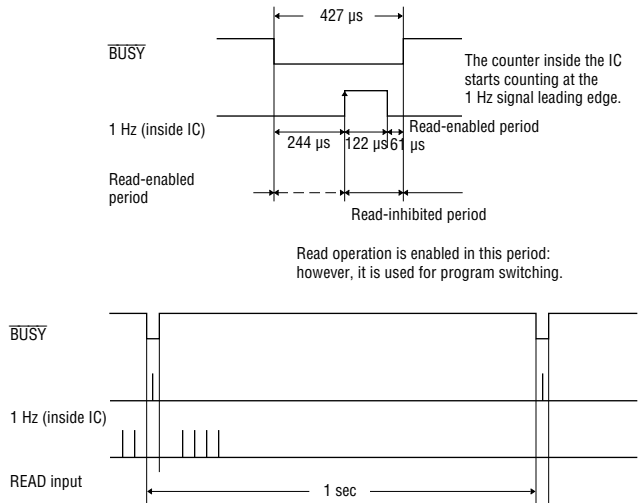


**Figure 2**

If the counter operation is stopped by setting the STOP input to the H level, read operations are enabled regardless of the $\overline{BUSY}$ output.
A read operation is enabled by microcomputer software regardless of the $\overline{BUSY}$ output during the counter operation by setting the STOP input to the L level.
In this method, read operations are performed two or more times continuously
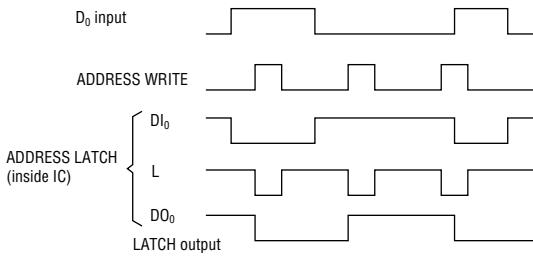
| Name | Pin No. | Description |
|------|---------|-------------|
| $D_0 \sim D_3$ | 4 ~ 7 | Data input/output pins. (Bidirectional bus). The output is a open-drain type and 4.7 kΩ ~ 10 kΩ pull-up registers are required utilize these pins as output pins. |
| GND | 8 | Ground pin. |
| ADDRESS WRITE | 9 | ADDRESS WRITE pin is used to load address information from the $D_0 \sim D_3$ I/O bus pins to the ADDRESS LATCH inside the IC; it is activated when it is at the H level. This input is activated by the level, not by the edge. Figure 3 shows the relationships between the $D_0$ address input, ADDRESS WRITE input, and ADDRESS LATCH input/output. <br><br>  <br> **Figure 3** |
| $\overline{\text{BUSY}}$ | 10 | $\overline{\text{BUSY}}$ pin outputs the IC operation state. It is N-channel MOSFET open-drain output. An external pull-up resistor of 4.6 kΩ or more must be connected (see Figure 4) to use the $\overline{\text{BUSY}}$ output. The signals are output in negative logics. If the oscillator oscillates at 32.768 kHz, the frequency is always 1 Hz regardless of the CS1 and CS2 unless the D output of the ADDRESS DECODER inside the IC is H (CODE = H•L•H•H) and CS1 = CS2 = WRITE = H. <br> Figure 5 shows the $\overline{\text{BUSY}}$ output time chart. <br><br>  <br> **Figure 4** <br><br>  <br> **Figure 5** |

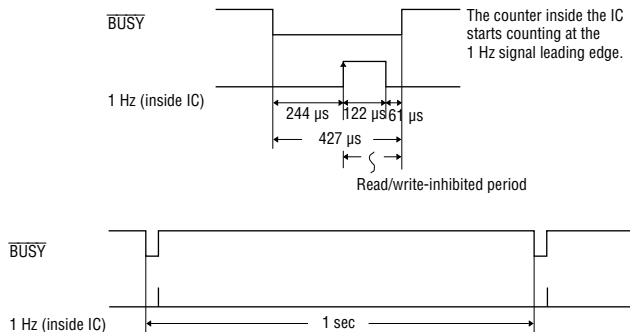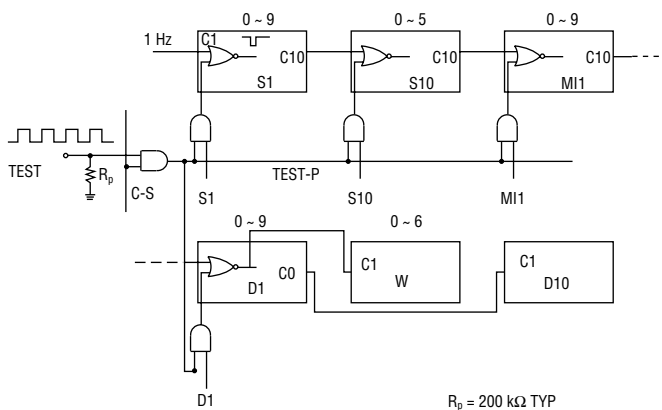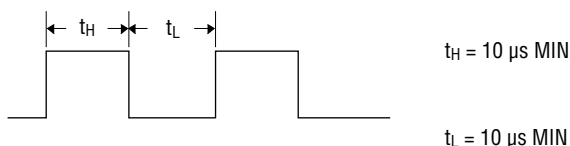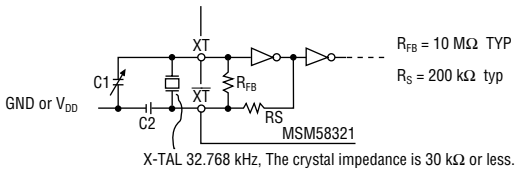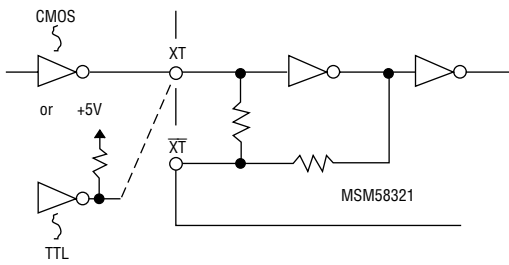| Name | Pin No. | Description |
|------|---------|-------------|
| STOP | 11 | The STOP pin is used to input on/off control for a 1 Hz signal. When this pin goes to the H level, 1 Hz signals are inhibited and counting for all digits succeeding the S1 digit is stopped. When this pin goes to the L level, normal operations are performed; the digits are counted up. This STOP input controls stopping digit counting. Writing of external data in digits can be assured by setting the STOP input to the H level to stop counting, then writing sequentially from the low-order digits. |
| TEST | 12 | The TEST pin is used to test this IC; it is normally open or connected to GND. It is recommended to connect it to GND to safeguard against malfunctions from noise.<br>The TEST pulse can be input to the following nine digits:<br>S1, S10, MI10, H1, D1 (W), M01, Y1 and Y10<br>When a TEST pulse is input to the D1 digit, the W digit is also counted up simultaneously.<br><br>Input a TEST pulse as follows:<br>Set the address to either digit explained above, then input a pulse to the TEST pin while CS1 = CS2 = STOP = H and WRITE = L. The specified and succeeding digits are counted up. (See Figure 6)<br><br>![Figure 6 circuit diagram]<br>**Figure 6**<br><br>A digit is counted up at the leading edge (changing point from L to H) of a TEST pin input pulse. The pulse condition for TEST pin input at $V_{DD}$ = 5V ±5% is described in Figure 7 below.<br><br>![Figure 7 timing diagram]<br>$t_H$ = 10 μs MIN<br>$t_L$ = 10 μs MIN |

| Name | Pin No. | Description |
|------|---------|-------------|
| $\overline{XT}$ | 14 | Oscillator pin.  A 32.768 kHz crystal oscillator, capacitor and trim capacitor for frequency adjustment are to be connected as shown in Figure 8 below. |
| XT | 15 | |



**Figure 8**

If an external clock is to be used for MSM58321's oscillation source, the external clock is to be input to XT, while $\overline{XT}$ should be left open.  Refer to the Figure 9 below.



**Figure 9**

## REFERENCE SIGNAL OUTPUT

Reference signals are output from the $D_0 \sim D_3$ pins under the following conditions:

| Conditions | Output pin | Reference signal frequency | Pulse width | Output logic |
|---|---|---|---|---|
| WRITE = L | $D_0$ | 1024 Hz | 488.3 μs | Pisitive logic |
| READ = H | $D_1$ | 1 Hz | 122.1 μs | Negative logic |
| CS1 = CS2 = H | $D_2$ | 1/60 Hz | 122.1 μs | Negative logic |
| ADDRESS = E or F | $D_3$ | 1/3600 Hz | 122.1 μs | Netgative logic |



$$122.1\ \mu s = \frac{10^{-3}}{32{,}768} \times 4$$

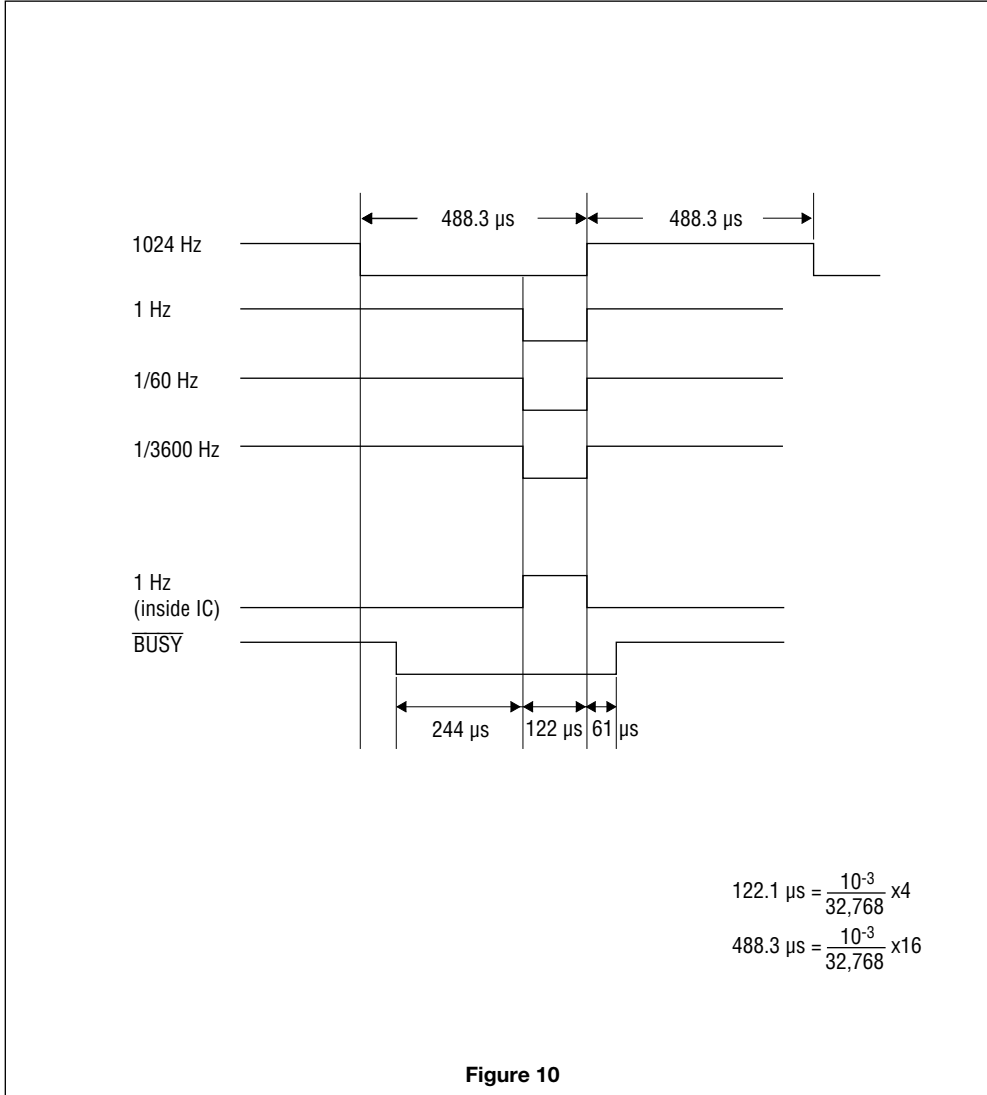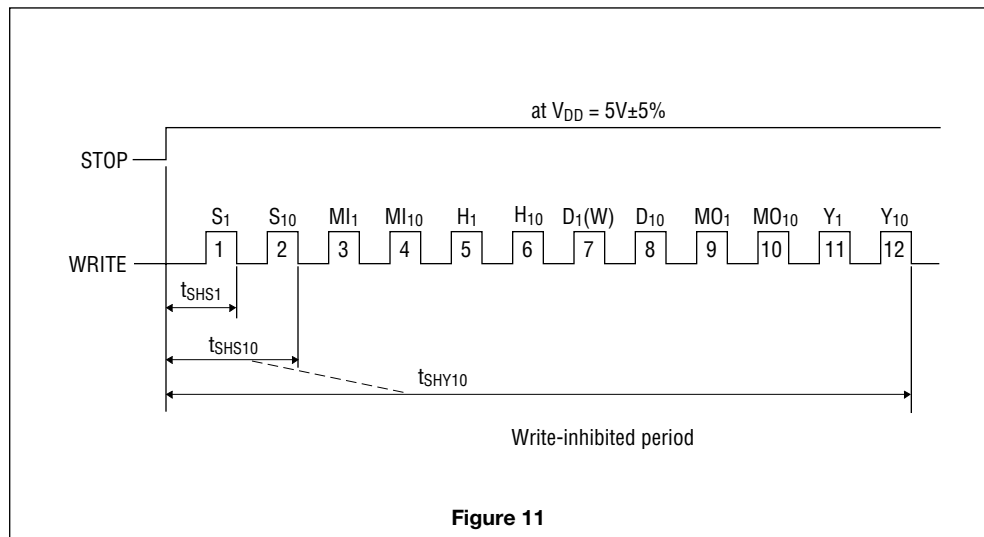$$488.3\ \mu s = \frac{10^{-3}}{32{,}768} \times 16$$

**Figure 10**

## APPLICATION NOTES

### WRITE and STOP

Note that the timing relationship between the STOP and WRITE inputs vary by the related digit when counting is stopped by the STOP input to write data. The time ($t_{SH}$) between the STOP input leading edge and WRITE input trailing edge for each digit is limited to the minimum value. (See Figure 11)



**Figure 11**

$t_{SHS1}$ = 1 μs, $t_{SHS10}$ = 2 μs, $t_{SHMI1}$ = 3 μs, $t_{SHMI10}$ = 4 μs, $t_{SHH1}$ = 5 μs
$t_{SHH10}$ = 6 μs, $t_{SHD1}$ = 7 μs, $t_{SHW}$ = 7 μs, $t_{SHD10}$ = 8 μs, $t_{SHMO1}$ = 9 μs
$t_{SHMO10}$ = 10 μs, $t_{SHY1}$ = 11 μs, $t_{SHY10}$ = 12 μs.

If a count operation is continued by setting the STOP input to the L level, write operation must be performed, in principle, while the $\overline{\text{BUSY}}$ output is at the H level. While the $\overline{\text{BUSY}}$ output is at the L level, count operations are performed by the digit counters and write operation is inhibited, but there is a marginal period of 244 µs from the $\overline{\text{BUSY}}$ output trailing edge. If the $\overline{\text{BUSY}}$ output goes to the L level during a write operation, the write operation is stopped temporarily within 244 µs and it is restarted when the $\overline{\text{BUSY}}$ output goes to the H level again. Figure 12 shows a time chart of $\overline{\text{BUSY}}$ output, 1 Hz signal inside the IC, and WRITE input.



**Figure 12**
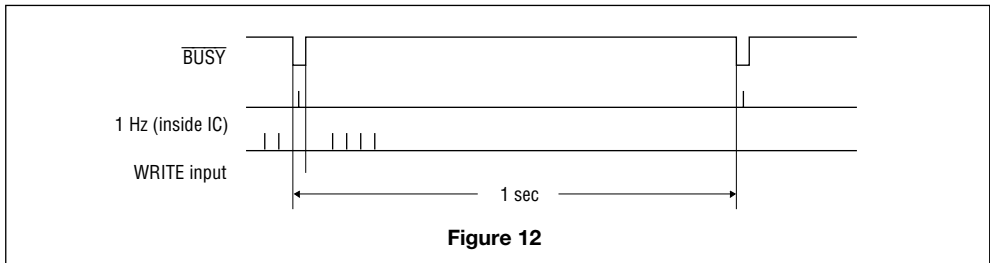
## Frequency divider and $\overline{\text{BUSY}}$ circuit reset

If A0 ~ A3 = H•L•H•H is input to ADDRESS DECODER, the DECODER output (D) goes to the H level. If CS1 = CS2 = H and WRITE = H in this state, the 5 poststage in the 15-stage frequency divider and the $\overline{\text{BUSY}}$ circuit are reset.

In this period, the $\overline{\text{BUSY}}$ output remains at the H level and the 1 Hz signal inside the IC remains at the L level, and counting is stopped. If this reset is inactivated while the oscillator operates, the $\overline{\text{BUSY}}$ output goes to the L level after 1000.1221 ±31.25 ms and the 1 Hz signal inside the IC goes to the H level after 1000.3663 ±31.25 ms. These times are not the same because the first ten stages in the 15-stage frequency divider are not reset. (See Figure 13)



**Figure 13**
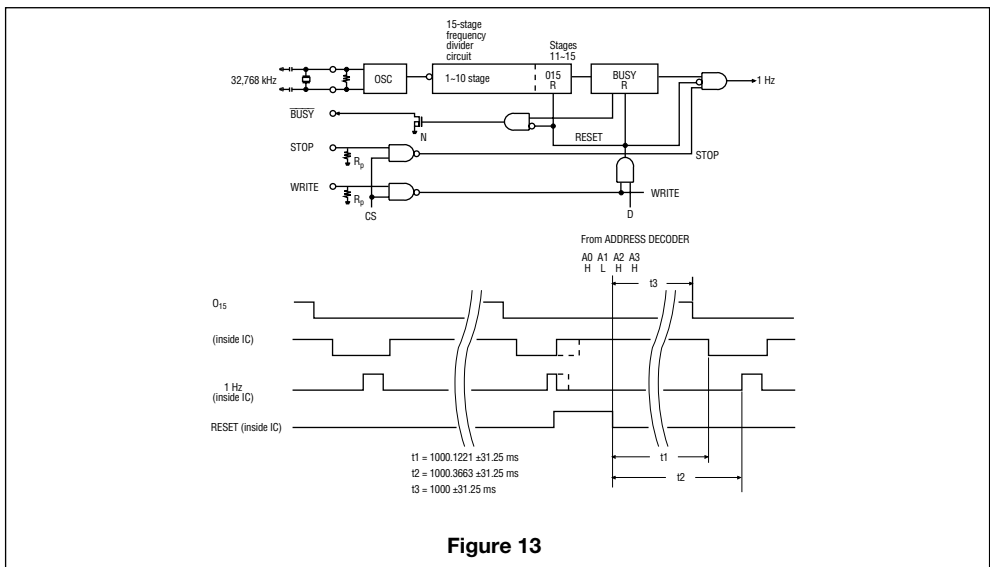
## Selection of leap year

This IC is designed to select leap year automatically.

Four types of leap years can be selected by writing a select signal in the D2 and D3 bits of the D10 digit (CODE = L•L•L•H).  (See table 1 for the functions.)

Gregorian calendar or other calendars can be set arbitrarily in the Y1 and Y10 digits of this IC.  There is a leap year every four years and the year number varies according to the calendar used.  There are four combinations of year numbers and leap years.  (See the Table below).

No. 1:  Gregorian calendar year.  The remainder obtained by dividing the leap year number by 4 is 0.
No. 2:  The remainder obtained by dividing the leap year number by 4 is 3.
No. 3:  The remainder obtained by dividing the leap year number by 4 is 2.
No. 4:  The remainder obtained by dividing the leap year number by 4 is 1.

| No.1 | Calendar | D10 digit | | Remainder obtained by dividing the leap year number by 4 | Leap years (examples) |
|------|----------|----|----|-------------------|------------------------|
|      |          | D2 | D3 |                   |                        |
| 1 | Gregorian | L | L | 0 | 1980, 1984, 1988, 1992 1996, 2000, 2004 |
| 2 |  | H | L | 3 | (83) (87) (91) (95) (99) 55, 59, 63, 67, 71, 75, 79 |
| 3 |  | L | H | 2 | 82, 86, 90, 94, 98, 102, 106 |
| 4 |  | H | H | 1 | 81, 85, 89, 93, 97, 101, 105 |

## APPLICATION EXAMPLE – POWER SUPPLY CIRCUIT



a)

| | |
|---|---|
| VF = 0.69V | Ripple |
| | Operating state | 20 mV P-P |
| | Backup | 0 mV |

b)

| | |
|---|---|
| VCE (Sat) = 0.1V | Ripple |
| | Operating state | 20 mV P-P |
| | Backup | 0 mV |

c)

d)