T-51-11-17

MOTOROLA
SEMICONDUCTORS
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

MC3419-1L

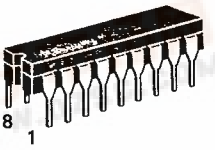
TELEPHONE LINE-FEED CIRCUIT

. . . designed as the heart of a circuit to provide BORSHT functions for telephone service in Central Office, PABX, and Subscriber Carrier equipment. This circuit provides dc power for the telephone (Battery), Overvoltage protection, Supervision features such as hook status and dial pulsing, two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input (Hybrid), and facilitates ringing insertion, Ring trip detection and Testing.

- Totally Upward Compatible with the MC3419
- All Key Parameters Externally Programmable
- Current Sensing Outputs Monitor Status of Both Tip and Ring Leads for Auxiliary Functions such as: Ground Key, Ring Trip, Message Waiting Lamp, etc.
- On-Hook Power Below 5.0 mW
- Digital Hook Status Output
- Powerdown Input
- Ground Fault Protection
- Operates from Single −20 V to −56 V Power Source
- Size and Weight Reduction Over Conventional Approaches
- The sale of this product is licensed under Patent No. 4,004,109. All royalties related to this patent are included in the unit price.

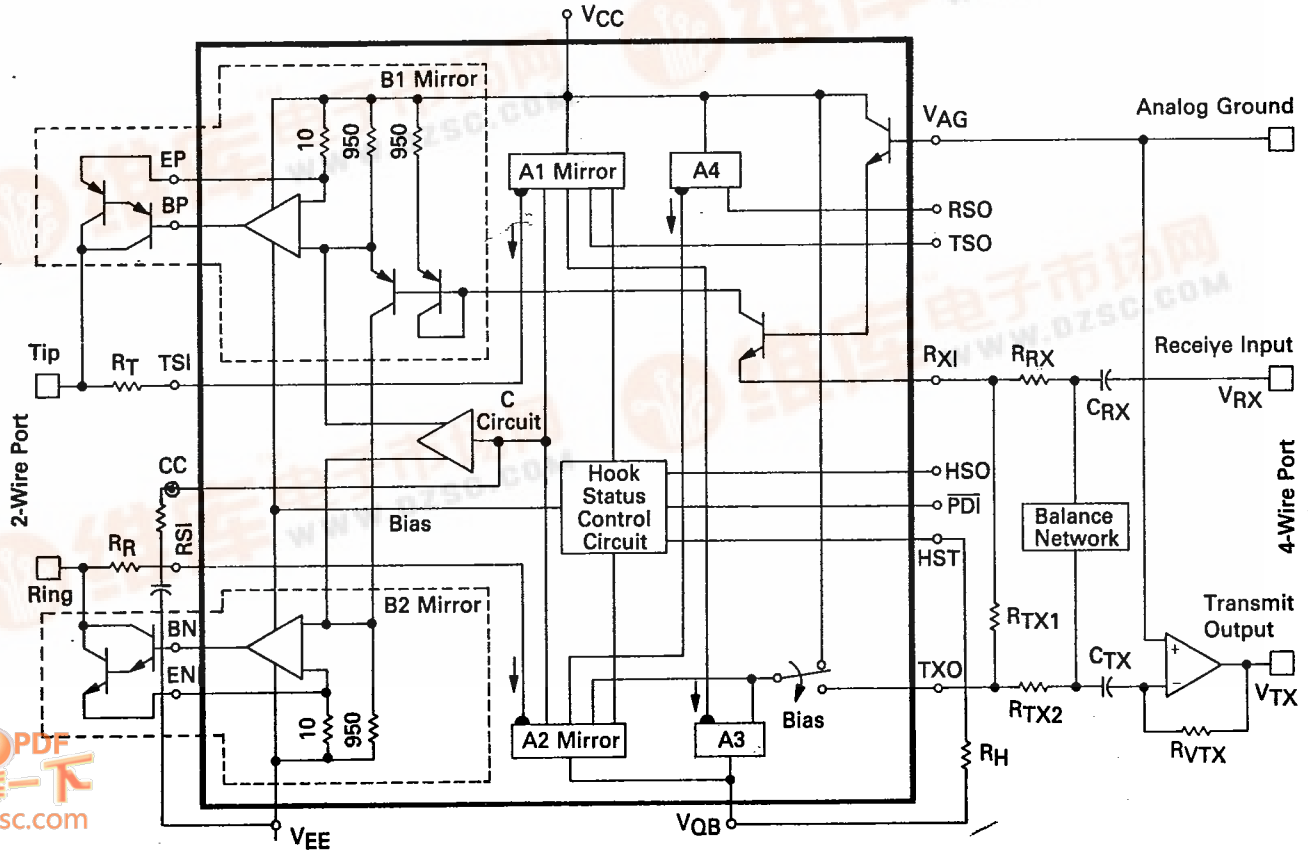
SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

BIPOLAR LASER-TRIMMED INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 726-04

FUNCTIONAL BLOCK DIAGRAM



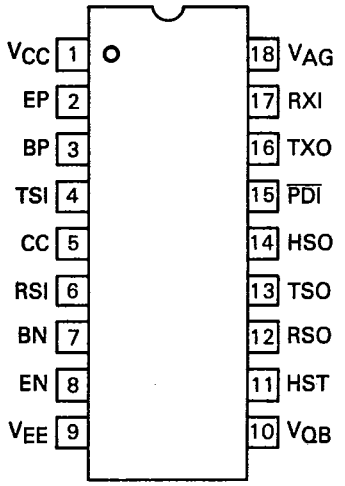
MAXIMUM RATINGS (Voltages Referenced to V_{CC}.)

Rating	Symbol	Value	Unit
Voltage	V_{EE} V_{QB}	−60 V_{EE} −1.0 V	Vdc
Powerdown Input Voltage Range	$V_{\overline{PDI}}$	+15 to −15	Vdc
Sense Current Steady State Pulse — Figure 4	I_{TSI}, I_{RSI}	 100 200	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature (θ_{JA} = 100°C/W Typ)	T_J	150	°C

OPERATING CONDITIONS (Voltages Referenced to V_{CC}.)

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70	°C
Loop Current	I_L	10 to 120	mA
Voltage	V_{EE} V_{QB}	−20 to −56 −20 to V_{EE}	Vdc
Analog Ground (I_L = 0 to 60 mA) (I_L = 0 to 120 mA)	V_{AG}	 0 to −12 −2.5 to −12	Vdc
Supervisory Output Voltage Compliance Range	V_{RSO}, V_{TSO}	−2.0 to −20	Vdc
Hook Status Output	V_{HSO}	+15 to −20	Vdc
Loop Resistance	R_L	0 to 2500	Ω

PIN CONNECTIONS



TRANSMISSION CHARACTERISTICS (R_L = 600 Ω unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Transmit and Receive Gain Variation (Insertion Loss) (1.0 kHz @ 0 dBm Input)	1	V_{TX}/V_L, V_L/V_{RX}	−0.3	0	+0.3	dB
Transhybrid Rejection (Input — 1.0 kHz @ 0 dBm) Fixed (1%) Resistor Balance Network Trimmed Balance Network All Types	1	V_{TX}/V_{RX}	 −23 —	 −35 −55	 — —	dB
Level Linearity (−48 to +3.0 dBm, referenced to 0 dBm @ 1.0 kHz) Transmission Reception	1	 V_{TX}/V_L V_L/V_{RX}	 −0.1 −0.1	 0 0	 +0.1 +0.1	dB
Frequency Response (200–3400 Hz referenced to 1.0 kHz @ 0 dBm) Transmission Reception	1	 V_{TX}/V_L V_L/V_{RX}	 −0.1 −0.1	 0 0	 +0.1 +0.1	dB
Total Distortion @ 1.0 kHz, 0 dBm (C-Message Filtered)	1	V_L/V_{RX} V_{TX}/V_L	— —	−60 −60	— —	dB

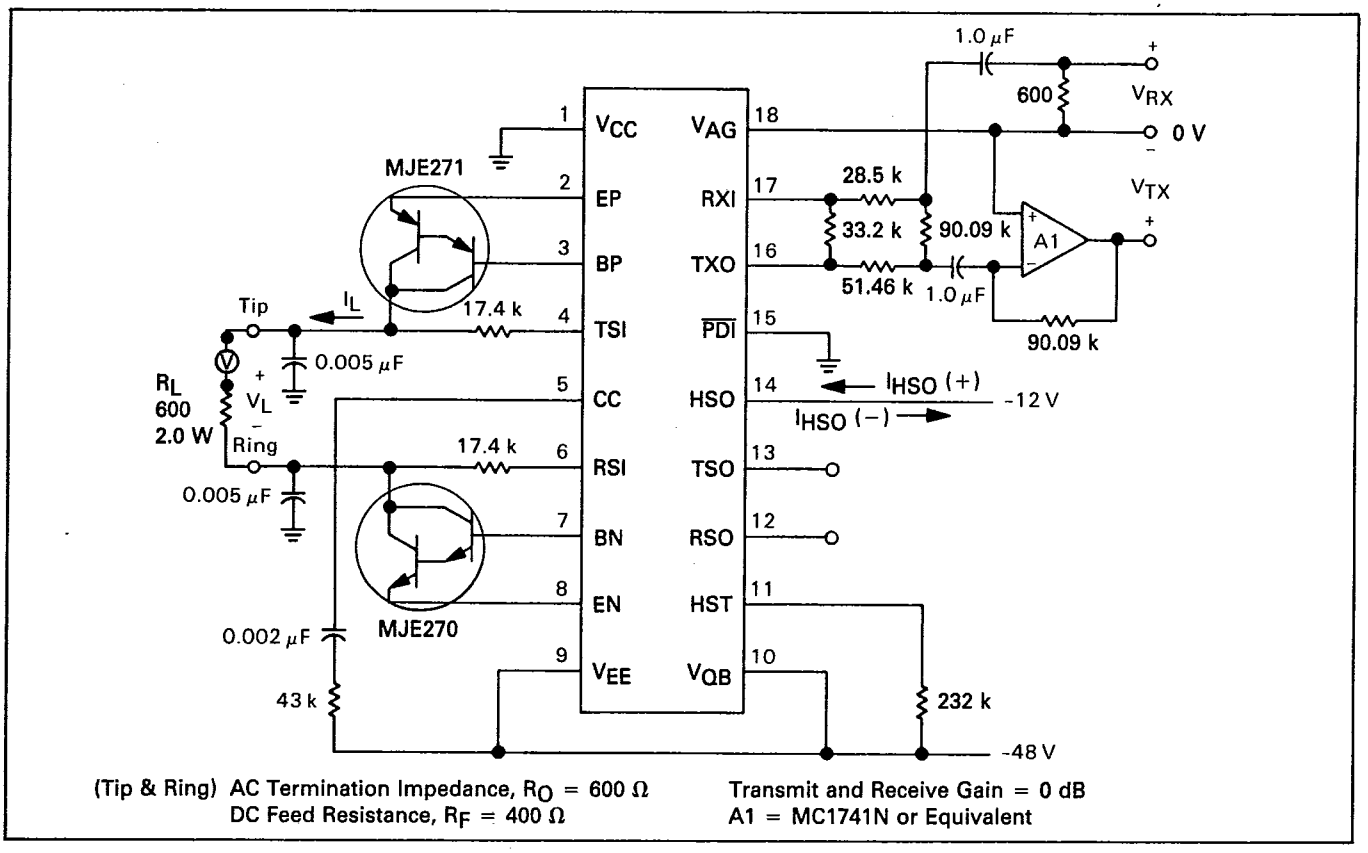
TRANSMISSION CHARACTERISTICS (continued) (R_L = 600 Ω unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Idle Channel Noise (V_{RX} = 0 V)	1	V_{TX}, V_L	—	3.0	10	dBrnC
Return Loss (referenced to 600 ohms) @ 1.0 kHz, 0 dBm	1	$20 \text{ Log } \left\lvert \frac{R_0 - 600}{R_0 + 600} \right\rvert$	30	—	—	dB
Longitudinal Induction (60 Hz) (I_{LON} = 35 mA RMS)	2	V_{TX}	—	5.0	—	dBrnC
Longitudinal Balance (200–3000 Hz)	2	V_{TX}/V_{LON}, V_L/V_{LON}	−45	—	—	dB

ELECTRICAL CHARACTERISTICS (V_{EE} = −48 V, V_{QB} = V_{EE}, V_{AG} = 0 V, R_L = 600 Ω, T_A = 25°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Propagation Delay	1	T_P, V_{RX} to V_L V_{RX} to I_{TX}	— —	750 1.2	— —	ns μs
Supply Current — On-Hook (V_{EE} = V_{QB} = 56 V, R_L > 100 MΩ)	3	I_{VCC}	—	40	200	μA
On-Hook Power Dissipation (R_L > 100 MΩ)	3	P_D	—	1.0	—	mW
Power Supply Noise Rejection (1.0 kHz @ 1.0 V_{RMS})	3	V_{TX}/V_{ee}	−40	—	—	dB
Quiet Battery Noise Rejection (1.0 kHz @ 1.0 V_{RMS})	3	V_{TX}/V_{qb}	—	−6.0	—	dB
Sense Current Tip Ring	4	 I_{TSO}/I_{TSI} I_{RSO}/I_{RSI}	 0.15 0.15	 0.17 0.17	 0.19 0.19	mA/mA
Fault Currents Tip to V_{CC} Ring to V_{CC} Tip to Ring Tip and Ring to V_{CC}	1	 I_{Tip} I_{Ring} I_{Loop} I_{Tip} and I_{Ring}	 — — — —	 0 2.5 120 2.5	 — — — —	mA
Analog Ground Current	1	I_{VAG}	—	0.1	2.0	μA
Powerdown Logic Levels		$I_{\overline{PDI}}$ V_{IH} V_{IL}	— −1.2 —	−1:0 — —	−10 — −4.0	μA Vdc Vdc
Hook Status Output Current (R_L < 2.5 kΩ, V_{HSO} = +0.4 Vdc) V_{HSO} = −0.4 Vdc) (R_L > 10 kΩ, V_{HSO} = +12 Vdc) V_{HSO} = −12 Vdc)	1	I_{HSO}	 +1.0 −0.4 — —	 +3.0 −1.5 0 0	 — — +50 −2.0	 mA mA μA μA

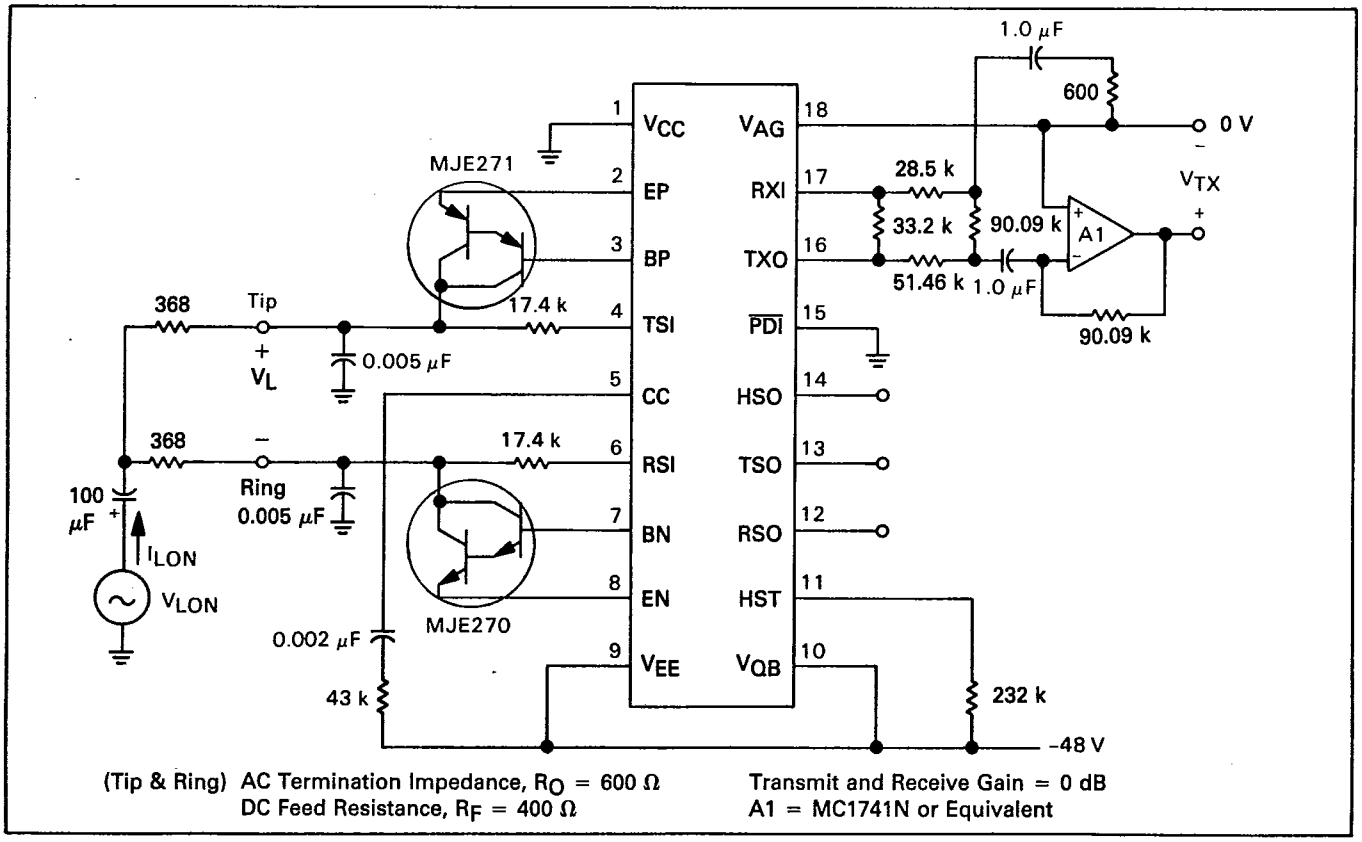
FIGURE 1 — AC TEST CIRCUIT



(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

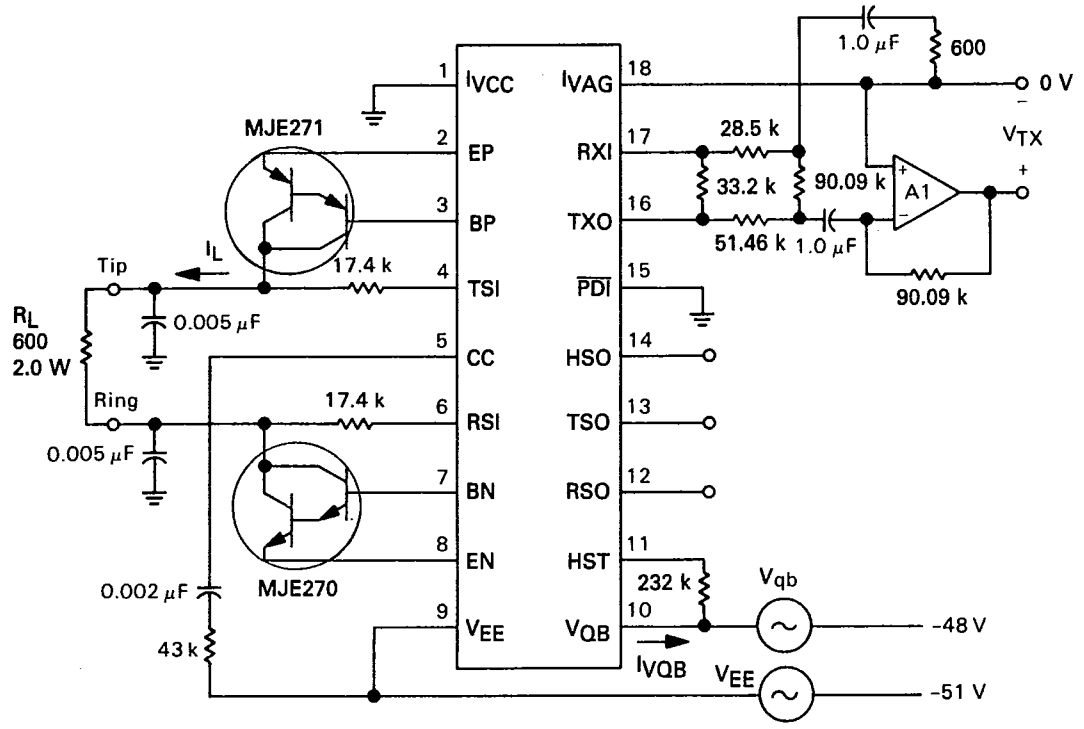
FIGURE 2 — LONGITUDINAL BALANCE TEST CIRCUIT



(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

FIGURE 3 — SUPPLY NOISE REJECTION TEST CIRCUIT



(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

FIGURE 4 — TSO AND RSO SUPERVISORY OUTPUT TEST CIRCUIT

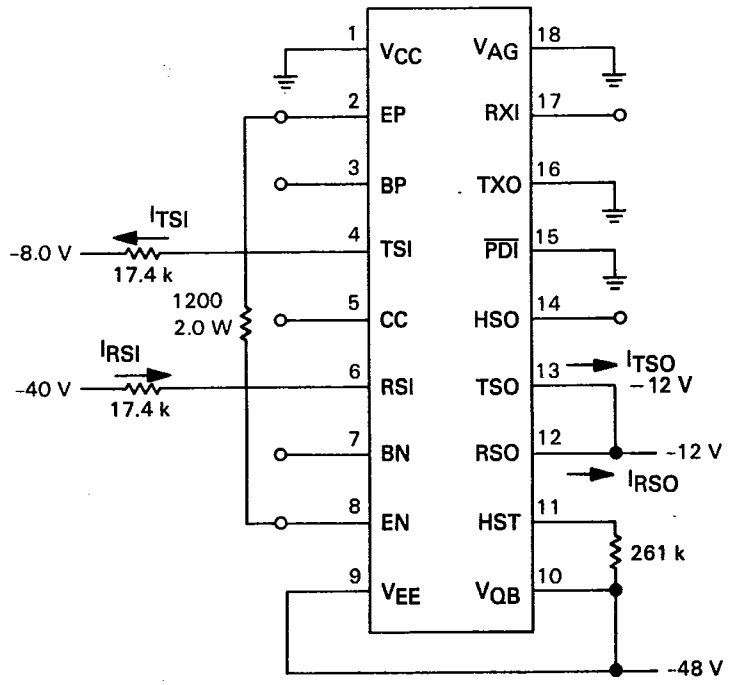


FIGURE 5 — QUIET BATTERY CURRENT I_{VQB} versus LOOP CURRENT I_L

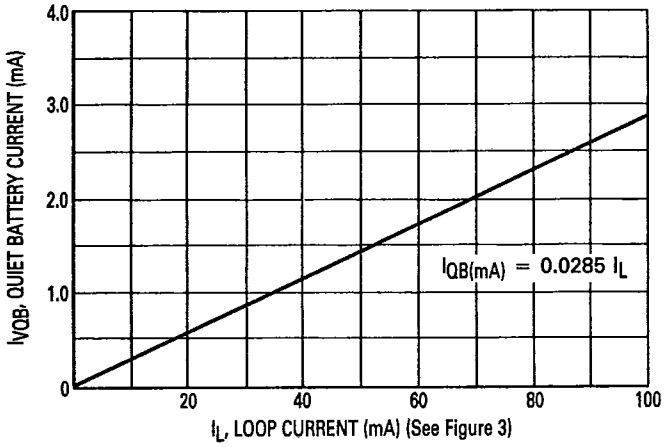
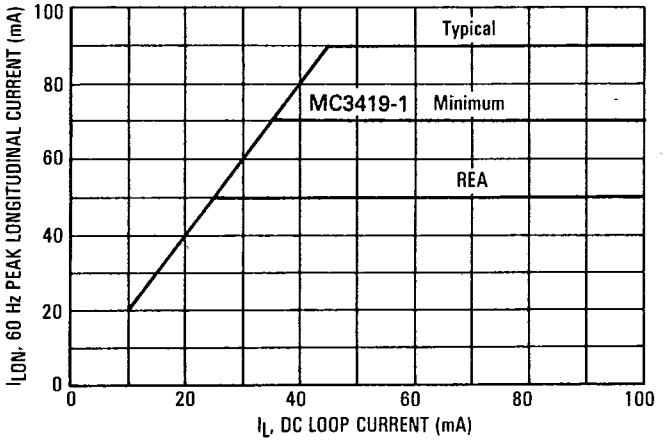
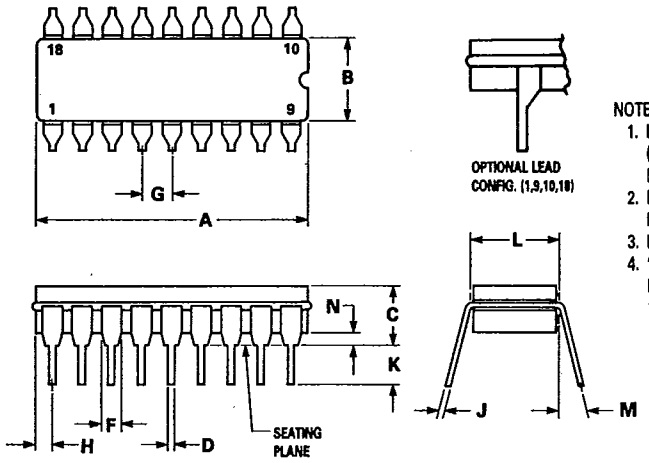


FIGURE 6 — LONGITUDINAL CAPACITY



OUTLINE DIMENSIONS



NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

CASE 726-04

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

PIN DESCRIPTIONS

Pin	Name	Function
1	V_{CC}	The positive supply voltage. This point is ground in typical applications.
2, 8	EP & EN	Loop current sensing inputs. These are connected to the emitters of the PNP and NPN Darlington transistors. They are tied through 10 Ω resistors to V_{CC} and V_{EE}, respectively. The maximum continuous current through these inputs is 240 mA.
3, 7	BP & BN	Base drive outputs. These pins drive the bases of the PNP and NPN transistors and are able to sink or source, respectively, up to 5.0 mA.
4, 6	TSI & RSI	Tip and Ring voltage Sensing Inputs. They are low impedance inputs (approximately 600 Ω each i.e., 400 Ω + 3 diodes) that translate the voltages on Tip and Ring to a current through resistors R_T and R_R. TSI is referenced to V_{CC} and RSI is referenced to V_{QB}. These pins have 6.0 V zener diodes (to their respective reference) for protection against overvoltage line surges.
5	CC	Compensation Capacitor pin. This pin is used to stabilize the longitudinal or common mode circuitry.
9	V_{EE}	Negative supply voltage. This pin ties to the chip substrate. Its operating voltage range is −20 V to −56 V. It can withstand −60 V without damage and can sustain a voltage surge to −75 V for less than 4.0 ms without significant degradation of performance. Most of the loop current and bias currents flow through this pin.
10	V_{QB}	Quiet Battery Voltage reference. This is the voltage reference for the RSI pin. Its voltage must not go more negative than V_{EE}. The current through this pin, while powered up, is proportional to the loop current, allowing it to be used for loop current limiting. The voltage on this pin, less 4 volts, is the "effective battery feed voltage for the 2-wire lines even though most of the power comes from the V_{EE} supply.
11	HST	Hook Status Threshold programming resistor input. R_H determines the value of loop resistance at which on-hook and off-hook status is switched.
12	RSO	Ring Sense current Output. This output reflects the voltage status of the Ring terminal for voltages more positive than V_{QB}. The current is sourced from this output, it is one-sixth I_{RSI}, its voltage range is 0 to −20 V and its saturation voltage is approximately −2.0 V.
13	TSO	Tip Sense current Output. This output reflects the voltage status of the Tip terminal for voltages more negative than V_{CC}. The current is sourced from this output, it is one-sixth I_{TSI}, its voltage range is 0 V to −20 V and its saturation voltage is approximately −2.0 V.
14	HSO/$\overline{\text{HSO}}$	Hook Status Output. This is a digital output that reflects the condition of the loop resistance. If loop resistance is less than a predetermined value established by R_H, usually $R_L < 2.5$ kΩ, the HSO pin will be active, i.e., with positive voltage logic (a resistor tied from a +5.0 V or +12 V supply to HSO), this pin will sink current to V_{CC} ($V_{HSO} \cong 0$ V); with negative voltage logic (a resistor tied from a −12 V supply to HSO), this pin will source current from V_{CC} ($V_{HSO} \cong 0$ V). If loop resistance is greater than a predetermined value again established by the same resistor R_H, usually $R_L > 10$ kΩ, the HSO pin is inactive, i.e., V_{HSO} = logic supply voltage.
15	$\overline{\text{PDI}}$	Powerdown Input pin. This pin is used to deny service to the subscriber. A logic level "0" ($V_{IL} <$ −4.0 V) powers down the MC3419-1 except for HSO, TSO and RSO. The voltage range of this high impedance input pin is ±15 V.
16	TXO	Transmit current Output. This output sinks current to V_{QB} and is proportional to $I_{TSI} + I_{RSI}$ by a ratio of K1 where: K1 = 0.51. Its saturation voltage is V_{QB} + 2.5 V typ. (+3.5 V over the temperature range). This pin is only active during the off-hook power-up condition.
17	RXI	Receive Input. This input sums ac currents from TXO and the receive voltage input (V_{RX}) and sources all the dc current to TXO. It has a low input impedance (15 Ω) typically biased 4.5 V below the V_{AG} pin voltage during off-hook power-up conditions. During powerdown conditions, the voltages on RXI and TXO can drift up to V_{AG}.
18	V_{AG}	Analog Ground Voltage reference input. The input impedance of this pin is much greater than 1.0 MΩ. It should be ac coupled to system ground and could be direct coupled if system ground is between 0 V and −12 V. AC coupling requires 300 kΩ to V_{CC} and 0.1 μF to system ground. If V_{CC} and system ground are common, tie V_{AG} directly to V_{CC}. If dc loop currents are allowed to go higher than 60 mA, V_{AG} should be biased from −2.5 V to −12 V to avoid problems at high ambient temperatures.

FUNCTIONAL DESCRIPTION

Referring to the functional block diagram on page 1, line sensing resistors (R_R and R_T) at the TSI and RSI pins convert voltages at the Tip and Ring terminals into currents which are fed into current mirrors* A1 and A2. An output of A1 is mirrored by A3 and summed together with an output of A2 at the TXO terminal. Thus, a differential to single-ended conversion is performed from the ac line signals to the TXO output.

All the dc current at the TXO output is fed back through the RXI terminals to the B1 mirror input. The inputs to B1 and B2 are made equal by mirroring the B1 input current to the B2 input through a unity gain output of the B1 mirror. Both B1 and B2 mirrors have high gain outputs (x95) which drive the subscriber lines with balanced currents that are equal in amplitude and 180° out of phase. The feedback from the TXO output, through the B-Circuit mirrors, to the subscriber line produces a dc feed resistance significantly less, but proportional to the loop sensing resistors.

In most line-interface systems, the ac termination impedance is desired to be greater than the dc feed impedance. A differential ac generator on the subscriber loop would be terminated by the dc feed impedance if the total ac current at the TXO output were returned to the B1 input along with the dc current. Instead, the MC3419-1 system diverts part of the ac current from the B-Circuit mirrors. This decreases the ac feedback current, causing the ac termination impedance at the line interface to be greater than the dc feed impedance.

The ac current that is diverted from the B1 mirror input is coupled to a current-to-voltage converter circuit that has a low input impedance. This circuit consists of an op amp (external to the MC3419-1) and a feedback resistor which produces the transmit output voltage (V_{TX}) at the 4-wire interface. Transmission gain is programmed by the op amp feedback resistor (R_{VTX}).

Reception gain is realized by converting the ac coupled receive input voltage (V_{RX}) to a current through an external resistor (R_{RX}) at the low impedance RXI terminal. This current is summed at RXI with the dc and ac feedback current from the A-Circuit mirrors and drives the B1 mirror input. The B-Circuit mirror outputs drive the 2-wire port with balanced ac current proportional to the receive input voltage. Reception gain is programmed by the R_{RX} resistor.

Since receive input signals are transmitted through the MC3419-1 to the 2-wire port, and the 2-wire port signals are returned to the 4-wire transmit output, a means of cancellation must be provided to maintain 4-wire signal separation (transhybrid rejection). Cancellation is complicated because the gain from the receive port to the transmit port depends on the impedance of the subscriber loop. A passive "balance network" is used to achieve transhybrid rejection by cancelling, at the low impedance input to the transmit op amp, the current reflected by the loop impedance to the 4-wire transmit output. For a resistive loop impedance, a single resistor provides the cancellation. For reactive loops, the balance network should be reactive.

Longitudinal (common-mode) currents that may be present on the subscriber lines are suppressed in the MC3419-1 by two methods. The first is inherent in the mirror configuration. Positive-going longitudinal currents into Tip and Ring create common-mode voltages that cause a decreasing current through the Tip Sensing resistor and an increasing current through the Ring Sensing resistor. When these equal and opposite signal currents are reflected through the A-Circuit mirrors and summed together at TXO, the total current at TXO remains unchanged. Therefore, the ac currents due to the common-mode signal are cancelled before reaching the transmit output.

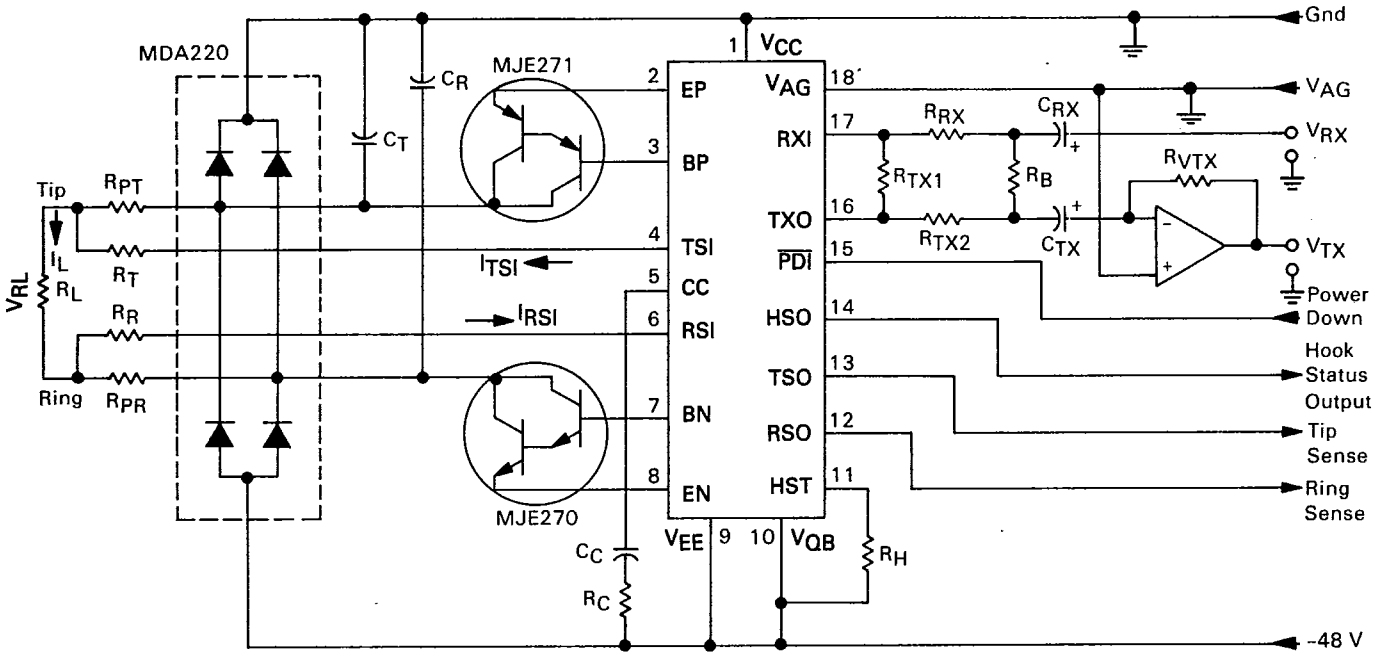
The second longitudinal suppression method is more dominant, since it limits the amplitude of common-mode voltages that appear at the Tip and Ring terminals.

A common-mode suppression circuit detects common-mode inputs and drives the loop with balanced currents to reduce the input amplitude. Subtracting currents from outputs of the A1 and A2 mirrors produces a signal current at the CC terminal in response to the common-mode voltage at Tip and Ring. A transconductance amplifier (C-Circuit) generates a current proportional to the CC terminal voltage which is summed with the current from the RXI terminal at the inputs of current mirrors B1 and B2. The weighting and polarity of the summing networks produce common-mode B1 and B2 mirror output currents at the 2-wire port. The common-mode input impedance is inversely proportional to the gain of the longitudinal suppression circuit. R_C and C_C compensate the common-mode feedback loop. At 60 Hz with typical component values, the 2-wire common-mode impedance is less than 5 Ω.

The longitudinal suppression circuit output currents are generated by modulating dc current fed to the loop by the B1 and B2 current mirrors. This configuration avoids the increased power dissipation attributed to current mode loop drive because dc and longitudinal currents are not cumulatively sourced to the loop. However, driving common-mode currents through the B-circuit current mirrors in this manner limits the longitudinal suppression capability. The suppression circuit is unable to reverse 2-wire current polarities to maintain a low-impedance termination when longitudinal currents exceed the dc loop current. At low dc loop currents, the common-mode signal capability, known as longitudinal capacity, is limited by the loop current (Figure 6). At high-loop currents, longitudinal capacity is limited by the maximum voltage swing of the CC terminal and is therefore independent of dc loop current.

*A current mirror is a circuit which behaves as a current controlled current source. It has a single low-impedance input terminal with respect to a reference point and one or more high impedance outputs.

FIGURE 7 — BASIC SLIC CIRCUIT



The hook status control circuit supplies the bias currents to activate the B-Circuit op amps and other sections of the MC3419-1. To activate the bias currents, the control circuit compares the current through the sense resistors, R_R and R_T, and the load resistance R_L with the current through the hook status threshold programming resistor, R_H, by using outputs from both A1 and A2 mirrors. The A1 mirror output sources current to the R_H resistor. (This reduces all internal currents to near zero during the on-hook state in order to eliminate unnecessary power consumption.) If this current is large enough the voltage on the HST pin will trip an internal comparator, then another circuit compares the current from the A1 output with that of an A2 output. These currents must match within ±15%. If so, HSO will be activated and the bias circuits will turn on provided the voltage on $\overline{PDI}$ is greater than −1.2 V. The HSO pin can have either a pull-up resistor or a pull-down resistor and when activated it will switch to V_{CC} (0 volts).

Once the MC3419-1 is powered up, a circuit with a gain of 20 feeds current to the R_H resistor in order to keep the bias circuitry active. (The sense resistors are paralleled with the Darlington transistors which reduces the sense input currents.) Should the sense input currents drop below one-twentieth of the required power-up current, the bias currents will be removed, forcing a power-down condition.

Current mode analog signal processing is critically dependent on voltage to current conversion at the 2-wire and 4-wire inputs. Precise, low-noise voltage sensing through resistors R_T, R_R and R_{RX} requires quiet, low impedance terminations at terminals TSI, RSI and RXI respectively. For 2-wire signals, terminal V_{QB} isolates the loop-sensing resistors and current mirrors from noise at the high-current V_{EE} terminal. External filtering from V_{CC} to V_{QB} ("quiet battery" terminal) ensures loop voltages are sensed without interference from system supply noise. V_{EE} noise rejection at audio frequencies is typically 60 dB or greater.

Receive input terminal RXI is referenced to the V_{AG} terminal which references the 4-wire input to the "analog ground" of the 4-wire signal source, thus isolating the input from power ground voltage transients. This isolation offers 70 dB of noise rejection at audio frequencies.

SYSTEM EQUATIONS

K1 — The current gain from $I_{TSI} + I_{RSI}$ to TXO only during an off-hook power-up condition. K1 = 0.51 ± 1%.

K2 — The current gain from RXI to the collectors of the off-chip Darlington transistors only during an off-hook power-up condition. K2 = 95 ± 1%.

For simplicity, the following equations do not use K1 or K2. Instead the actual numerical value is used, for instance (1 + [2]K1K2) = 1 + 1.02 x 95 = 97.9 is approximately 98.

R_L — Loop resistance. This is a load resistance from Tip to Ring and can be either ac or dc depending on context.

LOOP CURRENT REGULATIONS

FIGURE 8(a)

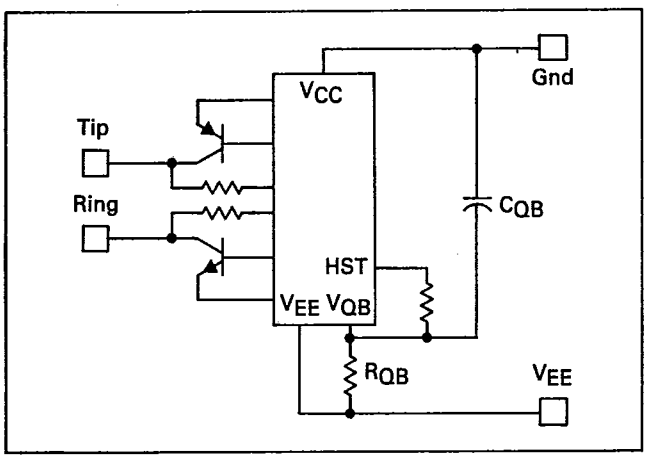


FIGURE 9(a)

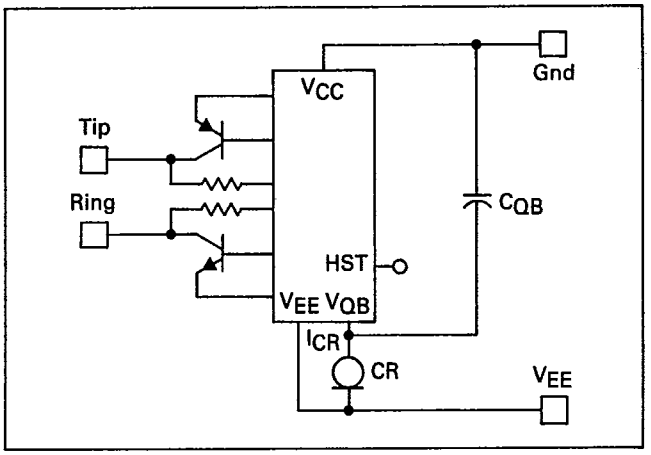


FIGURE 8(b)

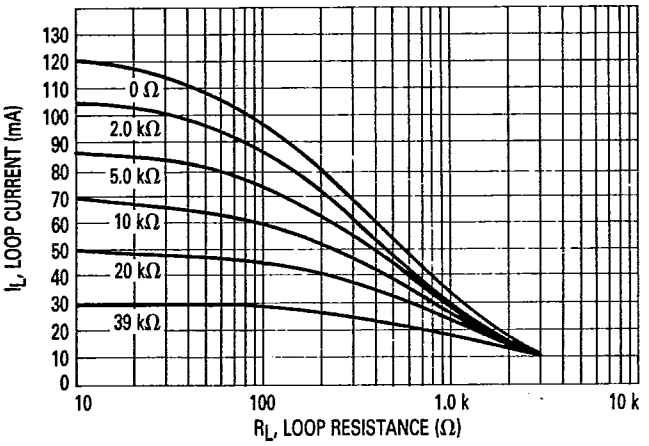
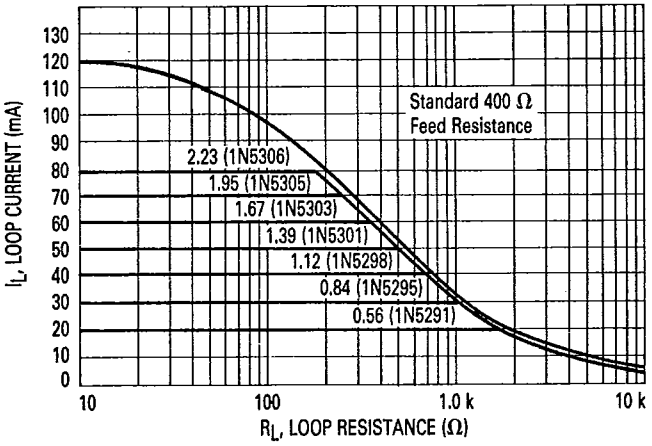


FIGURE 9(b)



SYSTEM EQUATIONS (continued)

Z_L — Loop impedance. This is used only to connote a complex impedance loading on Tip and Ring.

I_L — Loop current. The dc current flow through R_L.

R_F — Dc feed resistance. The synthesized resistance from which battery (V_{CC} and V_{EE}) current is fed to R_L. The battery feed resistance is balanced differential feed. See Figure 7. (This assumes $V_{QB} = V_{EE}$.) The first order equation is:

$$R_F = \frac{R_R + R_T + 1200\ \Omega}{98} \quad (1)$$

Because of the diode voltage drops on TSI and RSI, the actual dc feed resistance is higher. The second order equation is:

$$R_F = \frac{|V_{QB}|(98\ R_L + R_R + R_T + 1200\ \Omega)}{98\ (|V_{QB}| - 4.0\ V)} - R_L \quad (2)$$

ignoring the effects of R_L

$$R_F = \frac{|V_{QB}|(R_R + R_T + 1200\ \Omega)}{98\ (|V_{QB}| - 4.0\ V)} \quad (3)$$

So:

$$R_R = R_T = \frac{49R_F\ (|V_{QB}| - 4.0\ V)}{|V_{QB}|} - 600 \quad (4)$$

The minimum value for R_R and R_T is 5.0 kΩ.

The first order value of R_F can not be greater than the desired value of the termination impedance (usually 600 Ω or 900 Ω). To achieve dc feed resistances that are greater, a resistor can be placed between V_{QB} and V_{EE} along with a filter capacitor C_{QB} which restores the desired termination impedance and filters power supply noise. A diode should also be placed between V_{QB} and V_{EE} to prevent damage in case a catastrophic power supply failure occurs.

I_{VQB} — This is the current that is sourced from the V_{QB} pin and is proportional to the currents into and out of RSI and TSI. When the SLIC is in the off-hook power-up mode, I_{VQB} is also proportional to I_L.

$$I_{VQB} = 2.15\ I_{RSI} + 0.7\ I_{TSI} \quad (5)$$

$$I_{VQB} = 0.029\ I_L \quad (6)$$

R_{FQ} — Dc feed resistance. The synthesized resistance from which battery current is fed to R_L, see Figure 8. (This assumes V_{QB} is tied to V_{EE} through a resistor R_{QB}.) R_{QB} synthesizes additional dc feed resistance to the R_F value previously stated.

When using R_{QB}, the dc feed is effectively balance fed from V_{CC} and V_{QB} instead of V_{EE}. The sense resistors (R_R and R_T) should be selected to make R_F (first order) less than the termination impedance.

$$R_{FQ} = \frac{|V_{EE}|(98R_L + R_R + R_T + 1200 + 2.85R_{QB})}{98(|V_{EE}| - 4.0\ V)} - R_L \quad (7)$$

Ignoring R_L, this simplifies to:

$$R_{FQ} = \frac{|V_{EE}|(R_R + R_T + 1200 + 2.85R_{QB})}{98(|V_{EE}| - 4.0\ V)} \quad (8)$$

Therefore:

$$R_{QB} = \frac{98R_{FQ}(|V_{EE}| - 4.0\ V) - |V_{EE}|(R_R + R_T + 1200\ \Omega)}{2.85|V_{EE}|} \quad (9)$$

C_{QB} — Power supply noise filter capacitor.

$$C_{QB} = \frac{2.85\ R_{QB} + R_R + R_T + 1200\ \Omega}{2\pi f\ R_{QB}\ (R_R + R_T + 1200\ \Omega)} \quad (10)$$

Figure 9B shows R_{QB} replaced with a current regulating device such as Motorola's 1N5283 family.

I_{CRQB} — The current that is sourced to a current regulating device from the V_{QB} pin. When this current reaches the regulated value, the voltage differential between V_{EE} and V_{QB} increases causing the effective battery voltage to decrease which limits I_L to a maximum value as determined below:

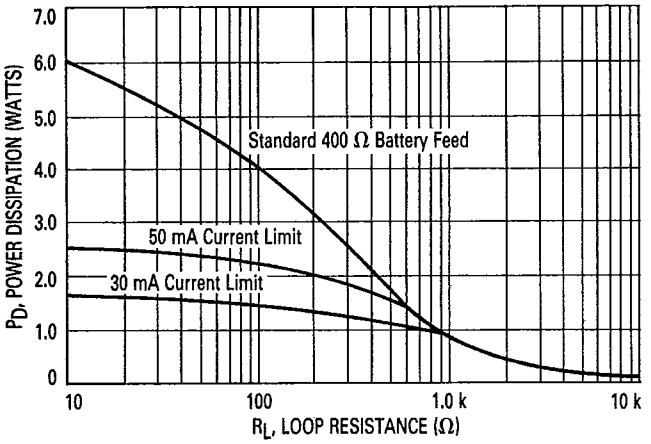
$$I_L = 34.5\ I_{CRQB} \quad (11)$$

The graph, Figure 9B, shows loop current versus loop resistance using several values of I_{CRQB}. The closest current regulating diode part number to that value is also shown. A typical value for C_{QB} in this case is 10 μF, 60 Vdc.

Figure 10 shows how power can be conserved on the shorter loop lengths by utilizing current limiting techniques.

Overvoltage protection on the 2-wire port is achieved with the MDA220 diode bridge and the protection resistors R_{PR} and R_{PT}. Whenever the voltage on the 2-wire port exceeds the power supply rails (V_{CC} and V_{EE}), the MDA220 diodes will forward bias and "clamp" to the rail voltage. The current is limited by the protection resistors. These resistors should be as large in value as possible. However, if they are too large, they will interfere with the performance of the SLIC under worst case conditions.

FIGURE 10 — TOTAL SLIC POWER DISSIPATION versus LOOP RESISTANCE



$$R_{PT} < R_T/196 - 15 \quad (12)$$

Using the voltage of V_{QB} when I_L is at its minimum off-hook value (Typ. 20 mA):

$$R_{PR} < R_R/196 + 25|V_{EE} - V_{QB}| - 15 \quad (13)$$

The tolerance of these resistors is not critical due to placement inside a closed loop. Positive temperature co-efficient resistors (PTC) may be considered here. Consult resistor manufacturers for component selections that will meet the surge current and peak voltage requirements.

Because the MC3419-1 is a broadband device it requires compensation components to keep its circuits stable.

C_R & C_T — Compensates the longitudinal gain of the A and the B circuit mirrors. Their values range from 2000 pF to 5000 pF.

R_C & C_C — Compensates the longitudinal "C" circuitry. Their values can be ratioed according to:

$$R_C \times C_C = R_T \times C_T. \quad (14)$$

Two off-chip power Darlington transistors are used with the MC3419-1. These transistors reduce any temperature gradiant problems with the precision matched devices on-chip and they alleviate thermal stress conditions that could occur for every on-hook and off-hook transition. The power dissipation in these devices is:

$$P_{QT} = I_L{}^2(R_T/98 - R_{PT} - 4) + (2.0\ V)I_L \quad (15)$$

$$P_{QR} = I_L\,[|V_{EE}| - 2 - I_L(R_T/98 + R_L + R_{PR} + 16)] \quad (16)$$

where $I_L = |V_{EE}|/R_{FQ}$ or I_L(max) in current limited designs.

SYSTEM EQUATIONS (continued)

R_H — The resistor that determines the hook status threshold values of R_L. R_H is selected from a graph of the following two equations:

Off-hook threshold

$$R_H = 6(R_L + R_R + R_T) \quad (17)$$

On-hook threshold

$$R_H = 27.25\,[R_L + 0.01(R_R + R_T)] \quad (18)$$

FIGURE 11 — HOOK STATUS DETECTION

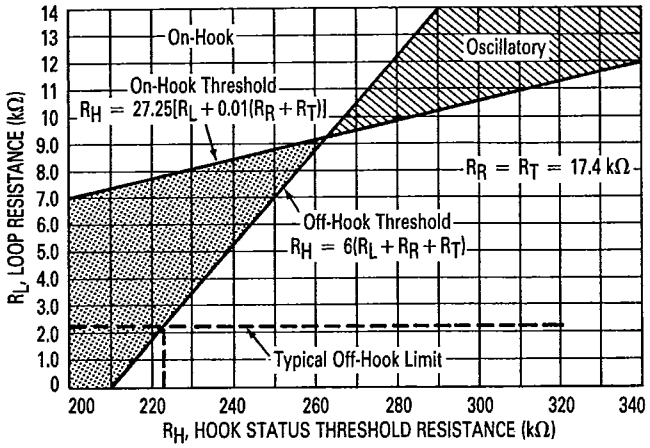


Figure 11 shows such a graph using 17.4 kΩ as the values for R_R and R_T. Note the oscillatory condition to the right of the crossing point. Selection of R_H in this region is usually not a problem since the majority of telephone lines do not fall into this resistance range. R_H always ties to V_{QB} and HST and will give reliable hook status information regardless of power supply voltages and $\overline{PDI}$.

R_O — Termination impedance of the 2-wire port. This impedance is greater than the dc feed resistance R_F because of a current splitting network in the feedback loop, R_{TX1} and R_{TX2}.

K3 — A constant, formed by R_{TX1} and R_{TX2}, between 0 and 1, which determines the ratio of the first order value of R_F to R_O.

$$R_O = \frac{R_R + R_T + 1200\ \Omega}{1 + 97K3} \quad (19)$$

So:

$$K3 = \frac{R_R + R_T + 1200\ \Omega - R_O}{97R_O} \quad (20)$$

and

$$K3 = \frac{R_{TX2} + Z_{in}}{R_{TX1} + R_{TX2} + Z_{in}} \quad (21)$$

Z_{in} — The input impedance of the current to voltage converter op amp. This impedance is usually negligible, it can be used to sway the selection of a 1% component value.

$$Z_{in} = \frac{(R_R + R_T + 1200\ \Omega)\,G_{TX}}{1020\,(1 - K3)} = \frac{R_{VTX}}{1000} \quad (22)$$

R_{TX1} — Feeds most of the TXO dc current to the RXI pin. To keep TXO from saturation the maximum value of R_{TX1} is as follows:

$$R_{TX1} < \frac{(R_R + R_T + 1200\ \Omega)\,(|V_{QB}|min - |V_{AG}|max - 6.5\ V)}{|V_{QB}|min - 5.4\ V} \quad (23)$$

Where:

$$|V_{QB}|min = \frac{(R_R + R_T + 1200\ \Omega)\,(|V_{EE}|min - 4)}{(R_R + R_T + 1200\ \Omega + 2.8\ R_{QB})} \quad (24)$$

or if a current regulator diode is used:

$$R_{TX1} < \frac{0.01\ I_L(max)\,(R_R + R_T + 600\ \Omega) - |V_{AG}|max - 3.9\ V}{0.01\ I_L(max)} \quad (25)$$

It is beneficial to make R_{TX1} as large as possible. Typical values range from 15 k to 24 kΩ.

$$R_{TX2} = \frac{K3\ R_{TX1}}{1 - K3} - Z_{in} \quad (26)$$

$$C_{TX} = \frac{R_R + R_T + 1200\ \Omega}{7R_{TX2}} \quad \text{The result is in } \mu F. \quad (27)$$

G_{TX} — The voltage gain from the 2-wire port to V_{TX} which is adjustable by R_{VTX}.

$$G_{TX} = \frac{1.02\,(1 - K3)\,R_{VTX}}{R_R + R_T + 1200\ \Omega} \quad (28)$$

$$R_{VTX} = \frac{G_{TX}(R_R + R_T + 1200\ \Omega)}{1.02\,(1 - K3)} \quad (29)$$

G_{RX} — The voltage gain from the V_{RX} input to the 2-wire port which is adjustable by R_{RX}.

$$G_{RX} = \frac{-95\ R_L\,(R_R + R_T + 1200\ \Omega)}{R_{RX}\,[(R_R + R_T + 1200\ \Omega) + R_L(1 + 97K3)]} \quad (30)$$

$$G_{RX} = \frac{-95\ R_L\ R_O}{R_{RX}(R_L + R_O)} \quad (31)$$

$$R_{RX} = \frac{95\ R_L\ R_O}{G_{RX}(R_L + R_O)} \quad (32)$$

$$C_{RX} > \frac{R_{RX} + R_B}{2\pi\ f\ R_{RX}R_B} \quad (33)$$

Where f is the minimum passband frequency, usually 200 Hz.

Transhybrid Rejection — The voltage gain from V_{RX} to V_{TX}. It is expressed in dB, the number should be negative and the larger the value the better. Transhybrid rejection is achieved by summing a current from the V_{RX} input (R_B) with the TXO current that flows to the current to voltage converter. R_B balances a resistive load, R_L.

$$R_B = \frac{R_{RX}(1 + 97K3)\,(R_O + R_L)}{97R_L\,(1 - K3)} \quad (34)$$

FIGURE 12 — BALANCE NETWORK FOR CAPACITIVE LINES

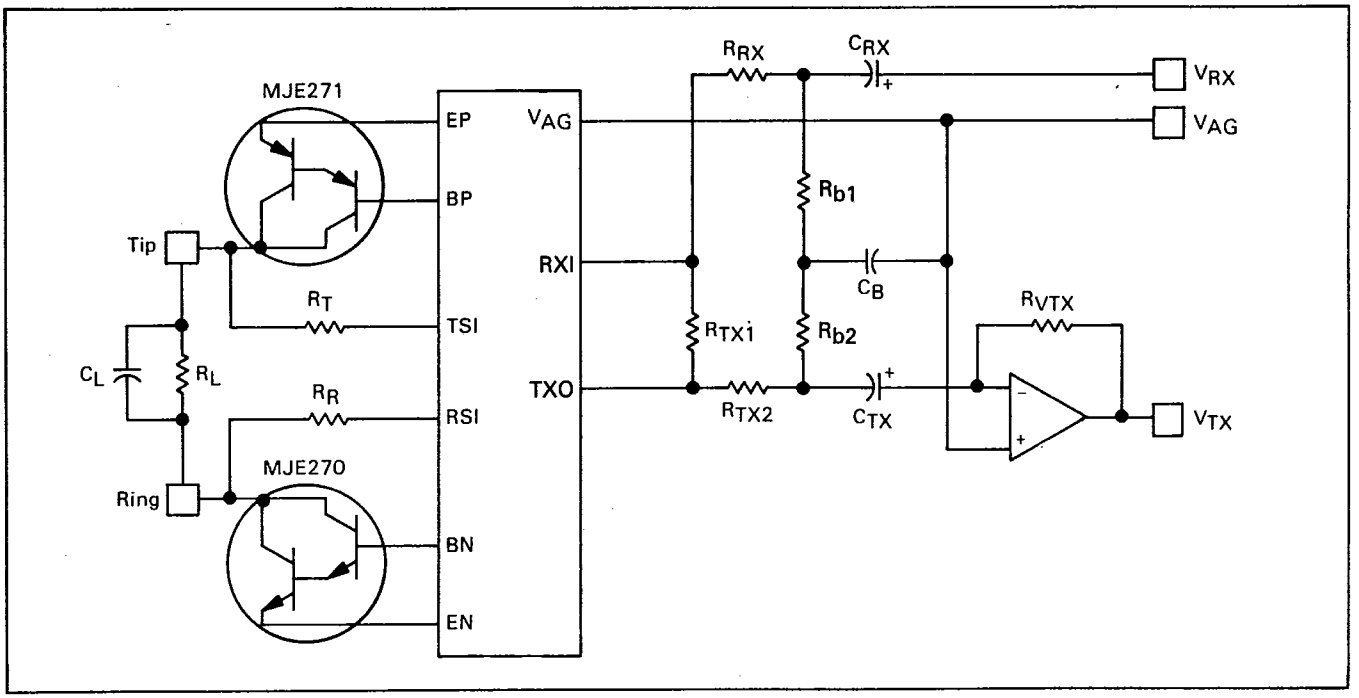
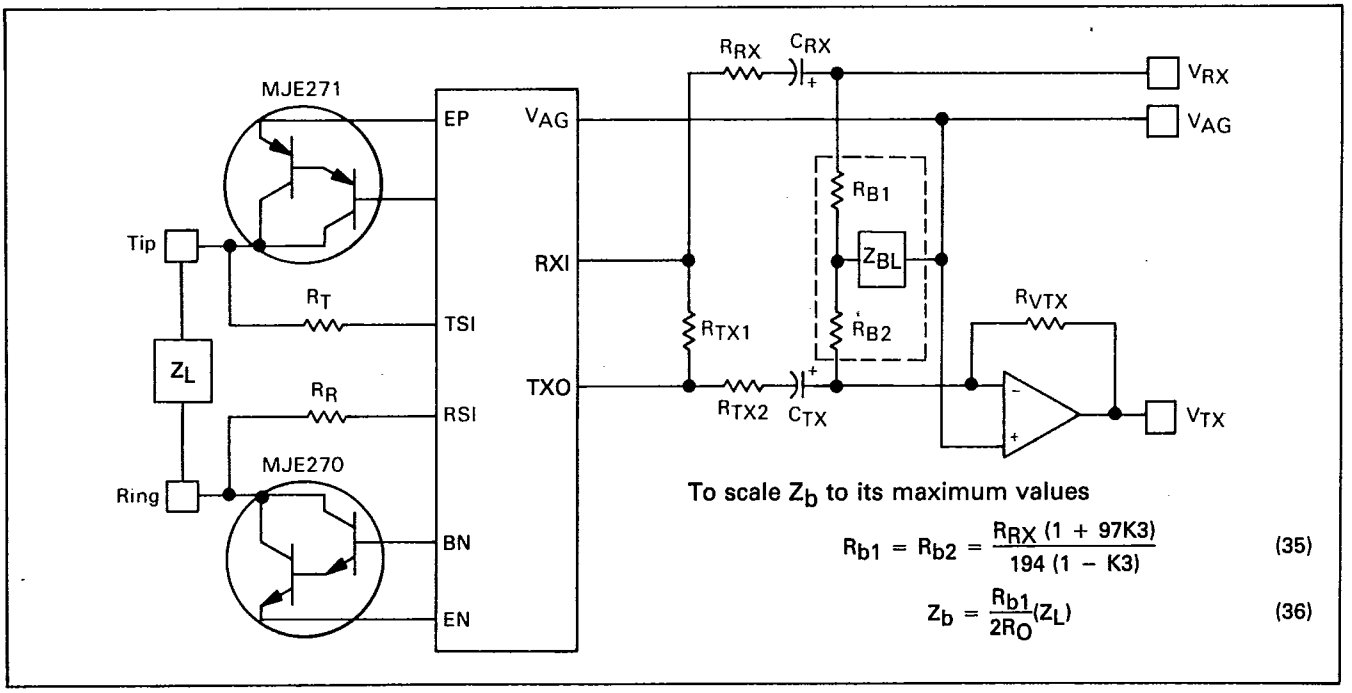


FIGURE 13 — BALANCE NETWORK FOR COMPLEX LOAD IMPEDANCES



To scale Z_b to its maximum values

$$R_{b1} = R_{b2} = \frac{R_{RX}\,(1 + 97K3)}{194\,(1 - K3)} \quad (35)$$

$$Z_b = \frac{R_{b1}}{2R_O}(Z_L) \quad (36)$$

When the 2-wire port has a parallel R and C load, then (see Figure 12):

$$R_{b1} = \frac{R_{RX}(R_R + R_T + 1200\ \Omega)}{97R_L\,(1 - K3)} \quad (37)$$

$$R_{b2} = \frac{R_{RX}(R_R + R_T + 1200\ \Omega)}{97R_O(1 - K3)} \quad (38)$$

$$C_b = \frac{R_L C_L}{R_{b2}} \quad (39)$$

When it is desirable to balance complex load impedances using component values that are equal to the load values (see Figure 13) then:

$$R_{b1} = \frac{R_{RX}(1 + 97K3)}{194(1 - K3)} + \sqrt{\left[\frac{R_{RX}(1 + 97K3)}{194(1 - K3)}\right]^2 - \frac{R_O R_{RX}(1 + 97K3)}{97(1 - K3)}} \quad (40)$$

$$R_{b2} = \frac{R_{RX}(1 + 97K3)}{97(1 - K3)} - R_{b1} \quad (41)$$

$$Z_b = Z_L \quad (42)$$

R_{b1} and R_{b2} values are interchangeable.

SYSTEM EQUATIONS (continued)

The Tip and Ring Sense Output currents are proportional to the currents out of and into TSI and RSI, respectively.

$$I_{TSO} = \frac{I_{TSI}}{6} \quad (43)$$

$$I_{RSO} = \frac{I_{RSI}}{6} \quad (44)$$

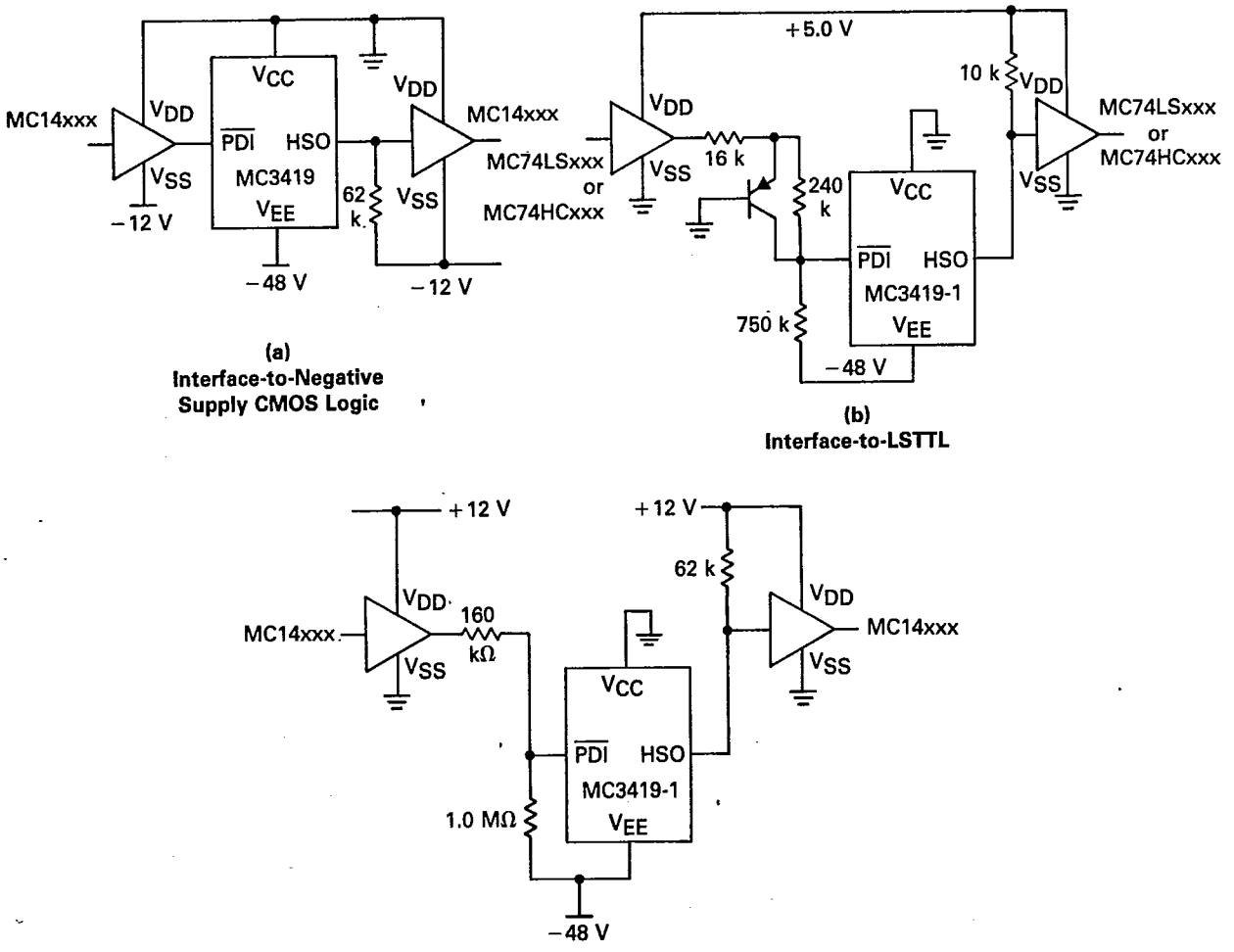
$$I_{TSO} = \frac{|V_{Tip} - V_{CC}| - 2.0\ V}{6\ (R_T + 600\ \Omega)} \text{ for } V_{Tip} < V_{CC} \quad (45)$$

$$I_{RSO} = \frac{|V_{Ring} - V_{QB}| - 2.0\ V}{6(R_R + 600\ \Omega)} \text{ for } V_{Ring} > V_{QB} \quad (46)$$

Digital interfacing to the MC3419-1 $\overline{PDI}$ pin and the HSO pin is shown in Figures 14a, 14b and 14c. If the $\overline{PDI}$ pin is not used it should be terminated to V_{CC} and if HSO is not used, it can be left open.

Figure 15 is an application circuit showing solid state ringing insertion using an MOC3030 zero-crossing detector optocoupled triac to replace the conventional electromechanical relay. This device inserts the ringing signal on a zero voltage crossing which eliminates noise in adjacent cable pairs and removes the signal on a zero current crossing which eliminates inductive voltage spikes that commonly destroy relay contacts. The ringing generator provides a continuous 40 V to 120 V RMS signal from 15 to 66 Hz superimposed upon −48 Vdc. Ringing cadencing is inserted with the Ring Enable Input. The 2N6558 and MPSA42 replace the MJE270 for systems that use ringing generator voltages greater than 70 V_{RMS}. The MDA220 diode bridge is replaced with a series 1N4007 on the Tip lead and a shunting 1N4004 to V_{EE} and to allow ringing voltage

FIGURE 14 — INTERFACE-TO-DIGITAL LOGIC



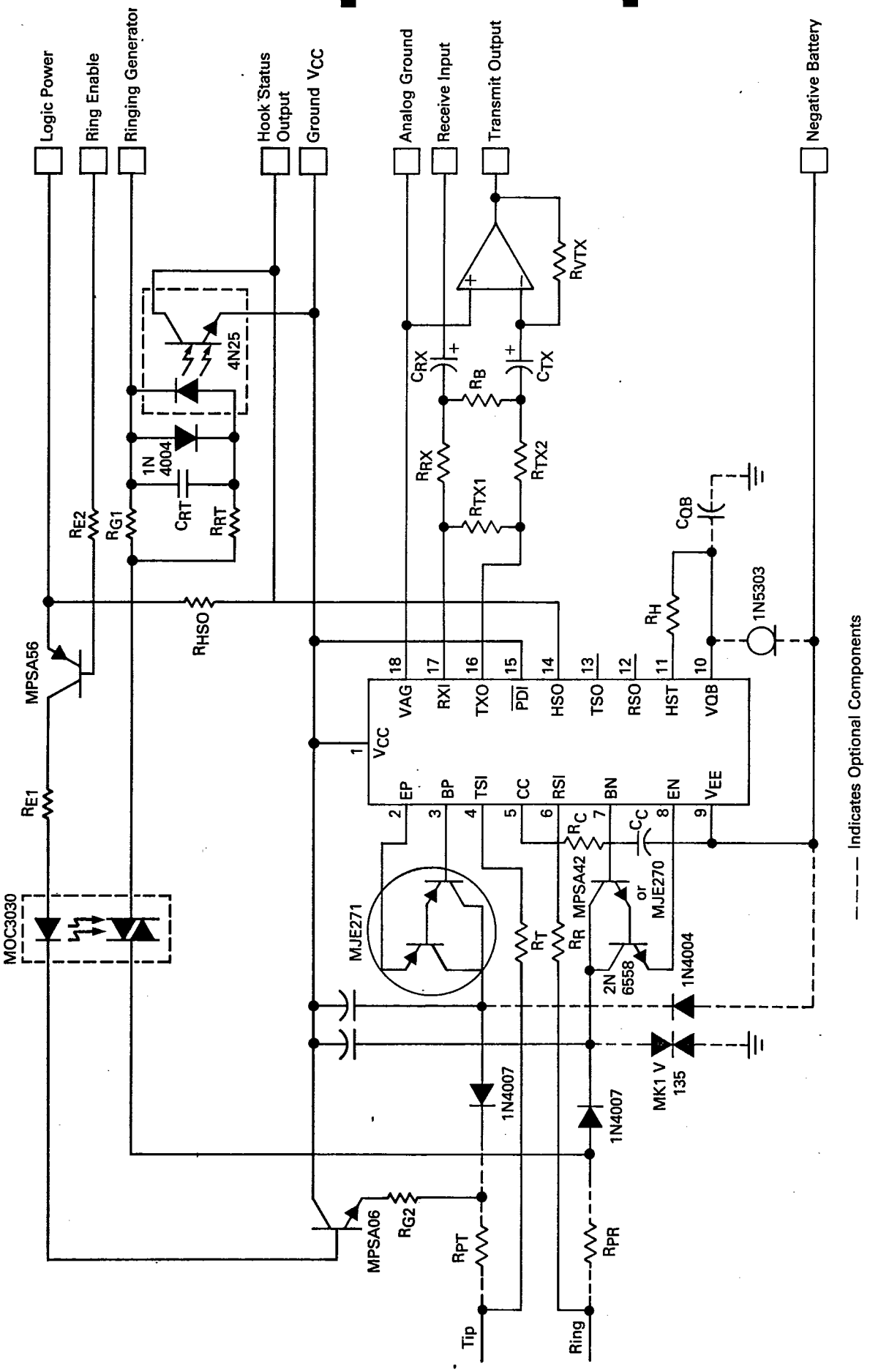


FIGURE 15 — PBX LINE CIRCUIT

SYSTEM EQUATIONS (continued)

on the Ring lead to exceed the power supply voltages, a 1N4007 and an MK1V-135 (Sidac) are used for protection. The forward voltage drop across the 1N4007, during normal operation, will not affect the parametric characteristics of the MC3419-1 since it is "inside" a feedback circuit. If the MJE270 is used, the MK1V-135 should be replaced with a lower voltage Sidac or MO•sorb transient suppressor.

An optocoupled transistor circuit is used for ring trip detection on long lines. It samples only the ac and dc ringing signal current and uses a simple one pole filter to eliminate the low level ac signal. Under worst case conditions this circuit will ring trip in 1½ to 4 cycles. In systems serving only short loops (<700 Ω), if R_{G1} and R_{G2} are 620 Ω or greater, the optotransistor circuit is not needed, the Hook Status Output will perform ring trip on a Zero Crossing. The Ring Enable input and the Hook Status Output interface with standard CMOS and TTL logic.

The op amp in this circuit is an integral part of the following codecs, filters or combos:

MC3417/8 — MC145414
MC14404/6/7 — MC14413/4
MC14401/2/3/5

LONG LINES OFF-PREMISE LINES

Specifications

R_F	— 200 Ω	R_O	— 600 Ω
I_L(max)	— 60 mA	R_X Gain	— 0 dB 200–3400 Hz
R_L(max)	— 1900 Ω	T_X Gain	— 0 dB 200–3400 Hz

Off-Hook	— <2500 Ω	V_{Logic}	— +5.0 V
On-Hook	— >10 kΩ	V_{EE}	— −42 to −56 Volts
Protection	— 1000 V	$V_{Ringing}$	— (40 V to 120 V_{RMS}) + V_{EE}
Ringer Equivalent	— 5		

Parts List

MPSA56	R_R	—	9.09 k	1%	Matched
2N3905	R_T	—	9.09 k	1%	if desired
2N6558	R_{PT}	—	47 Ω	5%	
MPSA42	R_{PR}	—	75 Ω	5%	
MJE271	R_{G1}	—	620 Ω	5%	
1N4007	R_{G2}	—	100 Ω	5%	
MK1V135	R_{E1}	—	91 Ω	5%	
1N4007	R_{E2}	—	3.0 k	5%	
1N4007	R_{RT}	—	20 k	5%	
1N5303	R_C	—	24 k	5%	
1N4004	R_H	—	127 k	1–3%	
MC3419-1	R_{HSO}	—	10 k	5%	

MOC3030	R_{TX1}	—	12.1 k	1%	
4N25	R_{TS2}	—	5.76 k	1%	
	R_{RX}	—	28.7 k	1%	
	R_B	—	28.0 k	1%	
	R_{VTX}	—	28.6 k	1%	
	C_T		0.004 μF		
	C_R	—	0.004 μF		
	C_C	—	0.001 μF		
	C_{RX}	—	1.0 μF/20 V		
	C_{TX}	—	2.0 μF/40 V		
	C_{RT}	—	20 μF/5.0 V		
	C_{QB}	—	10 μF/60 V		

SHORT LINES ON-PREMISE LINES

Specifications

R_F	—	500 Ω
R_L(max)	—	700 Ω
Ring Trip	—	<50 ms
Ringer Equivalent	—	2.5
R_O	—	600 Ω

R_X Gain	—	−5.0 dB
T_X Gain	—	0 dB
V_{Logic}	—	+5.0 Volts
V_{EE}	—	−20 to −56 Volts
$V_{Ringing}$	—	(40 V to 70 V_{RMS}) + V_{EE}

Parts List

MJE271	R_R	—	19.6 k	1%	
MJE270	R_T	—	19.6 k	1%	
MPSA56	R_{G1}	—	620 Ω	5%	
2N3905	R_{G2}	—	620 Ω	5%	
1N4007	R_{E1}	—	91 Ω	5%	
1N4007	R_{E2}	—	3.0 k	5%	

MOC3030					
	C_T	—	0.004 μF		
	C_R	—	0.004 μF		
	C_C	—	0.004 μF		
	C_{RX}	—	0.1 μF		
	C_{TX}	—	0.5 μF		

	R_{HSO}	—	10 k	5%	
	R_{TX1}	—	19.6 k	1%	
	R_{TX2}	—	42.2 k	1%	
	R_{RX}	—	69.8 k	1%	
	R_B	—	301 k	1%	
	R_{VTX}	—	127 k	1%	
	R_C	—	56 k	5%	