Bt8075

CRC-4 Encoder/Decoder

Distinguishing Features

- CRC-4 Transmit and Receive per CCITT Recommendation G.704
- Insertion and Extraction of Spare Bits (SP1 and SP2)
- Independent Error Detection and Reporting of CRC-4 and Multiframe Alignment Errors
- CRC-4 Enable/Disable Capability
- Enhanced HDB3 Encode/Decode Section, Includes Reporting of Bipolar Violations
- Read/Write Access to International Bits in CRC-4 Disable Mode
- Bit, Channel, and Frame Timing Available to System
- Low Power CMOS Technology
- Operates From a Single +5 V Power Supply
- Package Options
  – 24-Pin Plastic DIP
  – 28-Pin PLCC

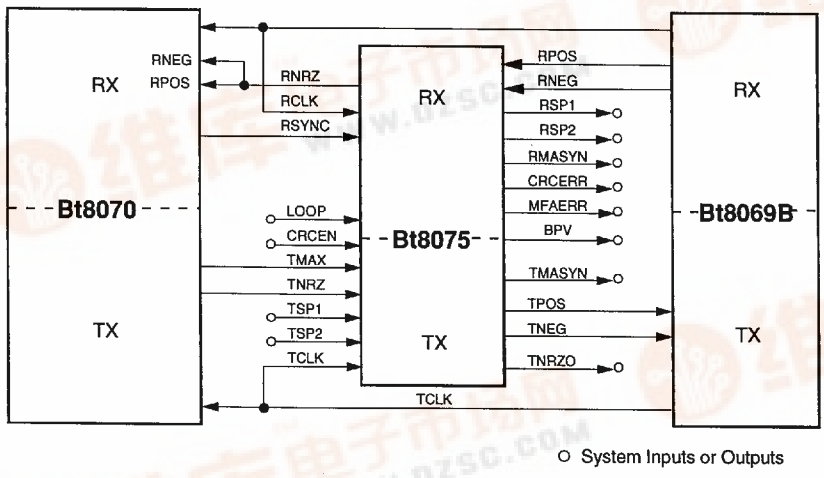

Figure 1. Bt8075 Functional Interface

Product Description

The Bt8075 CRC-4 Encoder/Decoder is a support device to the Bt8070/Bt8070A T-1/CEPT PCM Transceiver and the Bt8069B Line Interface Unit. Used with the Bt8070 and the Bt8069B, the Bt8075 implements transmit and receive functions in accordance with CCITT Recommendation G.704 for PCM–30 using CRC-4. Operation of the Bt8075 is entirely transparent other than error detection/reporting and handling of the spare bits. The Bt8075 can be set in either enable or disable mode, for systems that handle data encoded with or without CRC-4.

Transmit functions compute the CRC-4 polynomial and insert the proper alignment timing and spare bits (SP1, SP2) into the transmit data stream. HDB3 encoding is also handled by the Bt8075.

Receive functions are independent error detection of CRC-4 and multiframe alignment, extraction of the spare bits, and HDB3 decoding (including reporting of bipolar violations).

The bit, channel, and frame timing signals are available to the system for both the transmit and receive sections. The Bt8075 can support ISDN applications using the Bt8070 256N mode and PCM–30 signaling modes using the 256S mode.

Brooktree Corporation • 9868 Scranton Rd. • San Diego, CA 92121-3707
(619) 452-7580 • (800) 2BT-APPS • TLX: 383 596 • FAX: (619) 452-1249
L807501 Rev. A

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Interface Signals

The Bt8075 interfaces to the Bt8070 T1/CEPT PCM Transceiver, the Bt8069B Line Interface Unit, and the system. Figure 1 illustrates the functional interface. Figure 2 shows the signals grouped by interface. The Bt8075 interface signals are listed by pin number Table 1. This table alsi details pin assignments. Interface signal definitions are given in Table 2. Graphic representation of the pin assignments is given in Figure 3.

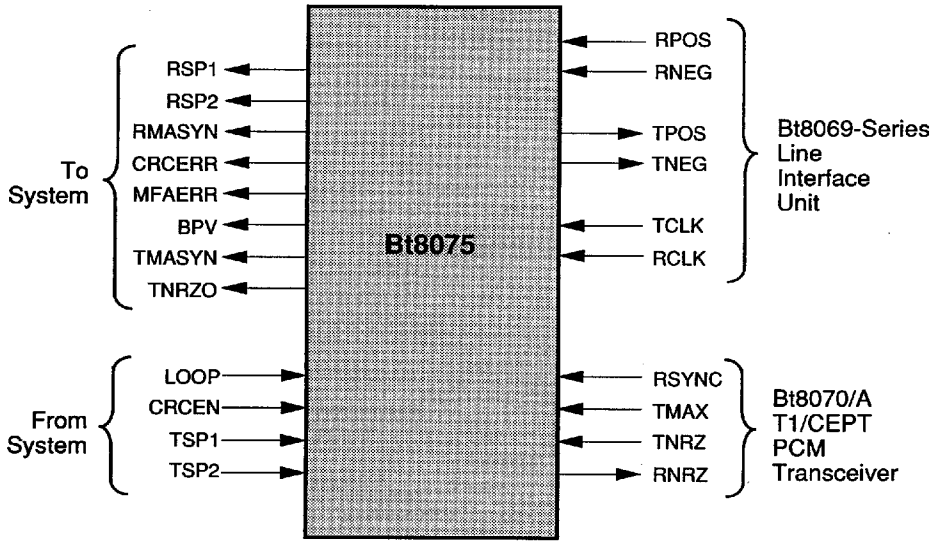


Figure 2. Bt8075 Interface Signals

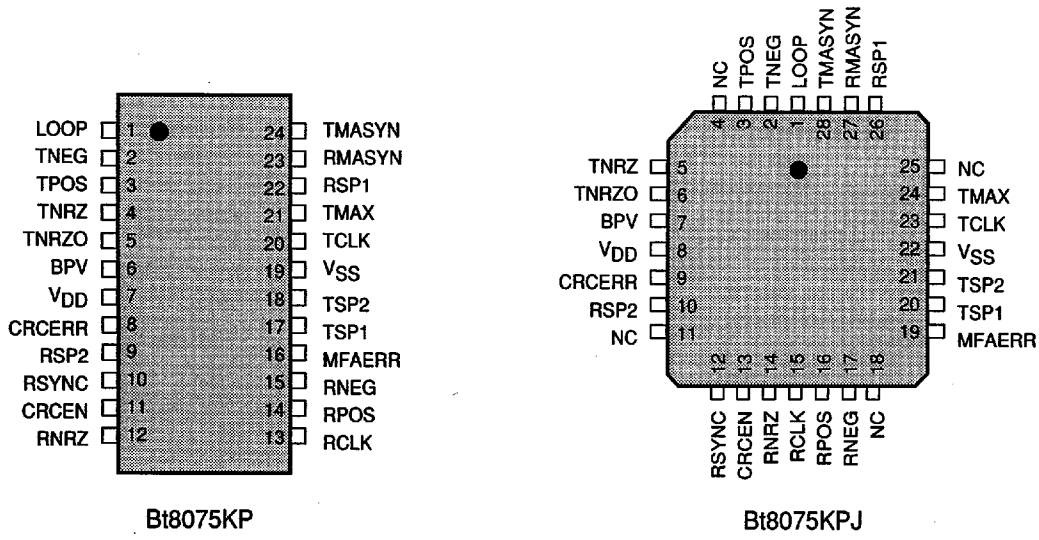


Figure 3. Bt8075 Pin Assignments

Interface Signals *(continued)*

Symbol	24-Pin DIP	28-Pin PLCC	Signal Name	I/O	Source/ Destination
LOOP	1	1	Loopback Mode	I	System
TNEG	2	2	Transmit Unipolar Negative	O	Bt8069B
TPOS	3	3	Transmit Unipolar Positive	O	Bt8069B
N.C.	–	4	No Connect		
TNRZ	4	5	Transmit NRZ Data (IN)	I	Bt8070
TNRZO	5	6	Transmit NRZ Data (OUT)	O	System
BPV	6	7	Bipolar Violation	O	System
VDD	7	8	+5 VDC Power	–	Power Supply
CRCERR	8	9	CRC-4 Error	O	System
RSP2	9	10	Receive Spare Bit 2	O	System
N.C.	–	11	No Connect		
RSYNC	10	12	Receive Sync	I	Bt8070
CRCEN	11	13	CRC-4 Enable	I	System
RNRZ	12	14	Receive NRZ Data	O	Bt8070
RCLK	13	15	Recovered (Receive) Clock	I	Bt8069B
RPOS	14	16	Receive Unipolar Positive	I	Bt8069B
RNEG	15	17	Receive Unipolar Negative	I	Bt8069B
N.C.	–	18	No Connect		
MFAERR	16	19	Multiframe Alignment Error	O	System
TSP1	17	20	Transmit Spare Bit 1	I	System
TSP2	18	21	Transmit Spare Bit 2	I	System
VSS	19	22	Ground	–	Ground
TCLK	20	23	Transmit Clock	I	Bt8069B
TMAX	21	24	Transmit Maximum	I	Bt8070
N.C.	–	25	No Connect		
RSP1	22	26	Receive Spare Bit 2	O	System
RMASYN	23	27	Receive MF Alignment Sync	O	System
TMASYN	24	28	Transmit MF Alignment Sync	O	System

Table 1. Bt8075 Pin Assignments

Interface Signals *(continued)*

Mnemonic	DIP Pin No.	PLCC Pin No.	Name/Description
Inputs From Bt8069B (Line Interface Unit)			
RCLK	13	15	**Recovered (Receive) Clock** from Bt8069B. RCLK is the recovered clock output which is locked to the frequency and phase of the incoming data. RPOS and RNEG are clocked out of the Bt8069B at the falling edge of RCLK in the elastic store bypass mode (CB high). This signal is also input to the Bt8070 as the receiver clock input.
TCLK	20	23	**Transmit Clock** from Bt8069B. Transmitter Clock is either the smoothed clock provided through EXCLK (External Clock Reference, Bt8069B,or the smoothed clock extracted from the input data. The receive data are also clocked out on the falling edge of TCLK, except in elastic store bypass mode (CB high). This signal is also input to the Bt8070 as the transmitter clock input.
RPOS RNEG	14 15	16 17	**Receive Unipolar Positive, Negative** from Bt8069B. RPOS and RNEG are the outputs of the received data recovered from RXINP and RXINN AMI line pulses. RPOS and RNEG have TTL levels and are in NRZ format. These are directly connected to the Bt8075. RPOS and RNEG are clocked out of the Bt8069B at the falling edge of RCLK (elastic store bypass mode) or TCLK in (elastic store enable mode), and clocked into the Bt8075 at the rising edge of RCLK.
Inputs From Bt8070 (PCM –30 Transceiver)			
RSYNC	10	12	**Receive Sync** from Bt8070. While the receiver is synchronized, RSYNC is high during the first bit of each multiframe.
TMAX	21	24	**Transmit Maximum** from Bt8070. TMAX is high for one bit time per multiframe coincident with the sampling of the next to last bit of a multiframe.
TNRZ	4	5	**Transmit NRZ Data** from Bt8070. NRZ (Non-Return-to-Zero) output for transmitted data. This output is unaffected by LOOP or by HDB3 zero-suppression coding. There is an 8-bit throughput delay between the TSER input and the TNRZ output.
Inputs From The System			
CRCEN	11	13	**CRC-4 Enable.** Control input which enables the Bt8075 when CRCEN is high. When CRCEN is low, the Bt8075 is disabled, providing full transparent operation. In this mode the user has control of the international bits. The Bt8075 receiver functions always operate; only the transmit functions are bypassed when CRCEN is low.
LOOP	1	1	**Loopback Mode.** Control input placing the Bt8075 in loopback mode. In this mode, TPOS and TNEG are routed internally to RPOS, RNEG (respectively). This function replaces the Bt8070 loopback function. CRCEN does not affect this function.
TSP1 TSP2	17 18	20 21	**Transmit spare bits 1,2.** Input to Bt8075 which allows insertion of the spare international bits. When the Bt8075 is enabled, the user may update the TSP1, TSP2 inputs at the occurrence of TMASYN. These bits are reserved for future international applications, and for now, they should be fixed at 1 on digital paths crossing international borders. These inputs may optionally be used to insert E-bits in frames 13 and 15.
Outputs To Bt8069B (Line Interface Unit)			
TPOS TNEG	3 2	3 2	**Transmit Unipolar Positive, Unipolar Negative.** TPOS and TNEG are the "unipolar paired" outputs for transmitted data. These outputs from the Bt8075 replace those which ordinarily come from the Bt8070. They are clocked out on the rising edge of TCLK. The state TPOS, TNEG = 1 is not valid; all other combinations are valid. The Bt8075 never generates the invalid combination.

Table 2. Bt8075 Interface Signal Definitions

Interface Signals *(continued)*

Mnemonic	DIP Pin No.	PLCC Pin No.	Name/Description
Outputs To Bt8070 (PCM–30 Transceiver)			
RNRZ	12	14	**Receive NRZ Data.** This lead is connected to both the RNEG and RPOS pins of the Bt8070. When connected in this manner, the HDB3 encoder and decoder along with the Bipolar Violation Detector in the Bt8070 are disabled. These functions are supplied by the Bt8075.
Outputs To The System			
CRCERR	8	9	**CRC-4 Error.** At the end of every Sub-MultiFrame (SMF) (eight frames each), the current frame CRC result is clocked into a temporary holding register. During the following SMF, the incoming CRC bits on RSER are compared with the contents of the holding register. If a mismatch occurs, the CRC-4 error signal (CRCERR) is generated. This condition can result from a loss of frame alignment or by an incidental data error. This signal is valid after the falling edge of the second RCLK in the SMF and remains valid for the entire SMF, resetting at the end of the SMF. This output may optionally be used to encode outgoing E-bits.
MFAERR	16	19	**Multiframe Alignment Error.** The Multiframe Alignment Error signal is generated when there is a miss in the CRC-4 alignment bits (sequence of...001011...). It indicates each instance of multiframe alignment and is valid during each MF. It is reset when the CRC-4 alignment is regained. This signal can be used by the system to improve the frame alarm handling, and may be gated with CRCERR to produce E-bits.
TNRZO	5	6	**Transmit NRZ Data.** Serial transmit NRZ data. Derived by the Bt8075, includes inserted CRC and spare bits.
RMASYN	23	27	**CRC-4 Receive Multiframe Alignment Sync.** Derived signal generated by the Bt8075 indicating the beginning of the received CRC-4 multiframe. It is a positive pulse of one RCLK in duration.
TMASYN	24	28	**CRC-4 Transmit Multiframe Alignment Sync.** This signal indicates the beginning of the transmitted CRC-4 multiframe. It is a positive pulse of one TCLK period in duration.
BPV	6	7	**Bipolar Violation.** This signal indicates that a Bipolar Violation has occurred. It replaces the equivalent signal RVLL from the Bt8070, which indicates a Bipolar Violation. HDB3-encoded bipolar violations are not indicated.
RSP1 RSP2	22 9	26 10	**Receiver Spare International Bits.** The receive logic extracts these spare international bits and makes them available to the system at the beginning of each multiframe (RMASYN).
Power And Ground			
V_{DD}	7	8	**Power.** +5 V DC power.
V_{SS}	19	22	**Ground.** Power and signal ground.
NC		4, 11 18, 25	**No Connect.** These pins are on the PLCC, and must remain unconnected.

Table 2.** (continued). **Bt8075 Interface Signal Definitions

Functional Description

The Bt8075 is used with the Bt8070 Transceiver and the Bt8069 Line Interface Unit to provide CRC-4 capability for PCM–30 systems (see Figure 4). There are two basic sections to the Bt8075: Transmit and Receive.

Signals connected to either the Bt8069 or Bt8070 are described in the pin definitions (see Table 2). For more information, please refer to the functional and interface descriptions of the Bt8069 and Bt8070 data sheets.

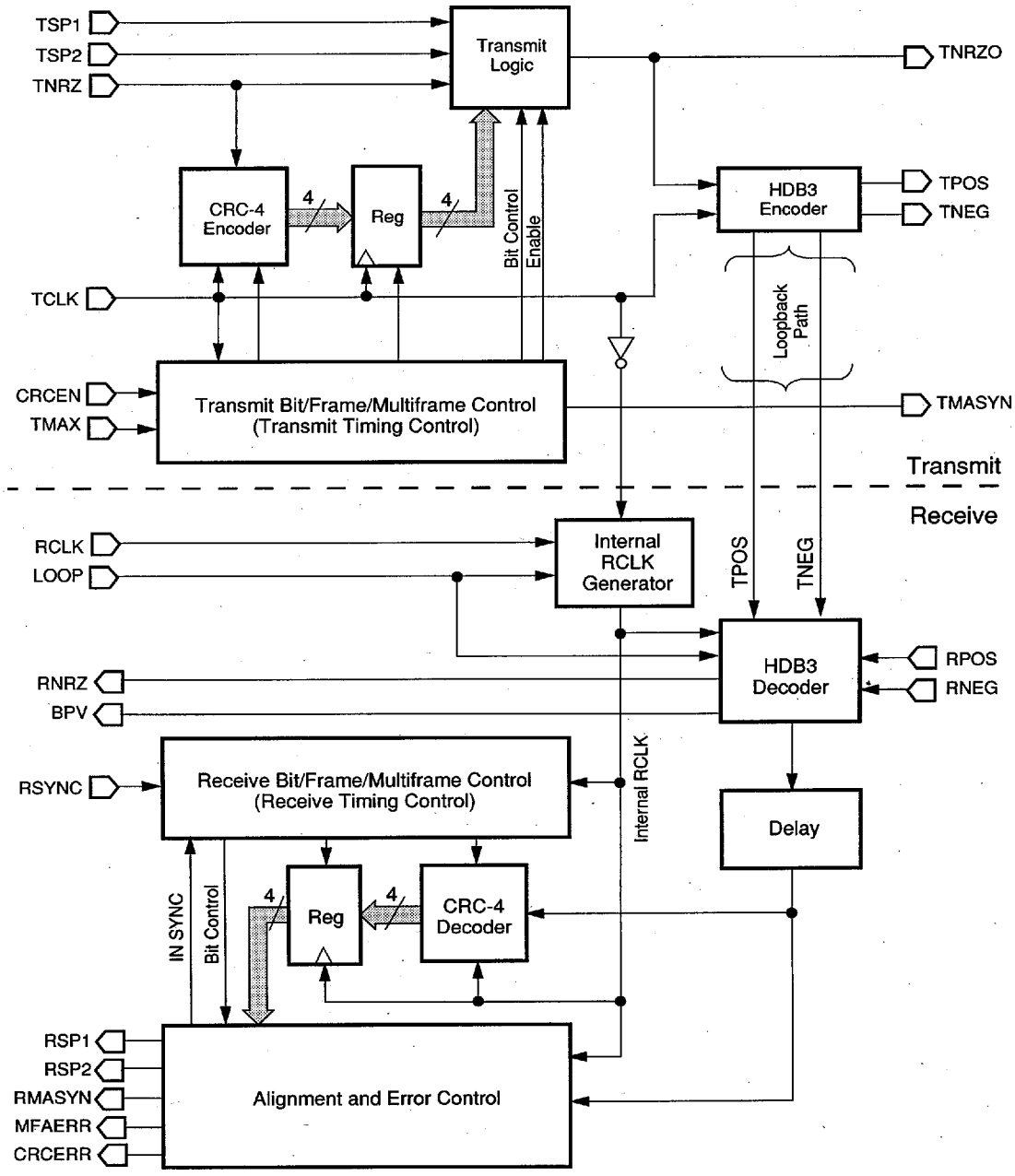


Figure 4. Bt8075 Functional Block Diagram

Functional Description *(continued)*

Transmit Section

The Transmit section computes the CRC-4 polynomial, inserts alignment timing signals and spare bits into the transmit data stream, and encodes the bipolar transmit data using HDB3.

The six Bt8075 Transmit section inputs are from the system (TSP1, TSP2, CRCEN), from the Bt8069 (TCLK), and from the Bt8070 (TNRZ, TMAX). The four Bt8075 Transmit section outputs go to the system (TNRZO and TMASYN) and to the Bt8069 (TPOS and TNEG).

The Bt8075 Transmit section is divided into four blocks:

1. Transmit Logic
2. CRC-4 Encoder
3. HDB3 Encoder
4. Transmit Bit/Frame/Multiframe Control (Transmit Timing Control)

Transmit Logic

Transmit Logic provides the Transmit NRZ Data (TNRZO) output to the system. The signal has the CRC-4 bits and the spare bits inserted at the proper time, as appropriate. There is a 1-bit throughput delay between TNRZ input and TNRZO output.

Data inputs to Transmit Logic are the Non Return-to-Zero (NRZ) output for transmitted data from the Bt8070 (TNRZ) and the Transmit spare bits from the system (TSP1, TSP2). When the CRC-4 encoder is enabled (CRCEN = High), it provides CRC-4 data to Transmit Logic for insertion into the transmitted bit stream. When CRCEN = LOW, CRC-4 is not being implemented and access to the international bit for each frame is provided through the Bt8070/70A. In this case, the Bt8075 passes the international bit transparently.

Control and timing inputs to the Transmit Logic are provided by the Transmit Bit/Frame/Multiframe Control (Transmit Timing Control) to determine the proper insertion points for the CRC-4 bits if CRCEN is HIGH. The Transmit Timing Control also properly times insertion of the spare bits. If CRCEN is LOW, there will be no insertion of CRC-4 bits into the transmitted bit stream, and the spare bits are accessed through the Bt8070 instead of through the Bt8075. In this condition, the CRC-4 is not implemented.

The output of Transmit Logic to the system is TNRZO which is the Transmit NRZ Data that have been CRC-4 encoded and have spare bits inserted at the proper time (if CRCEN is HIGH). This is a regenerated signal derived from the TNRZ signal from the Bt8070, which is unchanged if CRCEN is LOW. This signal, regardless of whether the Bt8075 is enabled or disabled, is used to replace the Bt8070 TNRZ signal as an output to the system. TNRZO is also an input to the HDB3 Encoder, which generates the Transmit Unipolar Data (TPOS and TNEG). There is a 6-bit throughout delay between TNRZ input and TPOS/TNEG outputs.

CRC-4 Encoder

The CRC-4 Encoder calculates the CRC-4 polynomial and provides the CRC-4 bits for insertion into the transmitted bit stream. This insertion is performed at the proper time by the Transmit Logic. The CRC-4 Encoder may be disabled for transparent operation without CRC-4 computation by CRCEN set LOW.

The data input to the CRC-4 Encoder section are the Non-Return-to-Zero (TNRZ) output for transmitted data from the Bt8070. Control and timing inputs to the CRC-4 Encoder are provided by the Transmit Bit/Frame/Multiframe Control (Transmit Timing Control) to determine the proper insertion points for the CRC-4 bits if CRCEN is high. This information is generated using TMAX (from Bt8070) to derive multiframe timing and CRCEN (from system) to decide whether to compute CRC-4.

The output of the CRC-4 Encoder goes through a holding register into the Transmit Logic for insertion of the CRC-4 bits (if CRCEN is HIGH) into the Transmit bit stream. (See Figures 5, 6, 7.)

HDB3 Encoder

The HDB3 Encoder takes the Transmit NRZ data provided by the Transmit Logic and provides HDB3 encoding. The resulting output is the two unipolar signals TPOS and TNEG which go to the Bt8069 for transmission onto the PCM–30 line.

Data input to the HDB3 Encoder are the TNRZ0 output of the Transmit Logic of the Bt8075. This signal already has CRC-4 and spare bits inserted as appropriate. The TNRZ0 data are converted to a set of unipolar signals (TPOS, TNEG) using HDB3 encoding for unipolar PCM–30 data.

The output of the HDB3 Encoder is the set of Transmit Unipolar signals (TPOS and TNEG). These signals go directly to the Bt8069 for transmission onto the PCM–30 line. These signals also are provided to the HDB3 decoder section for use during loopback operation.

Functional Description *(continued)*

Transmit Bit/Frame/Multiframe Control (Transmit Timing Control)

Transmit timing is provided to properly handle insertion of CRC-4 bits and spare bits into the outgoing transmit bit stream. This block provides timing and control to the CRC-4 Encoder and Transmit Logic sections. It also provides the Transmit Multiframe Alignment Sync (TMASYN) signal to the system allowing the system to properly align on multiframe boundaries.

Inputs to this block are TCLK (from Bt8069), TMAX (from Bt8070) and CRCEN (from system). If CRCEN is high, the control is provided to the Transmit Logic to implant the CRC-4 and spare bits into the transmit bit stream. TCLK is used to derive the bit timing; TMAX is used to derive the frame and multiframe timing (see Figure 5).

The CRC-4 bits are inserted in the even frames in the bit 1 position of these frames. There are four CRC-4 bits in each 8-frame Sub-MultiFrame (SMF). In odd frames, bit 1 of the first six frames of each 16-frame MultiFrame (MF) contains the CRC multiframe alignment signal (001011). Bit 1 of the last two odd frames of the multiframe (Frame 13, 15) contains the spare bits. Access to the international bit (bit 1 of each frame) is provided through the Bt8070 when the Bt8075 in CRC-4 disable mode (see Figure 8).

Outputs from this block are the timing and controls described previously and the Transmit Multiframe Alignment Sync (TMASYN) signal. TMASYN is an output to the system which indicates the beginning of the transmitted CRC-4 multiframe. It is a positive pulse of one TCLK period in duration. (See Figures 6 and 7.)

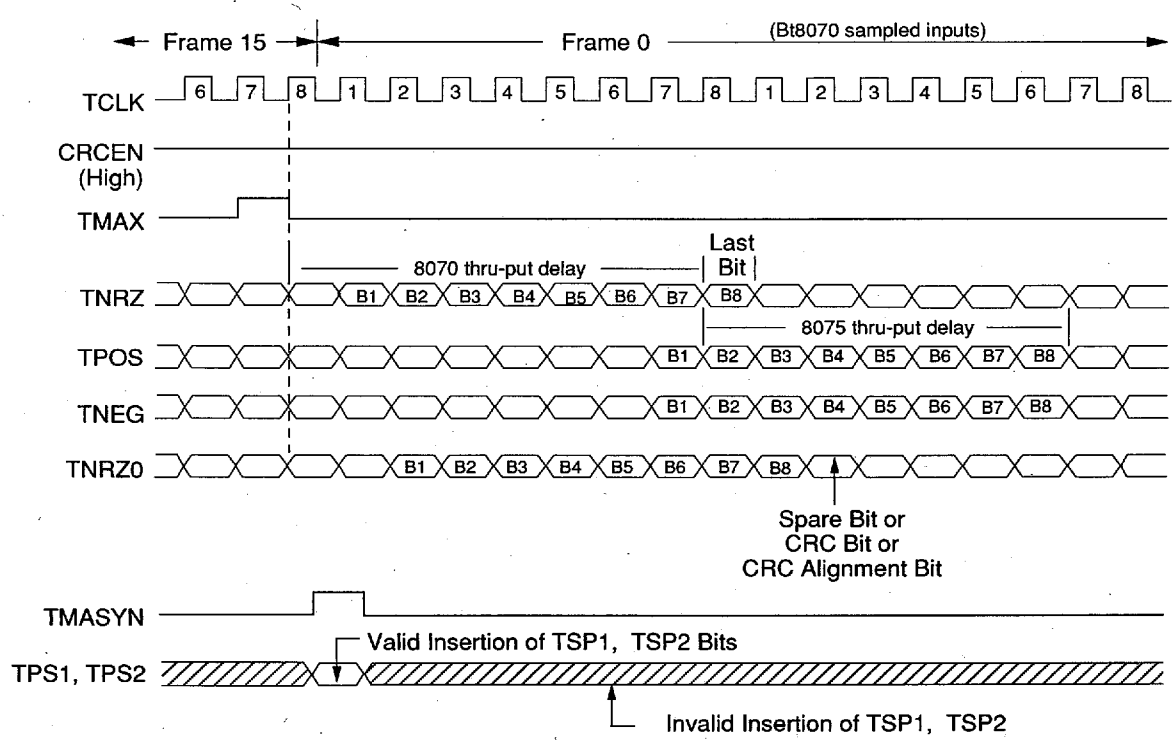


Figure 5. Bt8075 Transmit Timing

Functional Description *(continued)*

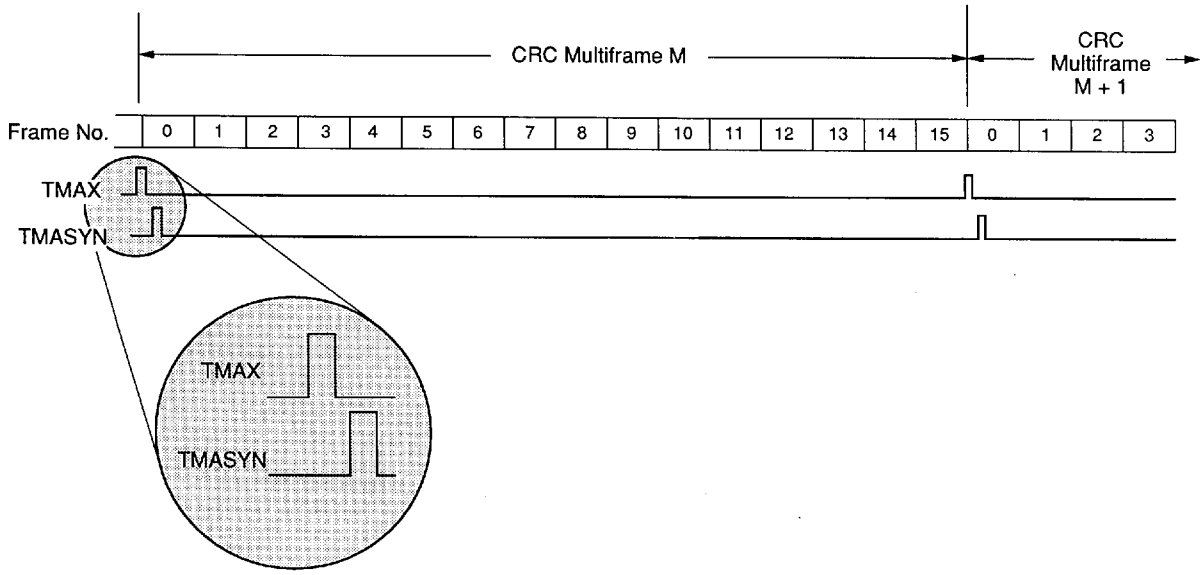


Figure 6. Transmit CRC Multiframe-Bt8070 Mode 256S.

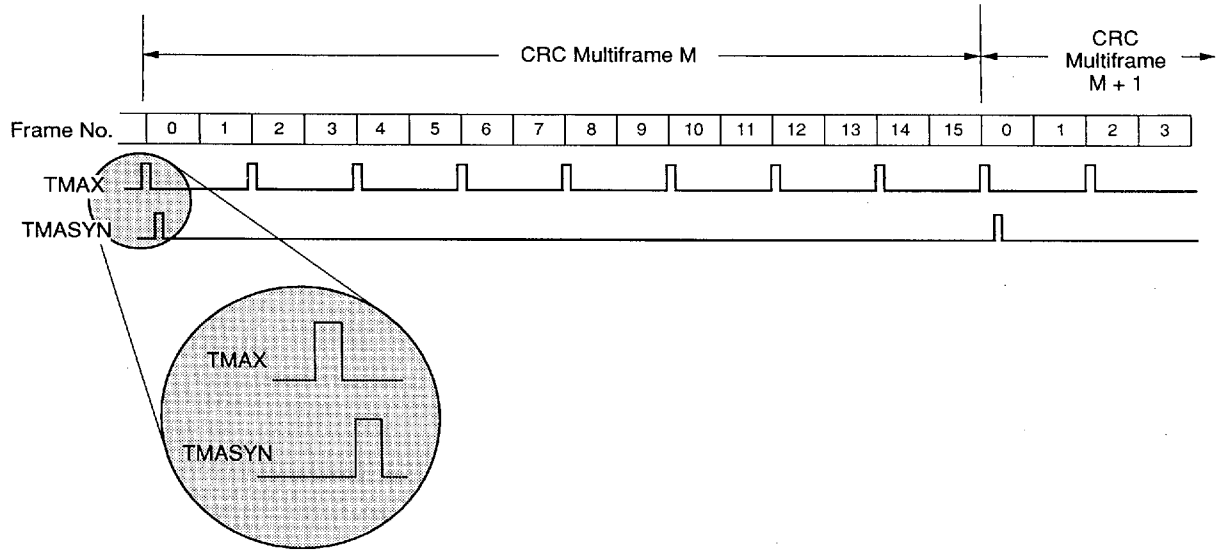


Figure 7. Transmit CRC Multiframe-Bt8070 Mode 256N

Functional Description *(continued)*

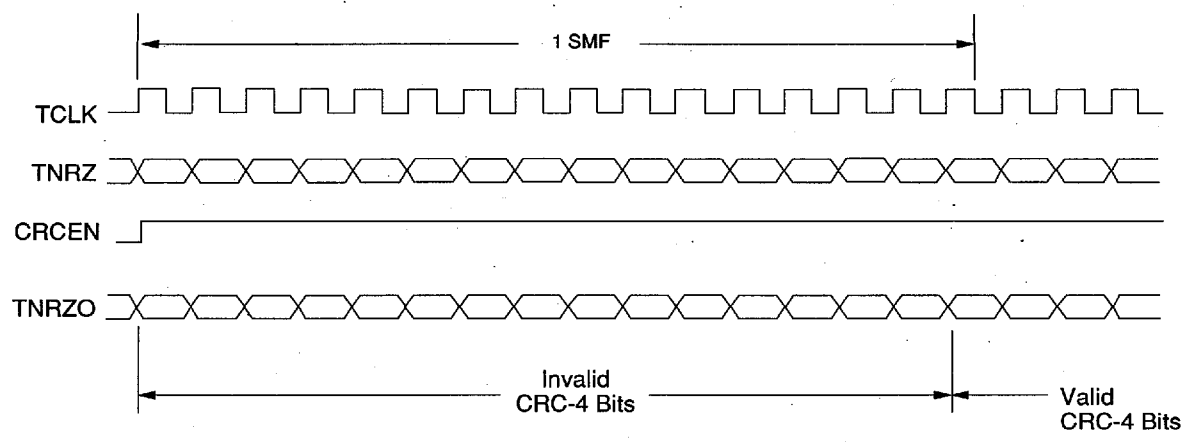


Figure 8. CRC-4 Output Timing

Receive Section

The Receive section provides independent error detection/reporting of the CRC-4 and Multiframe Alignment errors, extraction of the spare bits, and HDB3 decoding with reporting of bipolar violations. The Bt8075 Receive section also provides Receive NRZ Data (RNRZ) to the Bt8070, connected to the Bt8070 RPOS, RNEG inputs. This connection will bypass the HDB3 Encoder and Decoder sections of the Bt8070, along with the Bt8070 bipolar violations detector. These functions are replaced by the Transmit and Receive sections of the Bt8075.

The five inputs to the Bt8075 Receive section are: Receive Unipolar Data (RPOS, RNEG, RCLK) from the Bt8069, Receive Sync (RSYNC) from the Bt8070, and Loopback Mode (LOOP) from the system. There is a 6-bit throughput delay between RPOS/RNEG inputs and RNRZ output. Also, the international bit is internally sampled (after a 21-bit delay from the RPOS/RNEG inputs) in order to calculate the CRC bits.

The seven outputs from the Bt8075 Receive section are: Receive NRZ Data (RNRZ) to the Bt8070, and the Bt8075 outputs to the system. These are CRC-4 Error (CRCERR), Multiframe Alignment Error (MFAERR), Receive Multiframe Alignment Sync (RMASYN), Bipolar Violations (BPV), and Receive Spare Bits (RSP1, RSP2).

The Receive section has the following functional blocks:

1. Internal RCLK Regenerator
2. HDB3 Decoder
3. CRC-4 Decoder
4. Alignment and Error Control
5. Receive Bit/Frame/Multiframe Control (Receive Timing Control)

Internal RCLK Generator

This block takes the RCLK and TCLK from the Bt8069, along with the LOOP control from the system and produces the internal RCLK timing. This RCLK provides master bit timing for the other blocks of the Receive section of the Bt8075.

HDB3 Decoder

The HDB3 Decoder takes the RPOS and RNEG from the Bt8069 and generates the RNRZ output to the Bt8070 and identifies Bipolar Violations (BPV) for output to the system.

Inputs to this block are the RPOS and RNEG (from Bt8069), TPOS and TNEG (from Bt8075 HDB3 Encoder Block), the LOOP control (from system), and the Internal RCLK (from Internal RCLK). Using the LOOP and TPOS/TNEG signals, if the loopback

Functional Description *(continued)*

mode is enabled (LOOP = HIGH), the TPOS and TNEG signals generated in the Bt8075 HDB3 Encoder are routed to the RPOS/RNEG inputs of the HDB3 Decoder. This function replaces the equivalent Bt8070 function.

Outputs from this block are RNRZ (to the Bt8070) and BPV (to system). The RNRZ is generated according to the HDB3 format, and sent to the Bt8070 RPOS/RNEG inputs, bypassing the Bt8070's HDB3 encode and decode functions. According to the HDB3 algorithm, bipolar violations are detected and reported through the BPV (system output). After HDB3 decodes the receive data, it is passed to the CRC-4 Decoder and the Alignment/Error Control blocks. Tying Bt8075 RPOS and RNEG inputs together will disable the HDB3 Decode section.

CRC-4 Decoder

The RNRZ output of the HDB3 Decoder, the internal RCLK, and the RSYNC timing are inputs to the CRC-4 Decoder. At the end of every SMF, the current frame CRC-4 result computed by the CRC-4 Decoder block is clocked into a temporary holding register. During the following SMF, the incoming CRC-4 bits on RSER are compared with the contents of the holding register. If a mismatch occurs, the CRC-4 error signal (CRCERR) is generated in the Alignment/Error Control block. Timing is generated by the Receive Bit/Frame/Multiframe Control block. (See Figures 9 and 10.)

Alignment/Error Control

This block generates the Receive Multiframe Alignment Sync (RMASYN) signal output to the system, outputs the receive spare bits (RSP1, RSP2), and generates the error signals Multiframe Alignment Error (MFAERR) and CRC-4 error (CRCERR) output to the system.

Handling of the errors is a system function to be done in accordance with CCITT Standard G70X and Recommendation I.431.

Inputs to the Alignment/Error Control block are the internally generated RCLK, the RNRZ data from the HDB3 Decoder block, the contents of the CRC-4 holding register, and timing signals from the Receive Bit/Frame/Multiframe Control block.

While the CRCERR and MFAERR are closely related, they are independently generated. CRCERR is generated upon a mismatch between the incoming CRC bits from RSER and the previous SMF's CRC result from the previous SMF found in the holding register. This can occur due to an incidental data error or by a loss of frame alignment. This signal is valid for the entire SMF, resetting at the end of each SMF. MFAERR is generated when there is a miss in the CRC-4 alignment bits, indicating each instance of multiframe alignment error. It is valid during each MF, and is reset when the CRC-4 alignment is regained. This signal is useful to the system for implementing alarm handling.

RMASYN is derived from the RCLK. It is a positive pulse of one RCLK period in length, and indicates the beginning of the received CRC-4 multiframe. This section also extracts the spare bits (RSP1 and RSP2), making them available to the system at the beginning of each multiframe (at RMASYN).

Receive Bit/Frame/MF Control (Receive Timing Control)

This block takes RSYNC from the Bt8070, the internally generated RCLK, and a sync valid signal generated by the Alignment/Error Control to generate timing for the CRC-4 Decoder and the bit timing for the Alignment/Error Control. This block generates internal timing. It has no off-chip outputs. (See Figures 11, 12, and 13 and Table 3.)

Functional Description *(continued)*

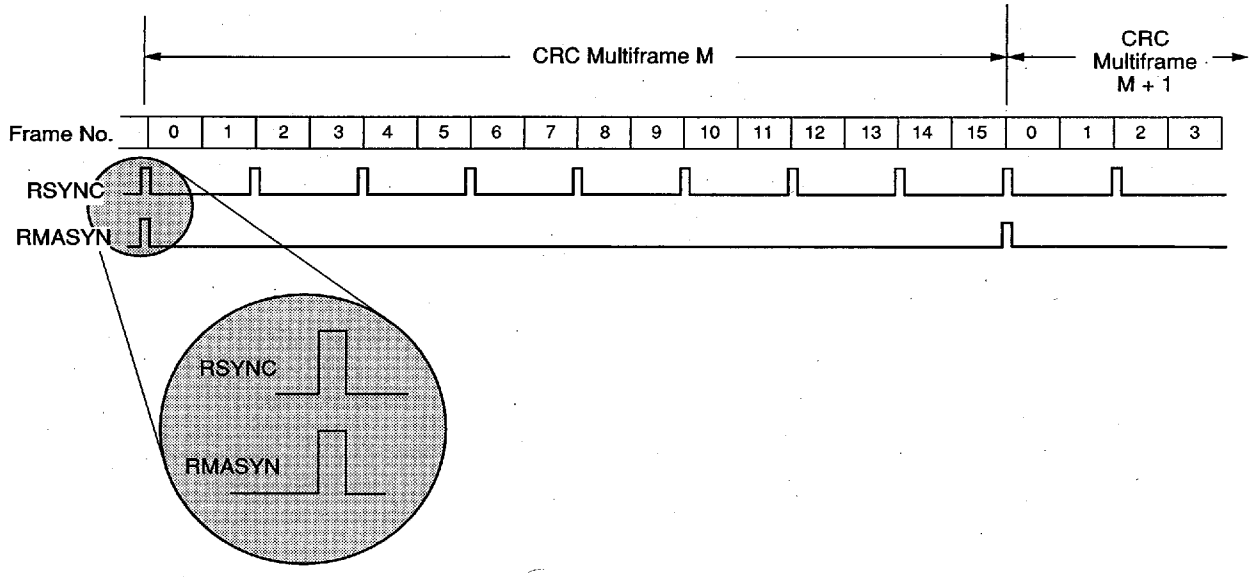


Figure 9. Receive CRC Multiframe-Bt8070 Mode 256S

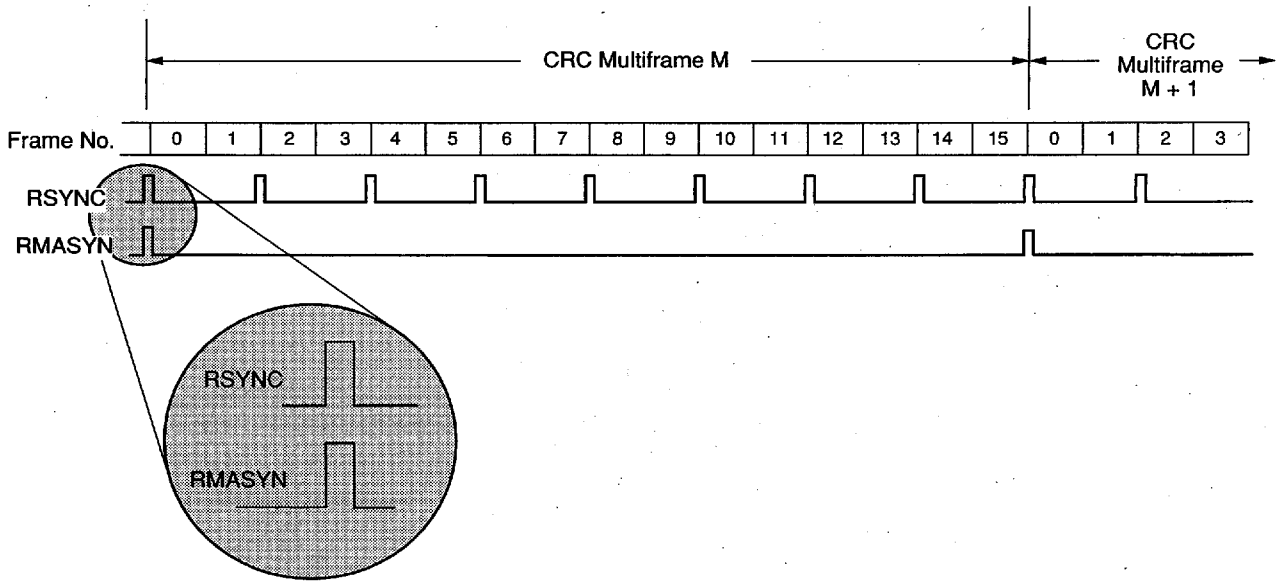


Figure 10. Receive CRC Multiframe-Bt8070 Mode 256N

Functional Description *(continued)*

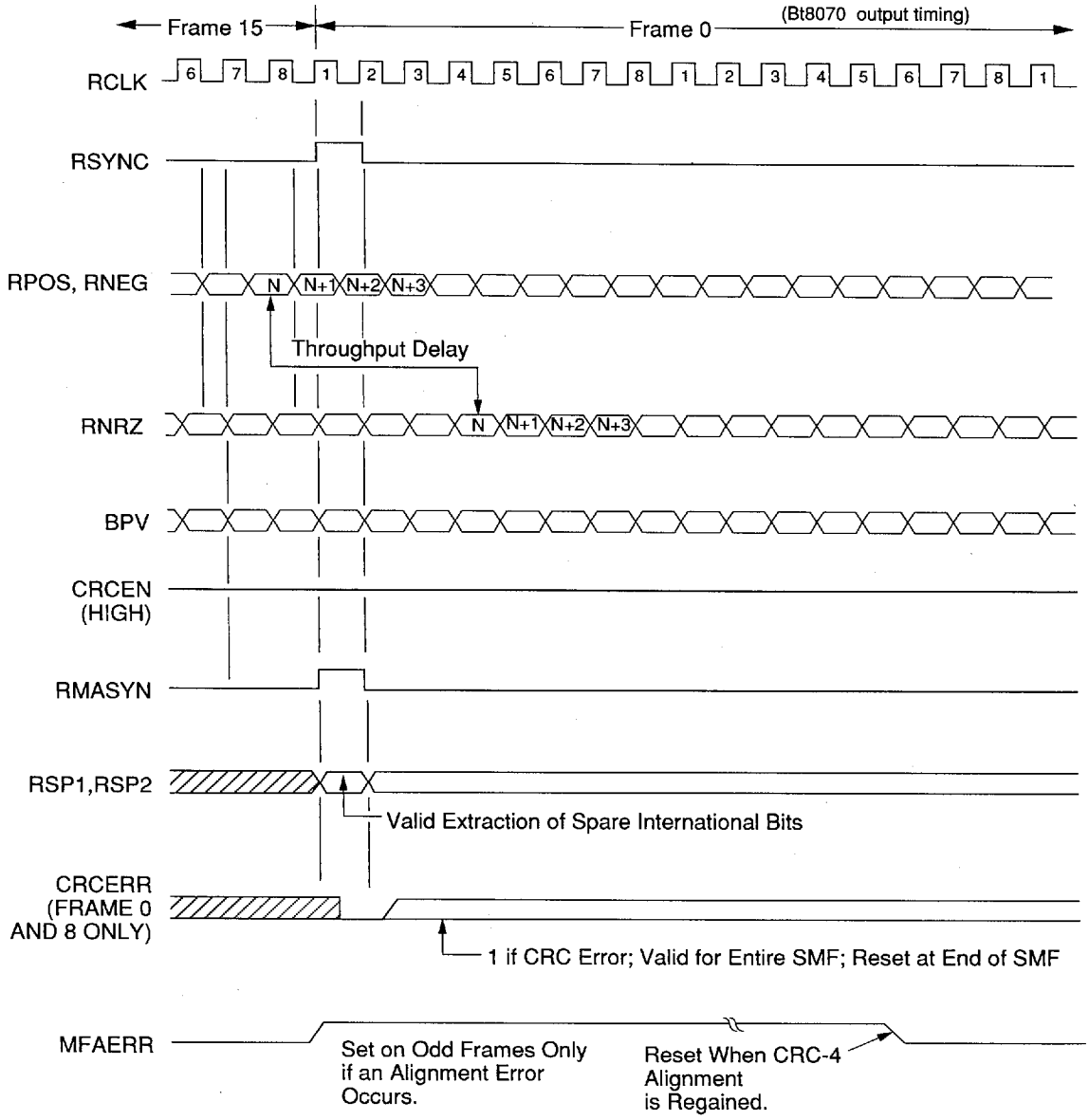
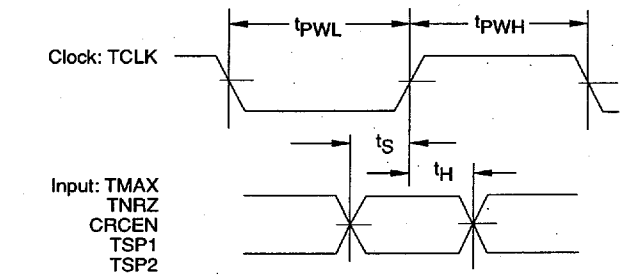
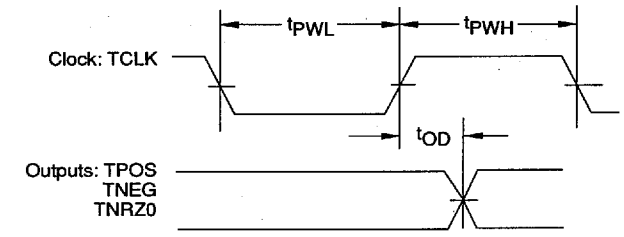


Figure 11. Bt8075 Receive Timing

Receive Section *(Continued)*





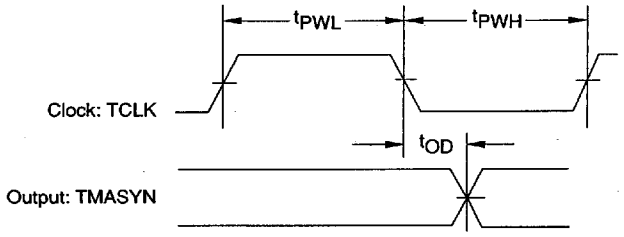
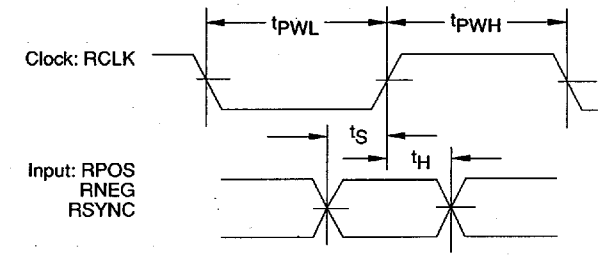
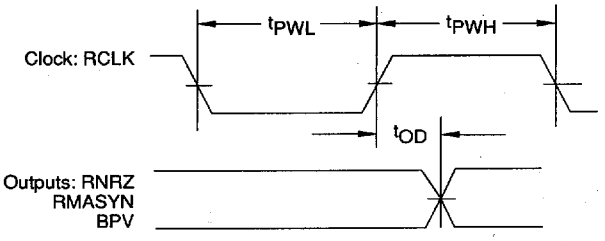


Figure 12. TCLK Input/Output Timing





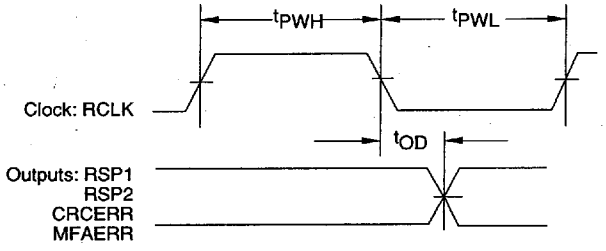


Figure 13. RCLK Input/Output Timing

Parameter	Symbol	Min.	Typ.	Max.	Units
Clock Pulse Width High, Low	t_{PWH}, t_{PWL}	200	244	–	ns
Input Setup Time	t_S	30	–	–	ns
Input Hold Time	t_H	0	–	–	ns
Output Delay Time	t_{OD}	–	–	60	ns

Table 3. Input and Output Timing

Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to Vcc +0.3	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	-55 to +150	°C

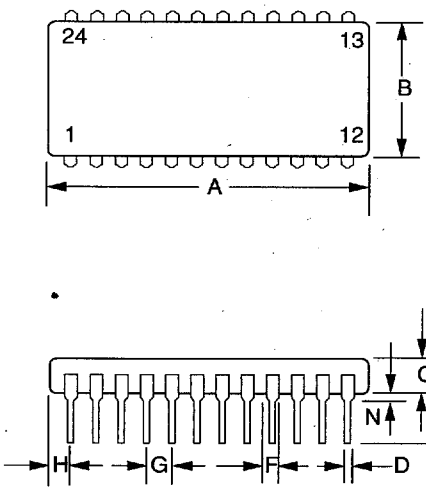
Note. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Operating Characteristics

V_{CC} = 5.0 Vdc ±5%, Vss = 0 Vdc, T_A = 0°C to 70°C, unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Condition
Input Low Voltage	V_{IL}	–0.3	–	+0.8	V	
Input High Voltage	V_{IH}	+2.0	–	VCC +0.3	V	
Output Low Voltage	V_{OL}	–	–	+0.4	V	I_{LOAD} = 1.6 mA
Output High Voltage						
TTL	V_{OH}	+2.4	–	–	V	I_{LOAD} = –100 µA
CMOS	V_{OH}	+3.5	–	–	V	I_{LOAD} = –100 µA
Output Low Current	I_{OL}	–1.6	–	–	mA	V_{OL} = 0.4V
Output High Current	I_{OH}	–100	–	–	µA	V_{OH} = 2.4V
Input Capacitance	C_{IN}	–	–	5	pF	
Power Dissipation	P_D	–	–	100	mW	

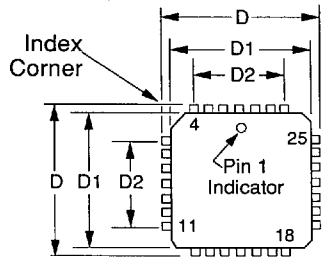
Package Dimensions



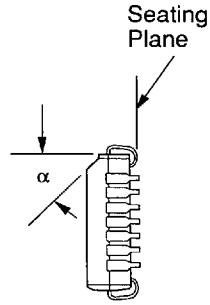
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	31.24	32.00	1.230	1.260
B	13.46	13.97	0.530	0.550
C	3.56	4.06	0.140	0.160
D	0.38	0.53	0.015	0.021
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040
REF: PD24P/GP00-D132				

24-Pin Plastic DIP

Package Dimensions

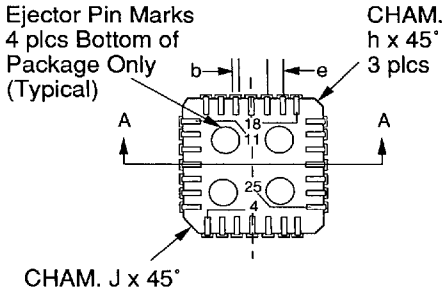


Top View

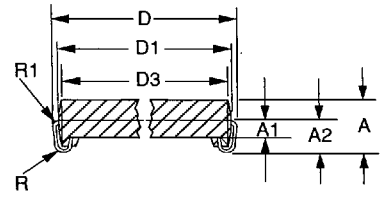


Side View

DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	4.14	4.29	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	12.37	12.52	0.487	0.493
D1	11.43	11.53	0.450	0.454
D2	7.54	7.70	0.297	0.303
D3	10.67 REF		0.420 REF	
e	1.27 BSC		0.050 BSC	
h	1.15 TYP		0.045 TYP	
J	0.25 TYP		0.010 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.25 TYP		0.010 TYP	



Bottom View



Section A-A

Typ for Both Axis
(Except for Beveled Edge)

28-Pin PLCC

Ordering Information

Part Number	Paclage	Temperature Range
Bt8075KP	24-Pin Plastic DIP	0° C to 70°C
Bt8075KPJ	28-Pin Plastic Leaded Chip Carrier (PLCC)	0°C to 70°C