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TRIPLE 2-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER

The HEF4053B is a triple 2-channel analogue multiplexer/demultiplexer with a common enable input ($\overline{E}$). Each multiplexer/demultiplexer has two independent inputs/outputs (Y_0 and Y_1), a common input/output (Z), and select inputs (S_n). Each also contains two-bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 and Y_1) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the two switches is selected (low impedance ON-state) by S_n. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_A to S_C.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S_A to S_C and $\overline{E}$). The V_{DD} to V_{SS} range is 3 to 15 V. The analogue inputs/outputs (Y_0, Y_1 and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

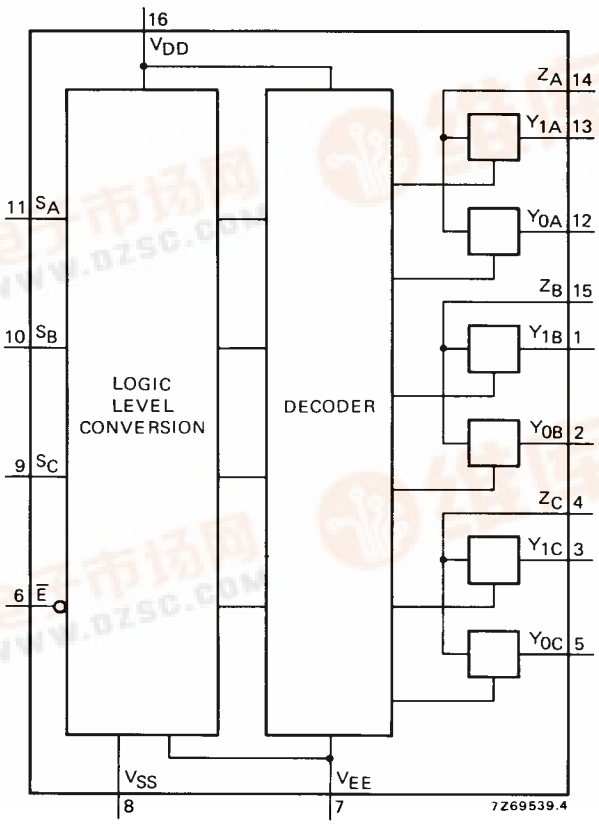

Fig. 1 Functional diagram.

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

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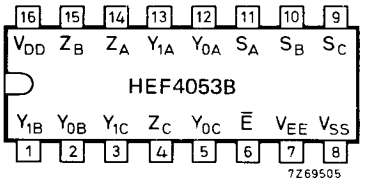

Fig. 2 Pinning diagram.

PINNING

Y_{0A} to Y_{0C}	independent inputs/outputs
Y_{1A} to Y_{1C}	independent inputs/outputs
S_A to S_C	select inputs
$\overline{E}$	enable input (active LOW)
Z_A to Z_C	common inputs/outputs

HEF4053BP : 16-lead DiL; plastic (SOT-38Z).
HEF4053BD: 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4053BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

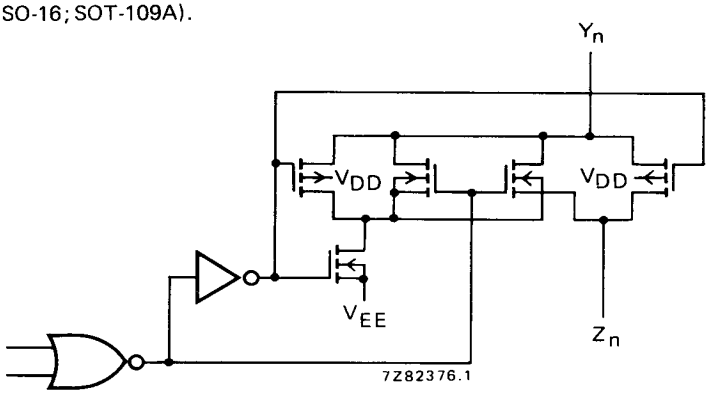

Fig. 3 Schematic diagram (one switch).

FUNCTION TABLE

inputs		channel ON
$\overline{E}$	S_n	
L	L	Y_{0n}–Z_n
L	H	Y_{1n}–Z_n
H	X	none

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to V_{DD}) V_{EE} −18 to + 0,5 V

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{EE}.

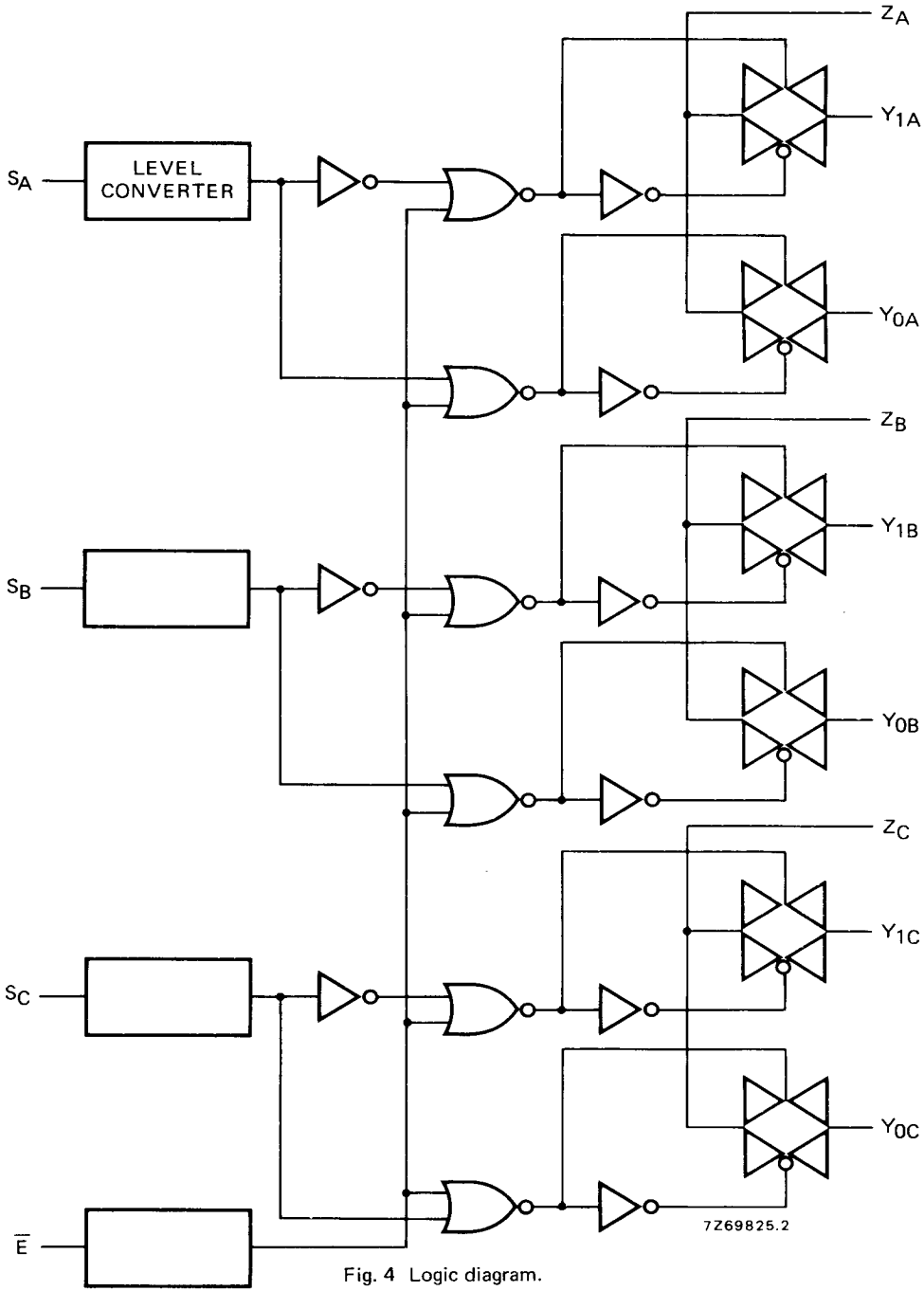

Fig. 4 Logic diagram.

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	$V_{DD}-V_{EE}$ V	symbol	typ.	max.		conditions
ON resistance	5	R_{ON}	350	2500	Ω	V_{is} = 0 to $V_{DD}-V_{EE}$ see Fig. 6
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R_{ON}	115	340	Ω	V_{is} = 0 see Fig. 6
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R_{ON}	120	365	Ω	V_{is} = $V_{DD}-V_{EE}$ see Fig. 6
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	25	–	Ω	V_{is} = 0 to $V_{DD}-V_{EE}$ see Fig. 6
	10		10	–	Ω	
	15		5	–	Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	–	–	nA	$\overline{E}$ at V_{DD}
	10		–	–	nA	
	15		–	1000	nA	
OFF-state leakage current, any channel	5	I_{OZY}	–	–	nA	$\overline{E}$ at V_{SS}
	10		–	–	nA	
	15		–	200	nA	

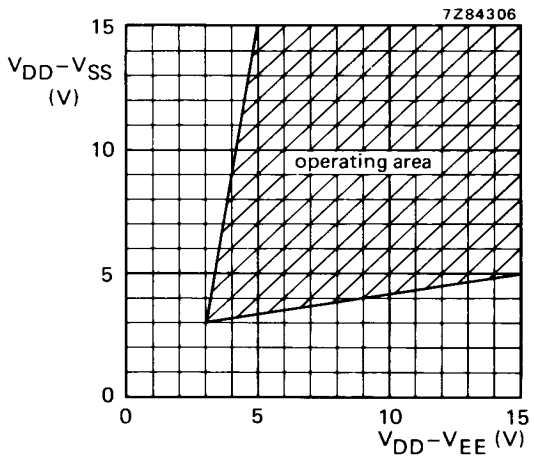

Fig. 5 Operating area as a function of the supply voltages.

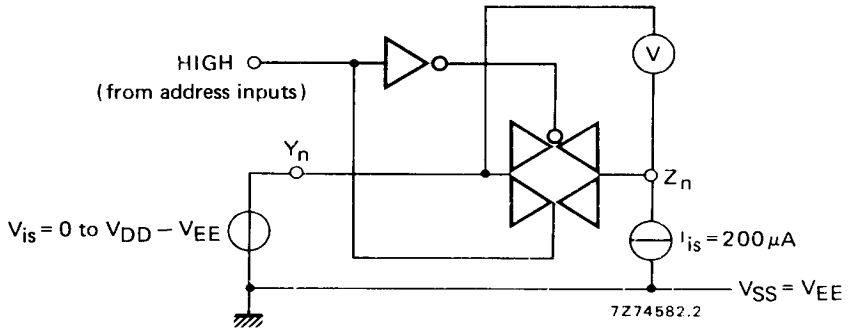

Fig. 6 Test set-up for measuring R_{ON}.

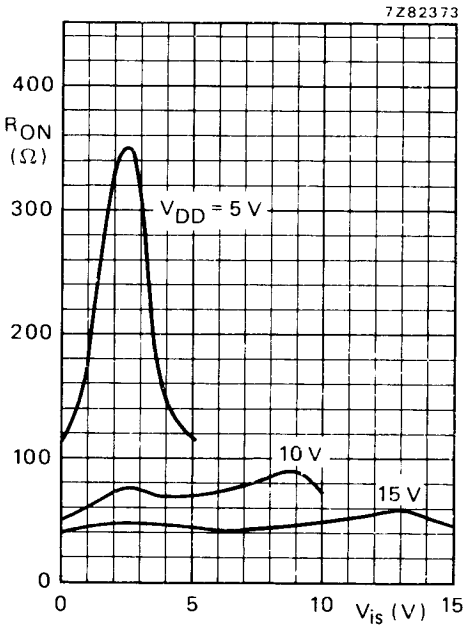

Fig. 7 Typical R_{ON} as a function of input voltage.

I_{is} = 200 μA
$V_{SS} = V_{EE}$ = 0 V

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$11\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$29\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		
Propagation delays						
$V_{is} \rightarrow V_{os}$						
HIGH to LOW	5	t_{PHL}	10	20	ns	note 1
	10		5	10	ns	
	15		5	10	ns	
LOW to HIGH	5	t_{PLH}	15	30	ns	note 1
	10		5	10	ns	
	15		5	10	ns	
$S_n \rightarrow V_{os}$						
HIGH to LOW	5	t_{PHL}	200	400	ns	note 2
	10		85	170	ns	
	15		65	130	ns	
LOW to HIGH	5	t_{PLH}	275	555	ns	note 2
	10		100	200	ns	
	15		65	130	ns	
Output disable times						
$\overline{E} \rightarrow V_{os}$						
HIGH	5	t_{PHZ}	200	400	ns	note 3
	10		115	230	ns	
	15		110	220	ns	
LOW	5	t_{PLZ}	200	400	ns	note 3
	10		120	245	ns	
	15		110	215	ns	
Output enable times						
$\overline{E} \rightarrow V_{os}$						
HIGH	5	t_{PZH}	260	525	ns	note 3
	10		95	190	ns	
	15		65	130	ns	
LOW	5	t_{PZL}	280	565	ns	note 3
	10		105	205	ns	
	15		70	140	ns	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.	
Distortion, sine-wave response	5		0,25	%	note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		–	MHz	note 5
	10		1	MHz	
	15		–	MHz	
Crosstalk; enable or address input to output	5		–	mV	note 6
	10		50	mV	
	15		–	mV	
OFF-state feed-through	5		–	MHz	note 7
	10		1	MHz	
	15		–	MHz	
ON-state frequency response	5		13	MHz	note 8
	10		40	MHz	
	15		70	MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. $R_L = 10$ kΩ to V_{EE}; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{SS}$; $V_{is} = V_{DD}$ (square-wave); see Fig. 8.
2. $R_L = 10$ kΩ; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{SS}$; $S_n = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PLH}; $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PHL}; see Fig. 8.
3. $R_L = 10$ kΩ; $C_L = 50$ pF to V_{EE}; $\overline{E} = V_{DD}$ (square-wave);
   $V_{is} = V_{DD}$ and R_L to V_{EE} for t_{PHZ} and t_{PZH};
   $V_{is} = V_{EE}$ and R_L to V_{DD} for t_{PLZ} and t_{PZL}; see Fig. 8.
4. $R_L = 10$ kΩ; $C_L = 15$ pF; channel ON; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$); $f_{is} = 1$ kHz; see Fig. 9.
5. $R_L = 1$ kΩ; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$);
   $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 10.
6. $R_L = 10$ kΩ to V_{EE}; $C_L = 15$ pF to V_{EE}; $\overline{E}$ or $S_n = V_{DD}$ (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig. 8.
7. $R_L = 1$ kΩ; $C_L = 5$ pF; channel OFF; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$);
   $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 9.
8. $R_L = 1$ kΩ; $C_L = 5$ pF; channel ON; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$);
   $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 9.

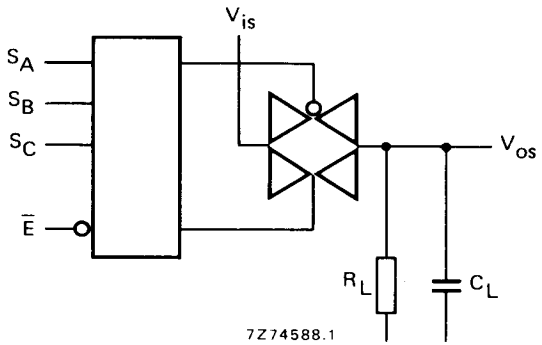

Fig. 8.

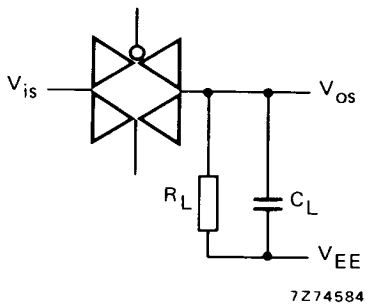

Fig. 9.

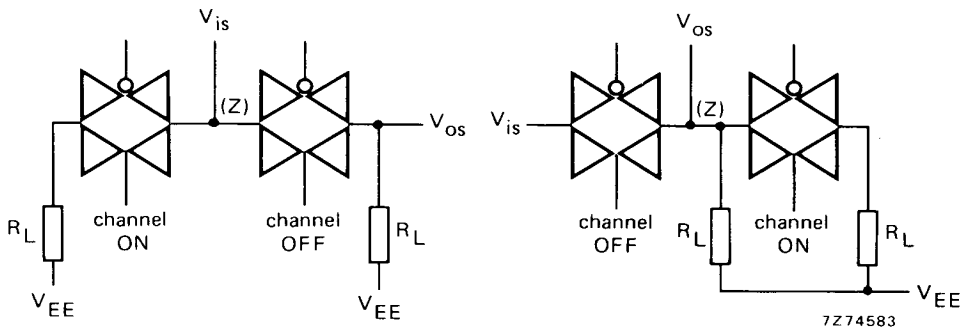

Fig. 10.

APPLICATION INFORMATION

Some examples of applications for the HEF4053B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.