Siliconix

SUP/SUB60N06-14

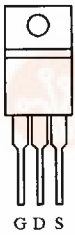
N-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.014	60[a]

TO-220AB



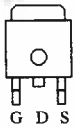
G D S

Top View

SUP60N06-14

DRAIN connected to TAB

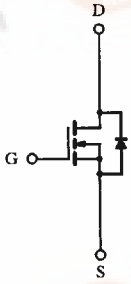
TO-263



G D S

Top View

SUB60N06-14



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (T_J = 175°C)	T_C = 25°C	I_D	60[a]	A
	T_C = 100°C		42	
Pulsed Drain Current		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Repetitive Avalanche Energy[b]	L = 0.1 mH	E_{AR}	180	mJ
Power Dissipation	T_C = 25°C (TO-220AB and TO-263)	P_D	100	W
	T_A = 25°C (TO-263)[c]		3.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount (TO-263)[c]	R_{thJA}	40	°C/W
	Free Air (TO-220AB)		80	
Junction-to-Case		R_{thJC}	1.5	

Notes:
a. Package limited.
b. Duty cycle ≤ 1%.
c. When mounted on 1" square PCB (FR-4 material).

(05/16/94)

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_{DS} = 1 mA	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C			250	
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	60			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A			0.014	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C			0.023	
		V_{GS} = 10 V, I_D = 30 A, T_J = 175°C			0.028	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 30 A		TBD		S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		TBD		pF
Output Capacitance	C_{oss}			TBD		
Reversen Transfer Capacitance	C_{rss}			TBD		
Total Gate Charge[c]	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 60 A		TBD	130	nC
Gate-Source Charge[c]	Q_{gs}			TBD		
Gate-Drain Charge[c]	Q_{gd}			TBD		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.47 Ω I_D ≅ 60 A, V_{GEN} = 10 V, R_G = 2.5 Ω		TBD	30	ns
Rise Time[c]	t_r			TBD	180	
Turn-Off Delay Time[c]	$t_{d(off)}$			TBD	100	
Fall Time[c]	t_f			TBD	50	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)[a]						
Continuous Current	I_s				60	A
Pulsed Current	I_{SM}				240	
Forward Voltage[b]	V_{SD}	I_F = 60 A, V_{GS} = 0 V			1.8	V
Reverse Recovery Time	t_{rr}	I_F = 60 A, di/dt = 100 A/µs		TBD		ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			TBD		A
Reverse Recovery Charge	Q_{rr}			TBD		µC

Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.