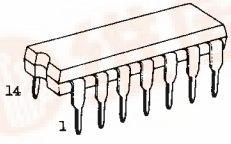
TC7400BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC7400BP QUAD 2-INPUT POSITIVE NAND GATE

TC7400BP is two input positive logic NAND gate. Since all the outputs of this gate are equiped with buffers which consist of inverters, the input/output transmission characteristic has been improved and the variation of transmission time caused by increase of load capacity has been kept minimum.



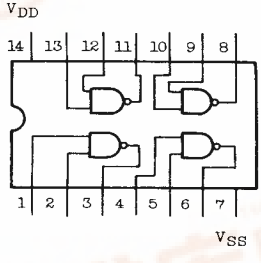
DIP 14 (3D14A-P)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	Tstg	-65 ~150	°C
Lead Temp./Time	Tsol	260°C · 10sec	

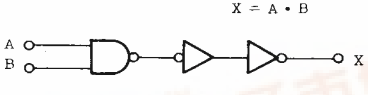
PIN ASSIGNMENT

TC7400BP



LOGIC DIAGRAM

1/4 TC7400BP



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temp.	Topr		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
"H" Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
"L" Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
"H" Level Output Current	I_{OH}	V_{OH} = 4.6V V_{OH} = 9.5V V_{OH} = 13.5V $V_{IN} = V_{SS}, V_{DD}$	5	-0.2	-	-0.16	-0.5	-	-0.12	-	mA
			10	-0.5	-	-0.4	-1.2	-	-0.3	-	
			15	-1.4	-	-1.2	-6.0	-	-1.0	-	
"L" Level Output Current	I_{OL}	V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V $V_{IN} = V_{DD}$	5	0.52	-	0.44	1.5	-	0.36	-	
			10	1.3	-	1.0	3.5	-	0.9	-	
			15	3.6	-	3.0	15	-	2.4	-	
"H" Level Input Voltage	V_{IH}	V_{OUT}=0.5V,4.5V V_{OUT}=1.0V,9.0V V_{OUT}=1.5V,13.5V $\|I_{OUT}\| < 1\mu A$	5	3.5	-	3.5	2.75	-	3.5	-	V
			10	7.0	-	7.0	5.5	-	7.0	-	
			15	11.0	-	11.0	8.25	-	11.0	-	
"L" Level Input Voltage	V_{IL}	V_{OUT}= 4.5V V_{OUT}= 9.0V V_{OUT}= 13.5V $\|I_{OUT}\| < 1\mu A$	5	-	1.5	-	2.25	1.5	-	1.5	
			10	-	3.0	-	4.5	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
Input Current "H" Level	I_{IH}	V_{IH} = 18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL} = 0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ *	5	-	1.0	-	0.001	1.0	-	7.5	μA
			10	-	2.0	-	0.001	2.0	-	15	
			15	-	4.0	-	0.002	4.0	-	30	

* All valid input combinations

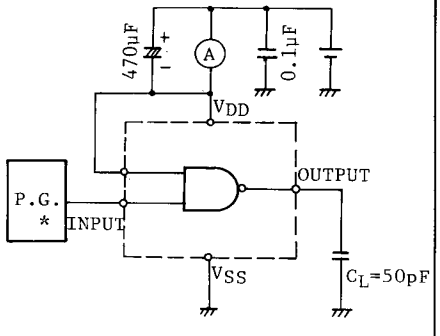
SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_{TLH}		5	-	130	400	ns
			10	-	65	200	
			15	-	50	160	
Output Fall Time	t_{THL}		5	-	100	200	
			10	-	50	100	
			15	-	40	80	

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}-OV, C_L=50pF)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
TC7400BP	(Low-High) Propagation Delay Time	t_{pLH}		5 10 15	- - -	140 60 50	300 150 125	ns
	(High=Low) Propagation Delay Time	t_{pHL}		5 10 15	- - -	180 80 60	300 150 125	
Input Capacitance		C_{IN}			-	5	7.5	pF

I_T TEST CIRCUIT



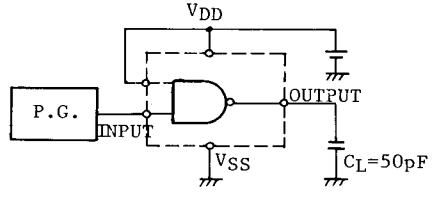
* INPUT PULSE CONDITION

DUTY RATIO = 50%

$t_r=t_f$=20ns

SWITCHING TIME TEST CIRCUIT AND WAVEFORM

TEST CIRUCIT



WAVEFORM