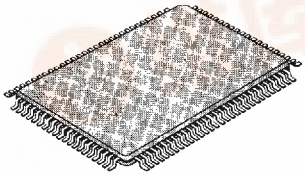
## 80-CHANNEL SEGMENT/COMMON DRIVER FOR DOT MATRIX LCD

KS0083/84 is a graphic type LCD driver LSI which is fabricated by CMOS process for high voltage. In case of segment driver, can be selected 4 bit, 1 bit data transfer or chip select mode. KS0084 is reverse type of KS0083

100 QFP



## FUNCTION

- **DOT MATRIX LCD DRIVER with 80 channel output.**
- **Input/Output**
  - **Output: 80 channel waveform for LCD driving**
  - **Input: • parallel display data and control signal from controller**
    **• bias voltage ($V_3$, $V_4$, $V_{SS}$)**

## FEATURES

- **Power supply voltage: −5V ± 10%**
- **LCD driving voltage: -24V(typ) ($V_{EE}$)**
- **Interface**

| type 1 | | type 2 | | type 3 | |
|---|---|---|---|---|---|
| COM | SEG | COM | SEG | COM | SEG |
| KS0083/84 | KS0083/84 | KS0103 | KS0083/84 | KS0083/84 | KS0104 |

- **100QFP and bare chip available**

## BLOCK DIAGRAM

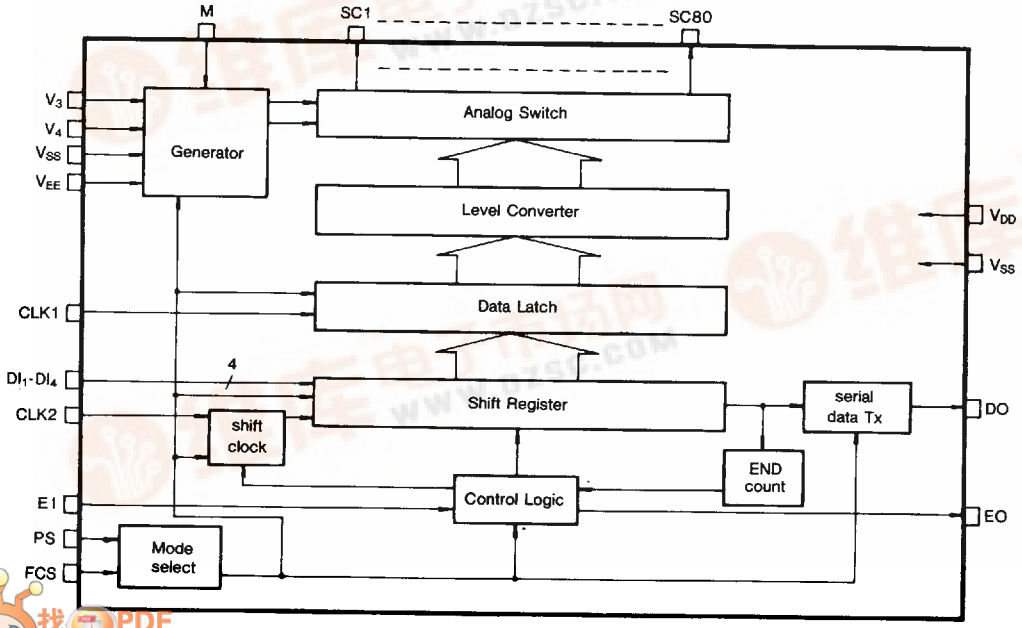



Fig. 1 KS0083/84 functional block diagram.

## PIN CONFIGURATION

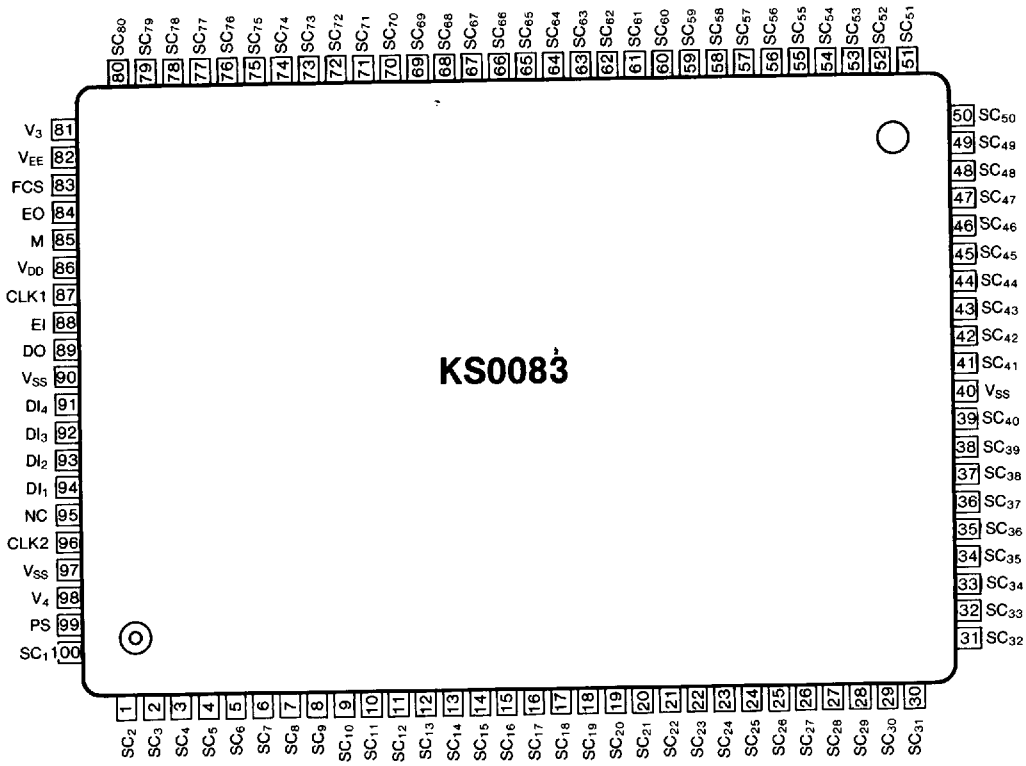



Fig. 2. 100 QFP Top View

## PIN CONFIGURATION

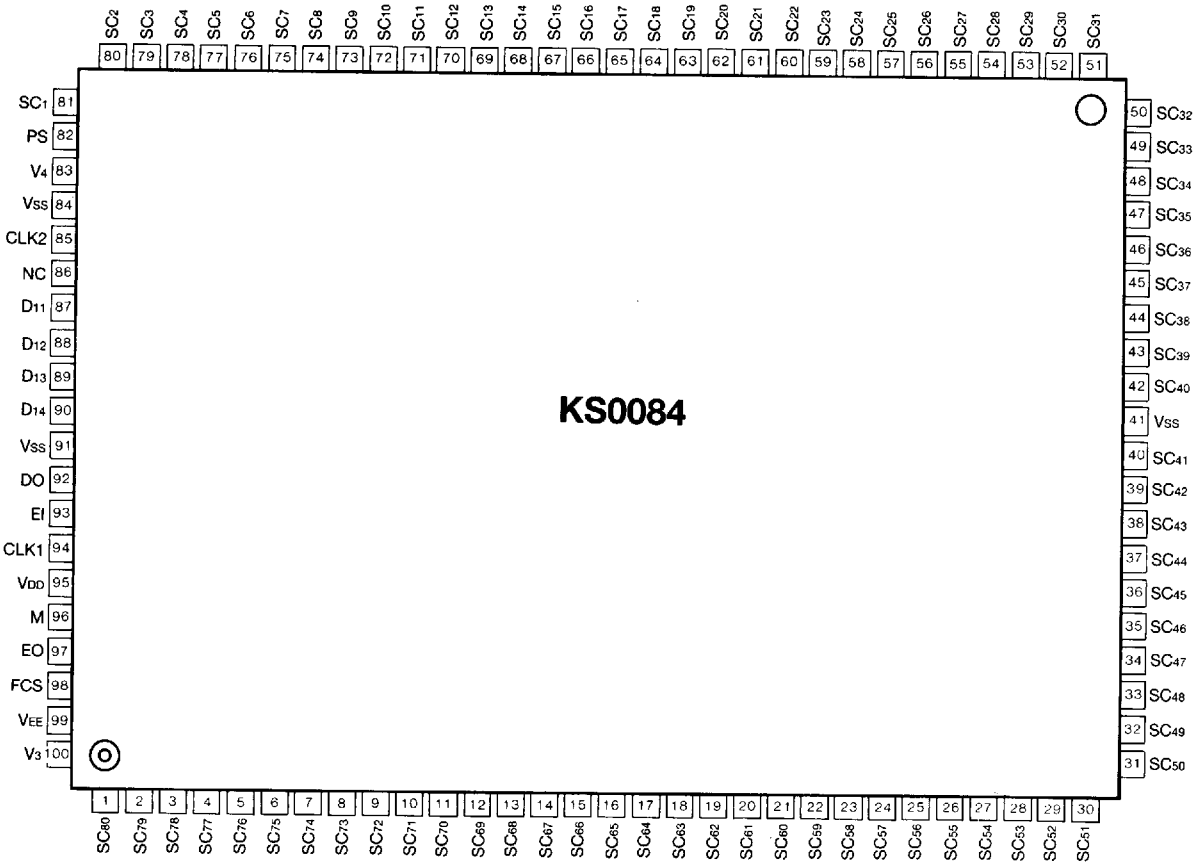
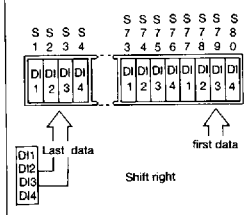
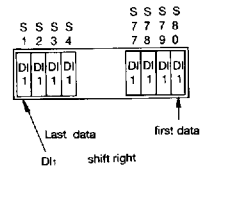



Fig.3 100QFP Top View.

## PIN FUNCTIONAL DESCRIPTION

<table>
<tr><th colspan="2">Pin (No.)</th><th>Input<br>Output</th><th>Description</th><th>Interface</th></tr>
<tr><td colspan="2">SC1~SC80<br>(100, 1-39, 41-80)</td><td>Output</td><td>LCD driver output terminals (80 Channel)</td><td>LCD</td></tr>
<tr><td rowspan="3">Power supply</td><td>VSS(40,90,97)</td><td rowspan="3"></td><td>GND (0V)</td><td rowspan="3">Power<br>Supply</td></tr>
<tr><td>VEE (82)</td><td>LCD driving Votage (-24V)</td></tr>
<tr><td>VDD(86)</td><td>Internal Logic driving Voltage</td></tr>
<tr><td colspan="2">V3, V4(81. 98)</td><td></td><td>Bias Voltage input for LCD drive: Non-select Level (Must maintain VSS>V3>V4>VEE.)</td><td>Power</td></tr>
<tr><td colspan="2">FCS, PS<br>(83, 89)</td><td>Input</td><td>Mode Select inputs. (refer to application circuit)
<table>
<tr><th>FCS</th><th>PS</th><th>Com/seg driver</th><th>Input mode</th><th>Chip select mode</th><th>DO Output</th></tr>
<tr><td>L</td><td>L</td><td>Segment driver</td><td>1 bit serial input</td><td>X</td><td>O</td></tr>
<tr><td>L</td><td>H</td><td>Segment driver</td><td>4 bit parallel input</td><td>O</td><td>H</td></tr>
<tr><td>H</td><td>L</td><td>Segment driver</td><td>1 bit serial input</td><td>X</td><td>H</td></tr>
<tr><td>H</td><td>H</td><td>Common driver</td><td>Serial input</td><td>O</td><td>O</td></tr>
</table>
- In case of serial input mode, DI1 is data input pin and D0 is data output pin
- In case of 4 bit parallel input mode, Data input and output are;
<table>
<tr><td>DI1</td><td>SC1, SC5, ...SC77</td><td>DI2</td><td>SC2, SC6, ...SC78</td></tr>
<tr><td>DI3</td><td>SC3, SC7, ...SC70</td><td>DI4</td><td>SC4, SC8, ...SC80</td></tr>
</table>
<table>
<tr><th>4 bit Data shift direction</th><th>1 bit Data shift</th></tr>
<tr><td> 
</td><td> 
</td></tr>
</table>
- In case of the common driver, the data transfer clock is CLK2
- Non-used data input pins are set to VSS or VDD to minimize current consumption</td><td></td></tr>
</table>

## PIN FUNCTIONAL DESCRIPTION (continued)

<table>
<tr><th>Pin (No.)</th><th>Input<br>Output</th><th>Description</th><th>Interface</th></tr>
<tr><td>EO, EI<br>(84, 88)</td><td>input<br>output</td><td>Input/Output for Chip Select.<br>1) EO becomes low by (CLK1, CLK2) timing.<br>2) When "HIGH" data is input to EI, the device becomes select mode and reads input data at CLK2 falling timing. Synchronized at the fall of CLK2. Input data is shifted.<br>3) After reading 80 input data(equivalent to 80 CLK2 clock cycle in the serial mode or 20 CLK2 clock cycles in the 4 bit paralle mode), EO automatically becomes HIGH level and data reading is complete. EO is reset 1.5 cycles later.<br>4) When two or more devices are used in the chip select mode, EO of each stage is connected to EI of the next stage.<br>(1) EO of all device connected is reset and device becomes non-select state and waits for EI input after the previous 1).<br>(2) When "HIGH" level is input to the first EI in the cascade connection, the first device performs the operations in 2) and 3).<br>(3) When EI of the second device is connected to DO of the first device, the second device perform the operations 2) and 3) after the first device. This operation is repeated in the same method subsequently</td><td>controller<br>or<br>KS0083/84</td></tr>
<tr><td>M(85)</td><td>input</td><td>LCD waveform AC conversion signal input<br>
<table>
<tr><th>Latch data</th><th>M</th><th>SC</th></tr>
<tr><td>L<br>(non-select)</td><td>L</td><td>V3</td></tr>
<tr><td></td><td>H</td><td>V4</td></tr>
<tr><td>H<br>(select)</td><td>L</td><td>GND</td></tr>
<tr><td></td><td>H</td><td>VEE</td></tr>
</table>
(segment signal drive mode)
<table>
<tr><th>Latch data</th><th>M</th><th>SC</th></tr>
<tr><td>L<br>(non-select)</td><td>L</td><td>V3</td></tr>
<tr><td></td><td>H</td><td>V4</td></tr>
<tr><td>H<br>(select)</td><td>L</td><td>VEE</td></tr>
<tr><td></td><td>H</td><td>GND</td></tr>
</table>
(common signal drive mode)</td><td>controller</td></tr>
<tr><td>CLK1(87)</td><td>input</td><td>Cock pulse input terminal for data latch</td><td>controller</td></tr>
<tr><td>CLK2(96)<br>DI1~DI4(91-94)</td><td>input<br>input</td><td>Clock pulse input terminal for data shift<br>Display data input from the LCD controller LSI.<br>In case of the common driver mode or serial input mode, supplu the input data to DI1 and DI2~DI$ have to be set to VSS level or VDD level.</td><td>controller<br>controller</td></tr>
<tr><td>DO(89)</td><td>output</td><td>DO is high level in the chip selet mode</td><td>KS0083/84</td></tr>
<tr><td>NC</td><td></td><td>No Connection</td><td>nc</td></tr>
</table>

## MAXIMUM ABSOLUTE LIMIT ($T_a$=25°C)

| Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|
| Supply voltage | Logic | $V_{DD}$ | −7 to +0.3 | V |
| | LCD drivers | $V_{LCD}$ | −30 to +0.3 | |
| Input voltage | | $V_{IN}$ | $V_{DD}$−0.3 to +0.3 | |
| Operating temperature | | $T_{opr}$ | −20 to +70 | °C |
| Storage temperature | | $T_{stg}$ | −55 to +150 | |

*Voltage greater than above may damage to the circuit.

**Maximum absolute limits are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device beyond them is not implied. Long exposure to these conditions may affect device reliability.**

## DC CHARACTERISTICS ($V_{DD}$= −5V ± 10%, $V_{SS}$=0V, $V_{EE}$= −24V ± 3V, $T_a$=25°C)

| Characteristic | | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Power supply current | | $I_{DD}$ | 1 bit serial (3.3MHz) | | | 5.0 | mA |
| | | | 4 bit parallel (2.0MHz) | | | 10.0 | mA |
| Input Voltage | High | $V_{IH}$ | — | 0.2$V_{DD}$ | | | V |
| | Low | $V_{IL}$ | — | | | 0.8$V_{DD}$ | V |
| Output Voltage | High | $V_{OH}$ | $I_{OH}$=−0.4mA | −0.4 | | | V |
| | Low | $V_{OL}$ | $I_{OL}$=0.4mA | | | $V_{DD}$+0.4 | V |
| Voltage descending (Vi-SCi) | | $V_{D1}$ | $I_{ON}$=1mA for one of SCi | | | 1.0 | V |
| | | $V_{D2}$ | $I_{ON}$=0.08mA for each SCi | | | 1.5 | V |
| Leakage Current | Input | $I_{LI}$ | — | | | 1.0 | μA |
| | Output | $I_{LO}$ | — | | | 10.0 | μA |

## AC CHARACTERISTICS

($V_{DD}$ = −5 V±10%, $V_{SS}$=0V, $V_{EE}$ = −24V±3V; $T_a$ = +25°C)

(1) Segment driver1; 1 bit serial data input (PS=LOW, FCS=LOW) (refer to: fig. 3)

| Characteristic | | Symbol | Test condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Clock cycle time | | $t_C$ | | 300 | | ns |
| Clock pulse width | High level | $t_{WH}$ | | 130 | | |
| | Low level | $t_{WL}$ | | 130 | | |
| Set up time D before CLK2↓ | | $t_{SU}$ | | 70 | | |
| Hold time D after CLK2↓ | | $t_h$ | | 50 | | |
| Clock margin time 1 (from CLK1↓ to CLK2↓) | | $t_{C1}$ | | 20 | | |
| Clock margin time 2 **NOTE 1** (from CLK2↓ to CLK1↓) | | $t_{C2}$ | | 200 | | |
| Clock margin time 3 (from CLK2↑ to CLK1↑) | | $t_{C3}$ | | 20 | | |
| Clock rise/fall time | | $t_r$,$t_f$ | | | 50 | |
| Output Delay | | $t_D$ | $C_L$=15pF | | 230 | |
| High level latch clock width | | $t_{CWH}$ | | 130 | **NOTE 2** | |
| Overlap time of CLK2 "L" and CLK1 "H" | | $t_{OV}$ | | 130 | | |

(2) segment driver; 4 bit data input (PS=High, FCS=LOW) (refer to: fig 4.)

| Characteristic | | Symbol | Test condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Clock cycle time | | $t_C$ | | 500 | | ns |
| Clock pulse width | High level | $t_{WH}$ | | 230 | | |
| | Low level | $t_{WL}$ | | 230 | | |
| Set-up time D before CLK2↓ | | $t_{SU}$ | | 70 | | |
| Hold time D after CLK2↓ | | $t_h$ | | 50 | | |
| Clock margin time 1 (from CLK1↓ to CLK2↓) | | $t_{C1}$ | | 20 | | |
| Clock margin time 2 **NOTE 1** (from CLK2↓ to CLK1↓) | | $t_{C2}$ | | 200 | | |
| Clock margin time 3 (from CLK2↑ to CLK1↑) | | $t_{C3}$ | | 20 | | |
| Clock rise/fall time | | $t_r$, $t_f$ | | | 50 | |
| Output Delay | | $t_D$ | $C_L$=15pF | | 230 | |
| High level latch clock width | | $t_{LWH}$ | | 130 | **NOTE 2** | |
| Overlap time of CLK2 "L" and CLK1 "H" | | $t_{OV}$ | | 130 | | |

(3) Common Driver (PS=HIGH, FCS=HIGH) (refer to: fig 5)

| Characteristic | | Symbol | Test condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Clock cycle time | | $t_C$ | | 1000 | | ns |
| Clock pulse width | High level | $t_{WH}$ | | 130 | | |
| | Low level | $t_{WL}$ | | 830 | | |
| Set-up time D before CLK↓ | | $t_{SU}$ | | 70 | | |
| Hold time D after CLK↓ | | $t_h$ | | 50 | | |
| Output Delay | | $t_D$ | CL=15pF | | 500 | |
| Clock rise/fall time | | $t_r, t_f$ | | | 50 | |

(4) segment driver 2; 1 bit serial data input (PS=LOW, FCS=HIGH) (refer to: fig 6)

| Characteristic | | Symbol | Test condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Clock cycle time | | $t_C$ | | 380 | | ns |
| Clock pulse width | High level | $t_{WH}$ | | 170 | | |
| | Low level | $t_{WL}$ | | | | |
| Set-up time D before CLK↑ | | $t_{SU}$ | | 70 | | |
| Hold time D after CLK↑ | | $t_h$ | | 50 | | |
| Clock margin time 1 (from CLK1↓ to CLK2↓) | | $t_{C1}$ | | 20 | | |
| Clock margin time 2 NOTE 1 (from CLK2↓ to CLK1↓) | | $t_{C2}$ | | 200 | | |
| Clock margin time 3 (from CLK2↑ to CLK1↑) | | $t_{C3}$ | | 20 | | |
| Clock rise/fall time | | $t_r, t_f$ | | | 50 | |
| Output delay | | $t_D$ | CL=15pF | | 230 | |
| High level latch clock with | | $t_{LWH}$ | | 130 | NOTE 2 | |
| Overlap time of CLK2 "L" and CLK1 "H" | | $t_{OV}$ | | 130 | | |

note (Input frequency, I/O reference level; 0.8 $V_{DD}$, 0.2 $V_{DD}$)

1; Valid time (internal shift register)

2; $(t_C \times 1.5) - (t_{C1}) - (t_{C3}) - (t_r \times 3)$

## TIMING DIAGRAM

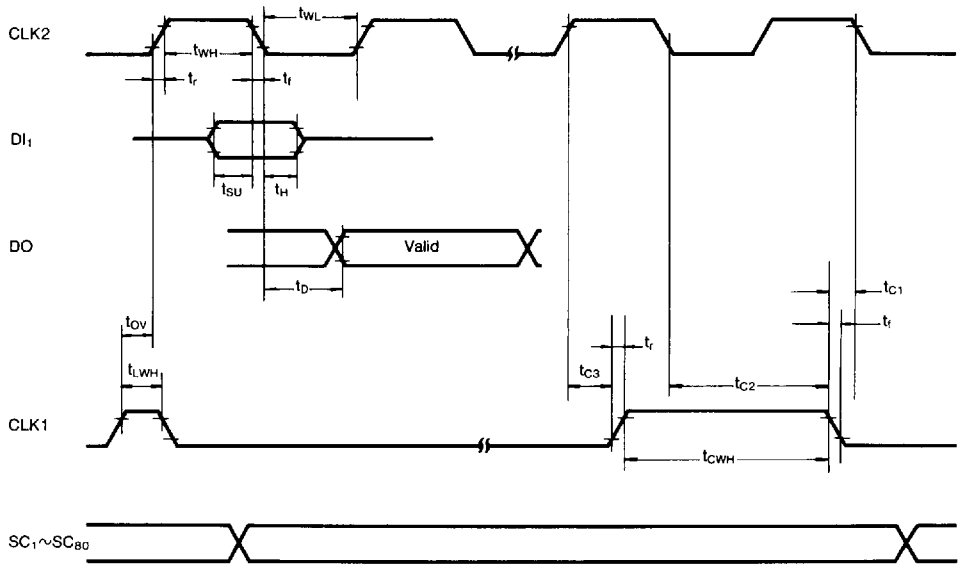



Fig. 3 Segment driver (1 bit serial input)

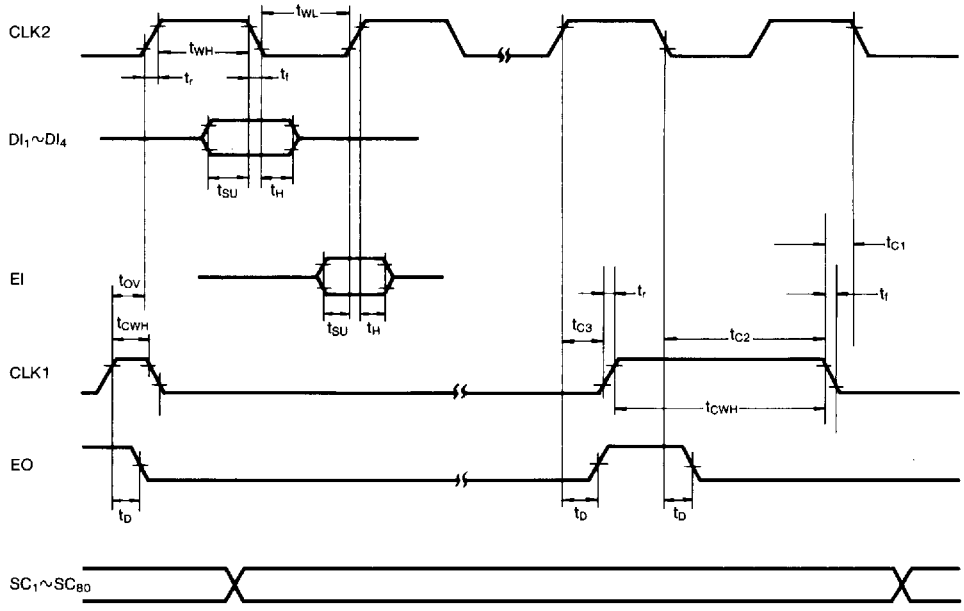



Fig. 4. 4-bit input segment driver

## TIMING DIAGRAMS (Continued)

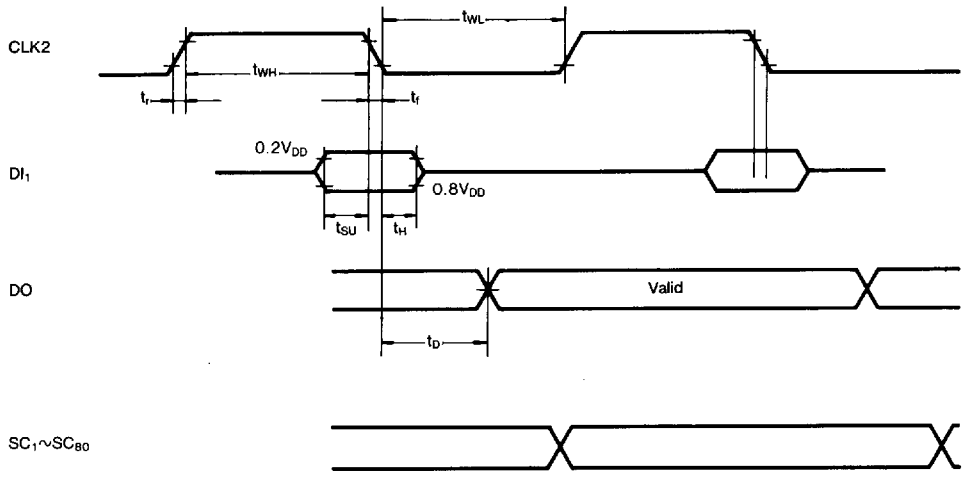



Fig. 5. Common driver

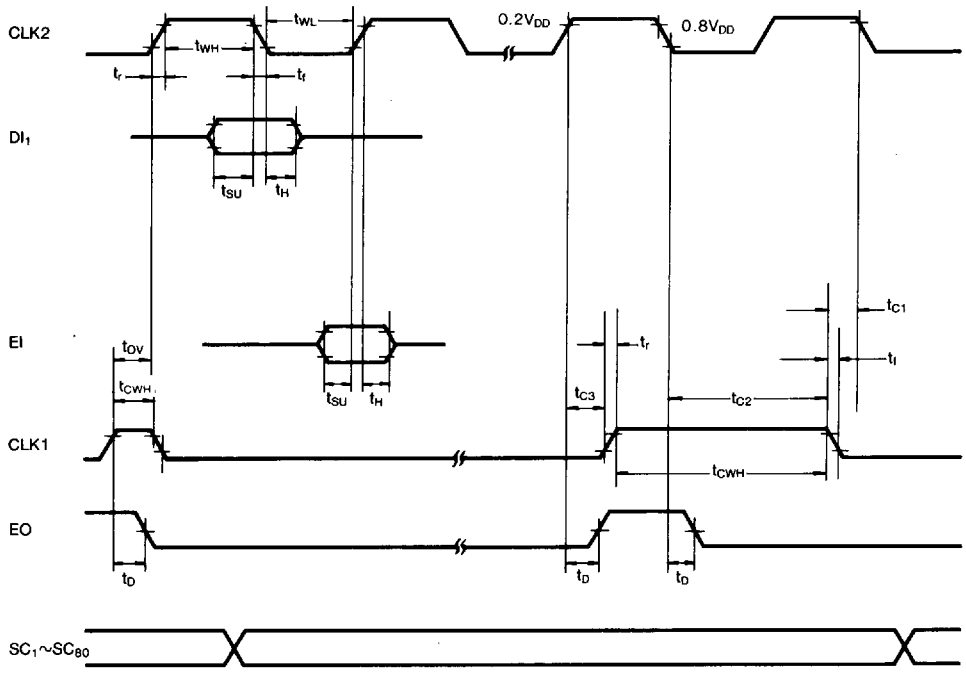
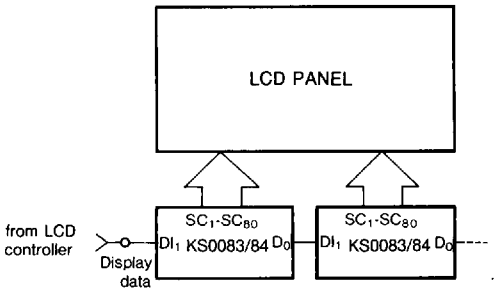



Fig. 6. Segment driver (1 bit serial data input)

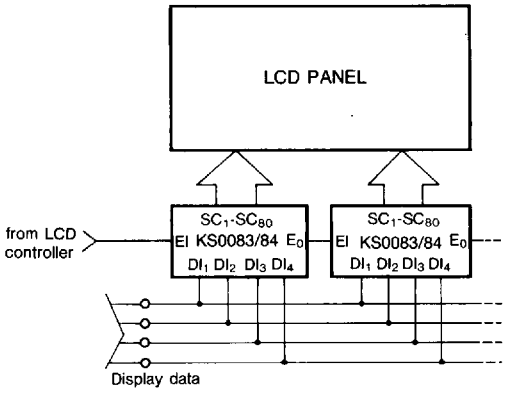
## APPLICATION CIRCUIT .

### Mode Select

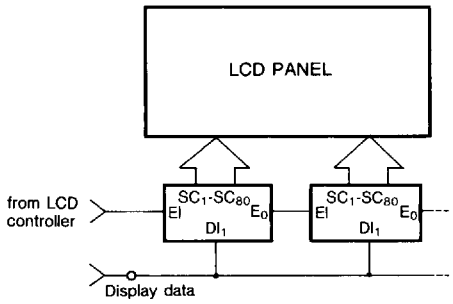
1. segment driver 1; 1 bit serial data input (FCS=L, PS=L)



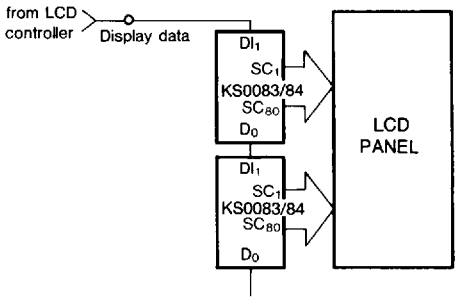

2. segment driver; 4 bit data input (FCS=L, PS=H)



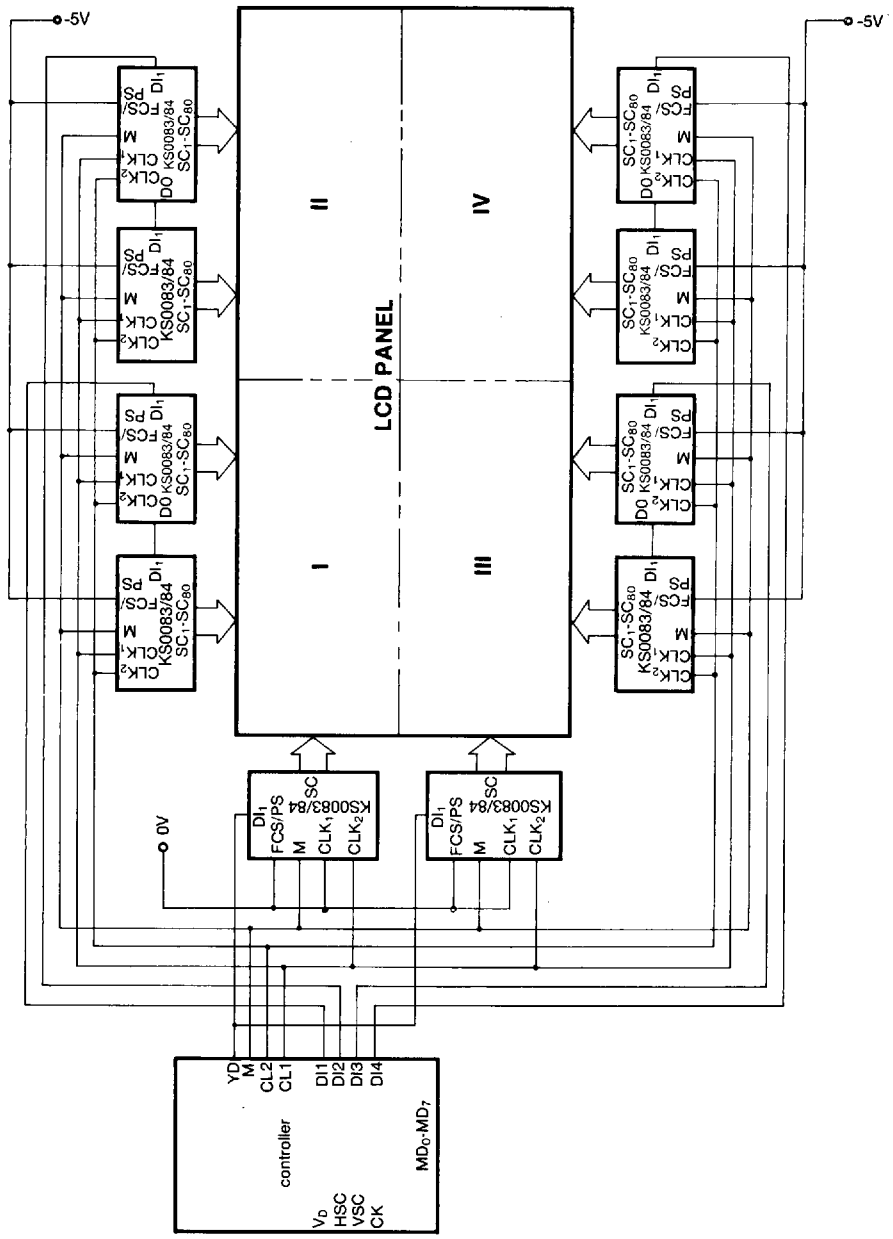

3. segment driver 2; 1 bit serial data input (FCS=H, PS=L)




4. common driver (FCS=H, PS=H)



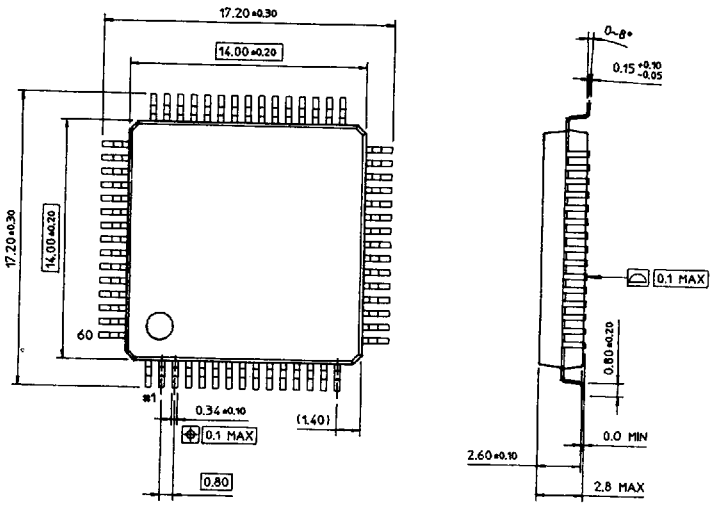
## APPLICATION CIRCUIT



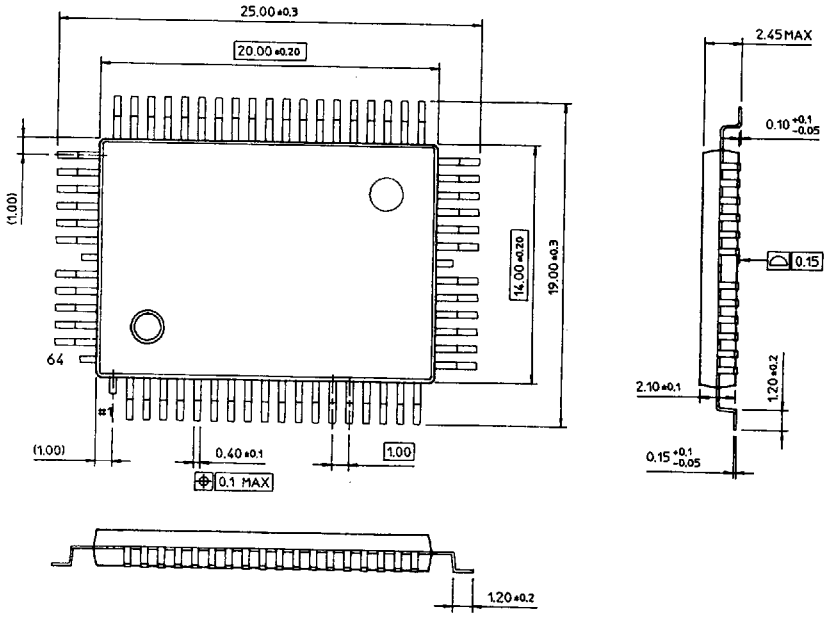
# PACKAGE DIMENSIONS

Dimensions in Milimeters

**60-QFP-1414A**



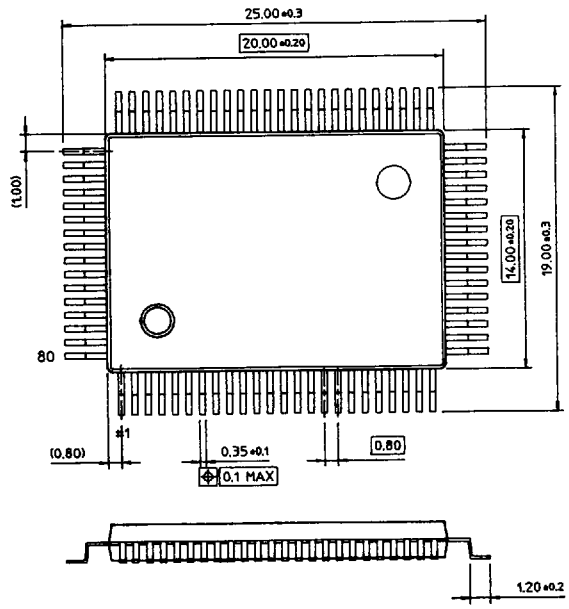

**64-QFP-1420D**



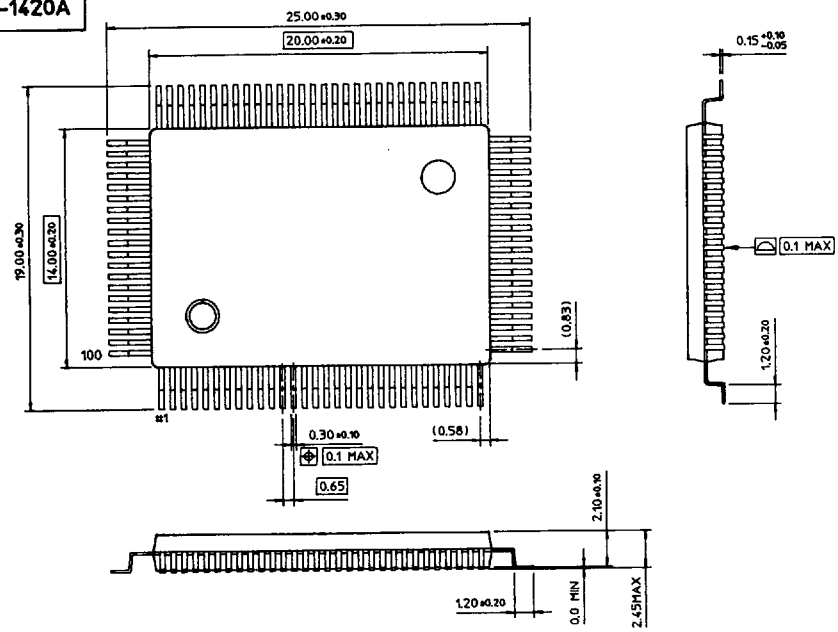
# PACKAGE DIMENSIONS

Dimensions in Milimeters

## 80-QFP-1420A



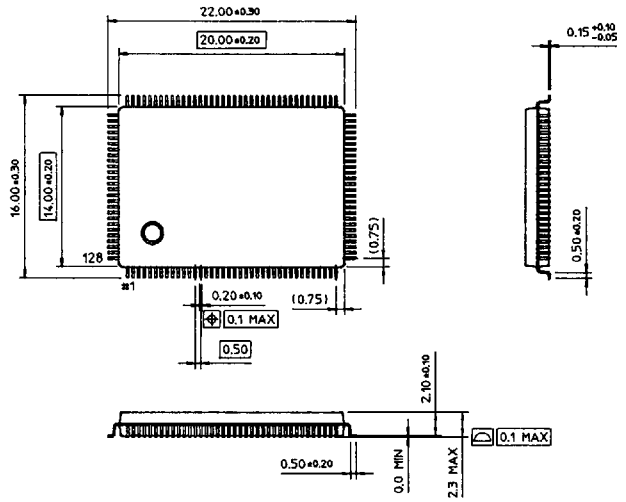

## 100-QFP-1420A



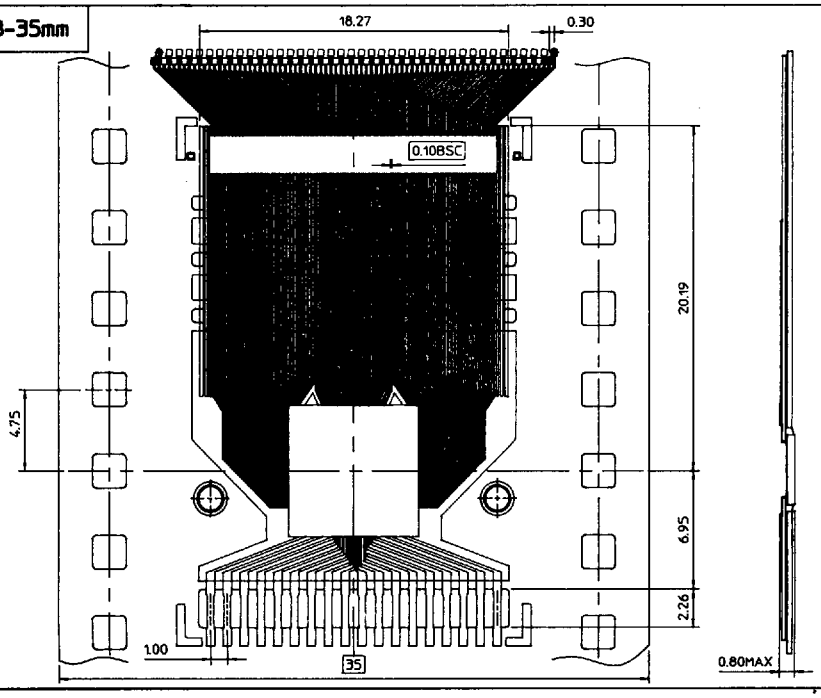
# PACKAGE DIMENSIONS

Dimensions in Milimeters

**128-QFP-1420**



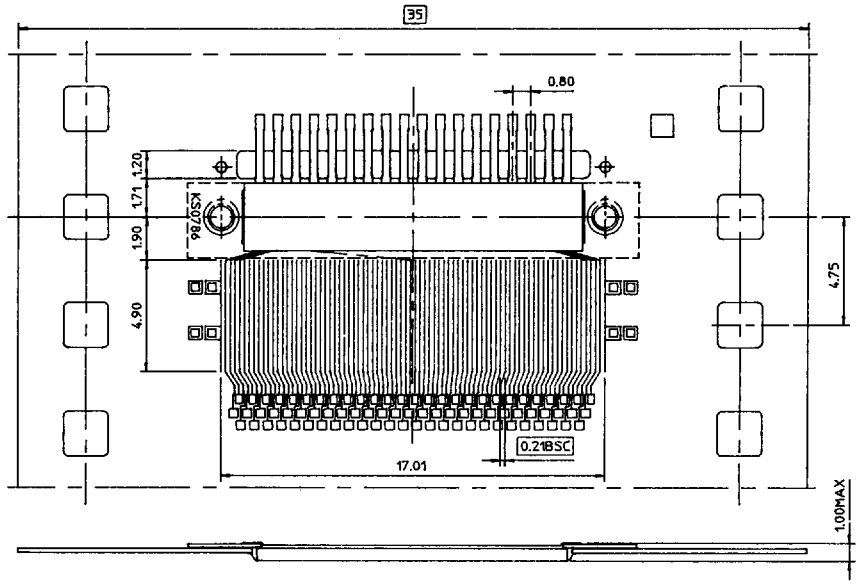

**98-TAB-35mm**



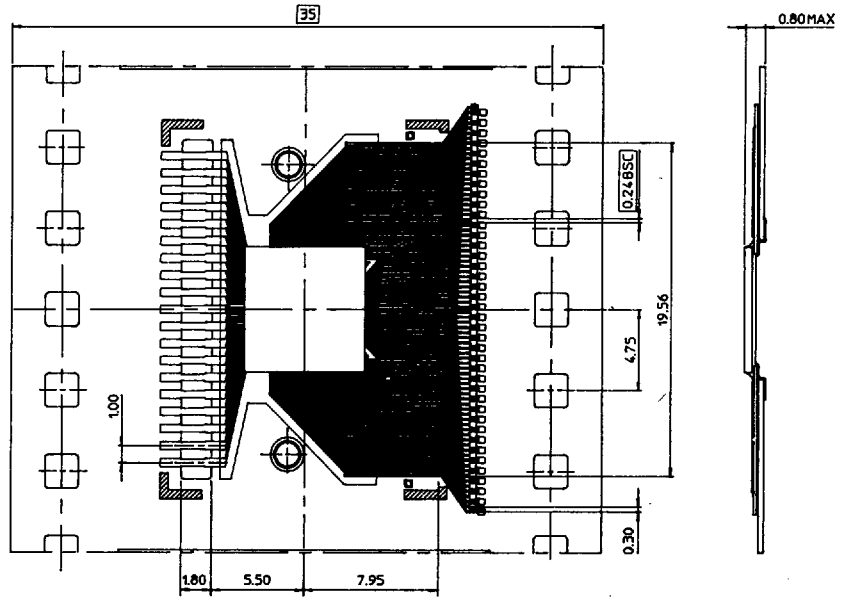
# PACKAGE DIMENSIONS

Dimensions in Milimeters

**98-STAB-35mm**




**99-TAB-35mm**



# PACKAGE DIMENSIONS

Dimensions in Milimeters

120-STAB-35mm