target spec

262,144WORDS X 8BITS MULTIPORT DRAM

DESCRIPTION

The TC528257 is a 2M bit CMOS multiport memory equipped with a 262,144-words by 8-bits dynamic random access memory (RAM) port and a 512-words by 8-bits static serial access memory (SAM) port. The TC528257 supports three types of operations; Random access to and from the RAM port, high speed serial access to and from the SAM port and bidirectional transfer of data between any selected row in the RAM and the SAM. To realize a high performance graphic frame buffer system the TC528257 features various special operations such as the write - per - bit, the pipelined page mode, the block write and flash write function on the RAM port and the read and masked write transfer operations between the RAM and the SAM port. The TC528257 is fabricated using Toshiba's CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

FEATURES

- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- All inputs and outputs : TTL Compatible
- Organization
  RAM Port : 262,144wordsX8bits
  SAM Port : 512wordsX8bits
- RAM Port
  Fast Page Mode, Read - Modify - Write, Pipelined Fast Page Mode, $\overline{CAS}$ before $\overline{RAS}$ Auto Refresh, Hidden Refresh, $\overline{RAS}$ only Refresh, Write per Bit (New/Old Mask Mode), Masked Flash Write (New/Old Mask Mode), Block Write, Masked Block Write (New/Old Mask Mode), Load Mask Register/Color Register Cycle, 512 refresh cycles / 8ms
- SAM Port
  Serial Read / Write Capability
  Addressable TAP Capability
  Stop Address (Binary Boundary) Capability
  Fully Static Register, Single Register/Split Register Mode Capability
- RAM - SAM Bidirectional Transfer
  Read / Real Time Read Transfer
  Masked Write Transfer
  Split Read / Masked Split Write Transfer
- Package
  TC528257J : SOJ40-P-400
  TC528257FT : TSOP44-P-400B
  TC528257TR : TSOP44-P-400C

KEY PARAMETERS

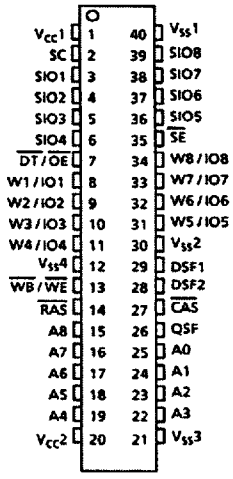
ITEM		TC528257	
		— 70	— 80
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	70ns	80ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	20ns	20ns
t_{AA}	Column Address Access Time (Max.)	35ns	40ns
t_{RC}	Cycle Time (Min.)	130ns	150ns
t_{PC}	Page Mode Cycle Time (Min.)	45ns	50ns
t_{SCA}	Serial Access Time (Max.)	20ns	25ns
t_{SCC}	Serial Cycle Time (Min.)	25ns	30ns
t_{RACP}	t_{RAC} in Pipelined Fast Page	90ns	95ns
t_{CAC1}	t_{CAC} in Pipelined Fast Page	20ns	20ns
t_{PCP}	Pipelined Fast Page Mode Cycle Time	30ns	30ns
I_{CC1}	RAM Operating Current (SAM : Standby)	100mA	85mA
I_{CC2A}	SAM Operating Current (RAM : Standby)	60mA	50mA
I_{CC2}	Standby Current	10mA	10mA

PIN NAME

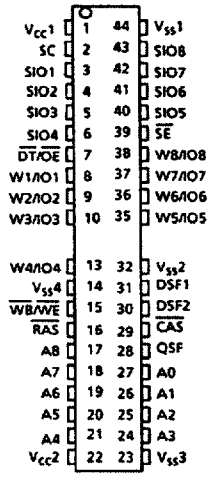
A0~A8	Address inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}/\overline{WE}$	Write per Bit/Write Enable
DSF1 DSF2	Special Function Control
WI/IOI ~W8/IO8	Write Mask/Data IN/OUT
SC	Serial Clock
SE	Serial Enable
SIOI~SIO8	Serial Input/Output
QSF	Special Flag Output
V_{CC}/V_{SS}	Power(5V)/Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

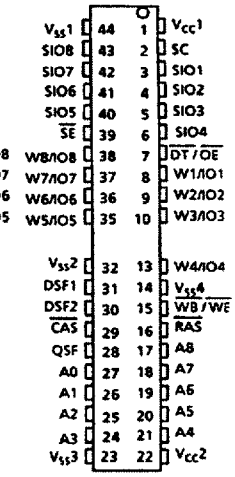
TC528257J



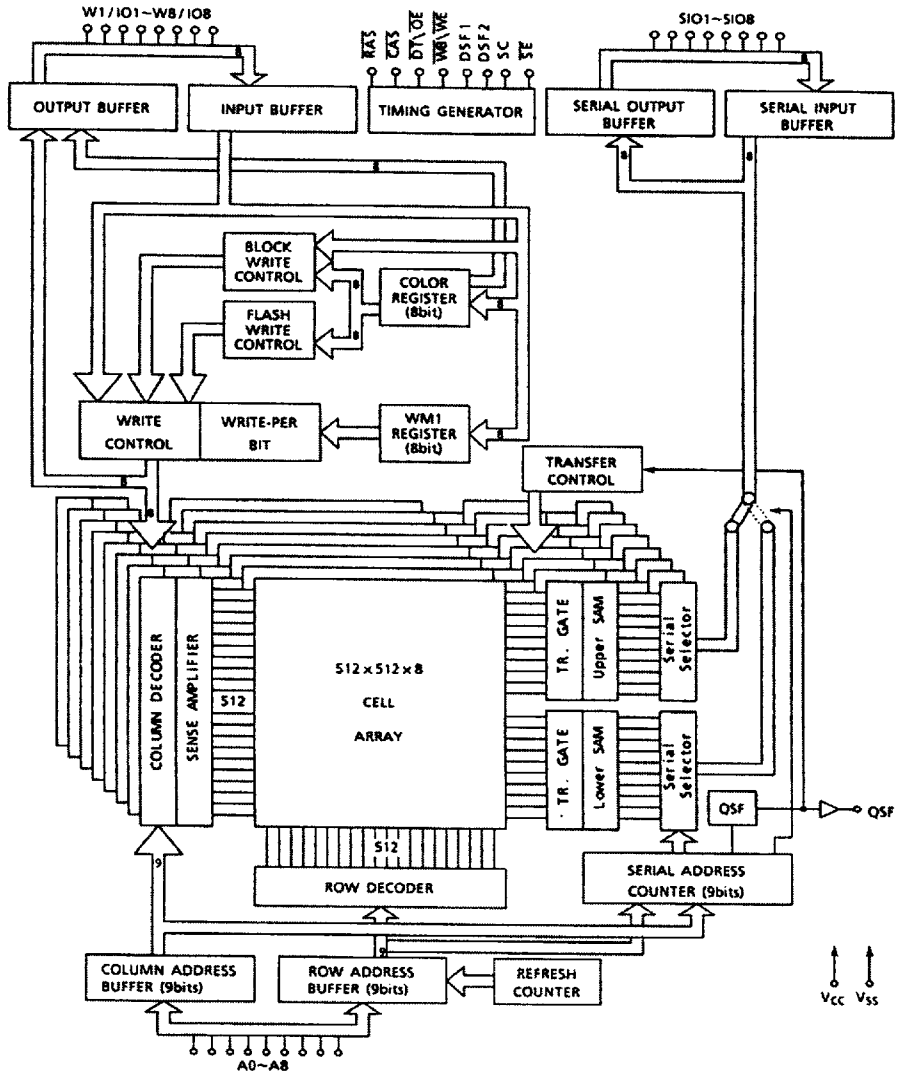
TC528257FT



TC528257TR



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}, V_{OUT}	Input Output Voltage	— 1.0~7.0	V	1
V_{CC}	Power Supply Voltage	— 1.0~7.0	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	— 55~150	°C	1
T_{SOLDER}	Soldering Temperature • Time	260•10	°C•sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	6.5	V	2
V_{IL}	Input Low Voltage	— 1.0	—	0.8	V	2

CAPACITANCE (V_{CC} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance	—	7	pF
C_{IO}	Input/Output Capacitance	—	9	
C_O	Output Capacitance (QSF)	—	9	

Note: This parameter is periodically sampled and is not 100% tested.

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

ITEM (RAM PORT)	SAM PORT	SYMBOL	-70		-80		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
OPERATING CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC1}	—	100	—	90	mA	3, 4, 5
	Active	I_{CC1A}	—	160	—	140		3, 4, 5
STANDBY CURRENT ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	Standby	I_{CC2}	—	10	—	10		
	Active	I_{CC2A}	—	65	—	55		3, 4, 5
RAS ONLY REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	Standby	I_{CC3}	—	100	—	90		3, 4, 5
	Active	I_{CC3A}	—	160	—	140		3, 4, 5
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = t_{RC} min.)	Standby	I_{CC4}	—	90	—	80		3, 4, 5
	Active	I_{CC4A}	—	150	—	130		3, 4, 5
CAS BEFORE RAS REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$, t_{RC} = t_{RC} min.)	Standby	I_{CC5}	—	100	—	90		3, 4, 5
	Active	I_{CC5A}	—	160	—	140		3, 4, 5
DATA TRANSFER CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC6}	—	135	—	125		3, 4, 5
	Active	I_{CC6A}	—	195	—	175		3, 4, 5
FLASH WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC7}	—	100	—	90		3, 4, 5
	Active	I_{CC7A}	—	160	—	140		3, 4, 5
BLOCK WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC8}	—	110	—	100		3, 4, 5
	Active	I_{CC8A}	—	170	—	150		3, 4, 5

ITEM	SYMBOL	MIN.	MAX	UNIT	NOTE
INPUT LEAKAGE CURRENT 0V ≤ V_{IN} ≤ 6.5V, All other pins not under test = 0V	$I_{I(L)}$	—10	10	μA	
OUTPUT LEAKAGE CURRENT 0V ≤ V_{OUT} ≤ 5.5V, Output Disable	$I_{O(L)}$	—10	10	μA	
OUTPUT "H" LEVEL VOLTAGE I_{OUT} = - 2mA	V_{OH}	2.4	—	V	
OUTPUT "L" LEVEL VOLTAGE I_{OUT} = 2mA	V_{OL}	—	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes: 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX		
t_{RC}	Random Read or Write Cycle Time	130		150		ns	
t_{RMW}	Read-Modify-Write Cycle Time	180		200			
t_{PC}	Fast Page Mode Cycle Time	45		50			
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	90		90			
t_{RAC}	Access Time from $\overline{RAS}$		70		80		9, 15
t_{AA}	Access Time from Column Address		35		40		9, 15
t_{CAC}	Access Time from $\overline{CAS}$		20		20		9, 16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		35		40		9, 16
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0		0			
t_{OELZ}	$\overline{OE}$ to Output in Low-Z	0		0			
t_{OFF}	Output Buffer Turn-Off Delay	0	15	0	15		11
t_T	Transition Time (Rise and Fall)	3	50	3	50		8
t_{RP}	$\overline{RAS}$ Precharge Time	50		60			
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10000	80	10000		
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	70	100000	80	100000		
t_{RSH}	$\overline{RAS}$ Hold Time	20		20			
t_{CSH}	$\overline{CAS}$ Hold Time	70		80			
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10000	20	10000		
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60		15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40		15
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35		40			
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5			
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10			
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		10			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	12		15			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0			12
t_{WCH}	Write Command Hold Time	10		15			
t_{WP}	Write Command Pulse Width	10		10			
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20			
t_{DS}	Data Set-Up Time	0		0			13
t_{DH}	Data Hold Time	12		15			13
t_{WCS}	Write Command Set-Up Time	0		0			14
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	95		105			14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60		65			14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45		45			14
t_{RES}	$\overline{RAS}$ to SC Boundary - reset time	30		30			

SYMBOL	PARAMETER	-70		-80		UNIT	NOTE
		MIN.	MAX	MIN.	MAX.		
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0		ns	
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{OE}$		20		20		9
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$		15		15		11
t_{OED}	$\overline{OE}$ to Data Delay Time	15		15			
t_{OEH}	$\overline{OE}$ Command Hold Time	15		15			
t_{ODS}	Output Disable Set up time	0		0			
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15		15			
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	5		5			
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		15			
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{WB}$ Set-Up Time	0		0		ns	
t_{RWH}	$\overline{WB}$ Hold Time	10		15			
t_{FSR}	DSF Set-Up Time referenced to $\overline{RAS}$	0		0			
t_{RFH}	DSF Hold Time referenced to $\overline{RAS}$ (1)	10		15			
t_{FSC}	DSF Set-Up Time referenced to $\overline{CAS}$	0		0			
t_{CFH}	DSF Hold Time referenced to $\overline{CAS}$	12		15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	10		15			
t_{THS}	$\overline{DT}$ High Set-Up Time	0		0			
t_{THH}	$\overline{DT}$ High Hold Time	10		15			
t_{TLS}	$\overline{DT}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{DT}$ Low Hold Time	10	10000	15	10000		
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	60	10000	65	10000		
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	25		25			
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	20		20			
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	50		60			
t_{TP}	$\overline{DT}$ Precharge Time	15		15			
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	70		80			
t_{ASD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	35		40			
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	20		20			
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5			
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	10		15			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	25		30			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	20		25			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	45		50			

SYMBOL	PARAMETER	-70		-80		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{SCC}	SC Cycle Time	25		30		ns	
t_{SC}	SC Pulse Width (SC High Time)	10		10			
t_{SCP}	SC Precharge Time (SC Low Time)	5		10			
t_{SCA}	Access Time from SC		20		25		10
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	10		15			
t_{SEA}	Access Time from $\overline{SE}$		20		25		10
t_{SE}	$\overline{SE}$ Pulse Width	20		25			
t_{SEP}	$\overline{SE}$ Precharge Time	20		25			
t_{SEZ}	Serial Output Buffer Turn-off Delay from $\overline{SE}$		15		20		11
t_{SZE}	Serial Output Buffer Turn-off Delay from $\overline{SE}$	0		0			
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	0		0			
t_{SWH}	Serial Write Enable Hold Time	10		15			
t_{SWIS}	Serial Write Disable Set-Up Time	0		0			
t_{SWIH}	Serial Write Disable Hold Time	10		10			
t_{STS}	Split Transfer Set-Up Time	25		30			
t_{STH}	Split Transfer Hold Time	25		30			
tSAAT	Split Transfer SC Set-Up Time from RAS	45		55			
tSAA	Split Transfer SC Hold Time from RAS	0		0			
t_{SQD}	SC-QSF Delay Time		20		25		
t_{TQD}	$\overline{DT}$-QSF Delay Time		20		25		
t_{CQD}	$\overline{CAS}$-QSF Delay Time		20		25		
t_{RQD}	$\overline{RAS}$-QSF Delay Time		70		80		
t_{RCDP}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time (Pipeline mode)	20	40	20	45		
t_{CSHP}	$\overline{CAS}$ Hold Time (Pipeline mode)	50		55			
t_{RACP}	Access TIme from $\overline{RAS}$ (Pipeline mode)		90		95		
t_{CAC1}	Access Time from $\overline{CAS}$ (1) (Pipeline mode)		20		20		10
t_{CAC2}	Access Time from $\overline{CAS}$ (2) (Pipeline mode)		50		50		10
t_{CASP}	$\overline{CAS}$ Pulse Width (Pipeline mode)	10		10			
t_{CPP}	$\overline{CAS}$ Precharge Time Pipeline mode)	10		10			
t_{PCP}	Fast Page Mode Cycle Time (Pipeline mode)	30		30			
t_{COH}	$\overline{CAS}$ Hold Time referenced to $\overline{OE}$ (Pipeline mode)	5		5			
t_{RSH1}	$\overline{RAS}$ Hold Time (1) (Pipeline mode)	20		20			
t_{RSH2}	$\overline{RAS}$ Hold Time (2) (Pipeline mode)	50		50			
t_{CWLP}	Write Command to $\overline{CAS}$ lead Time (Pipeline mode)	10		10			
t_{CWP}	$\overline{WE}$ to $\overline{CAS}$ Delay Time (Pipeline mode)	30		30			
t_{OFFP}	Outoff Buffer Turn-off Delay from $\overline{RAS}$ (Pipeline mode)	0	15	0	15		11, 17

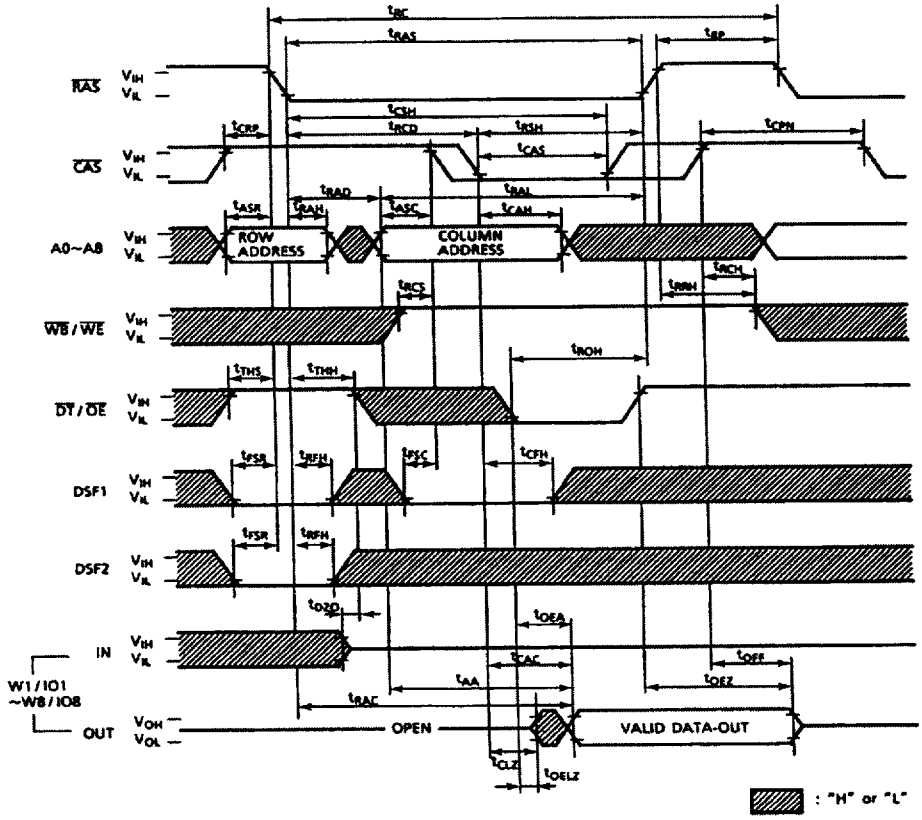
RAM Output Reference Level	2.0V/0.8V
SAM Output Reference Level	2.0V/0.8V
RAM Output Load	1 TTL and 50PF
SAM Output Load	1 TTL and 30PF

NOTES:

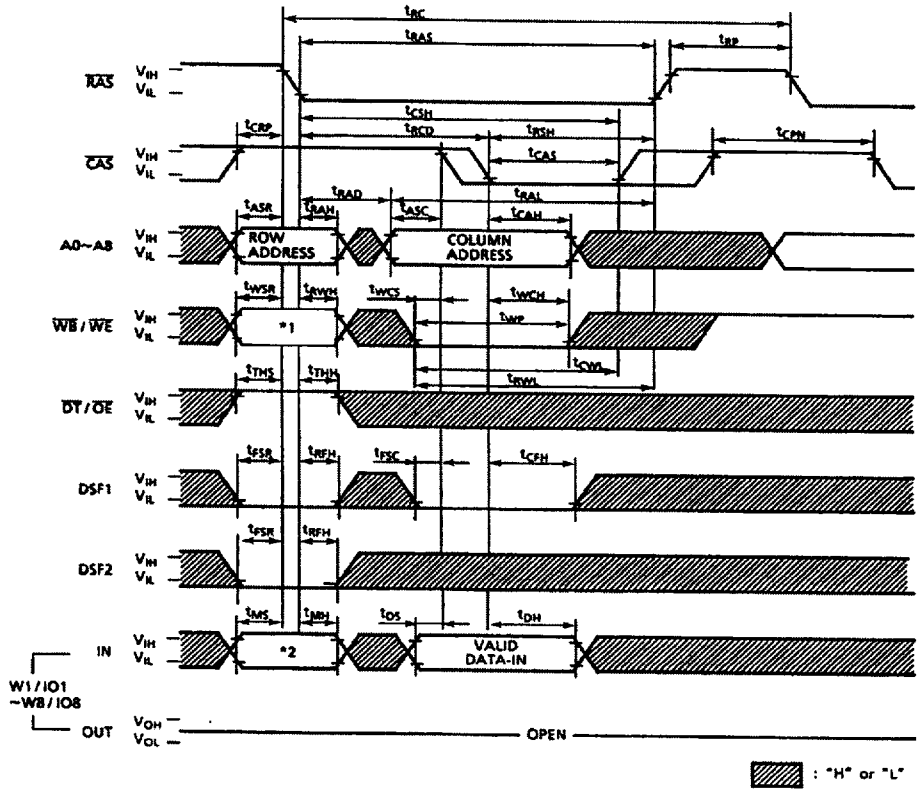
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. These parameters depend on cycle rate.
4. These parameters depend on output loading. Specified values are obtained with the output open.
5. Address can be changed once or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).
6. An initial pause of 200μs is required after power-up followed by any of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles before proper device operation is achieved.
7. AC measurements assume $t_T = 5ns$.
8. $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. RAM port outputs are measured with a load equivalent to 1 TTL load and 50pF.
   D_{OUT} reference levels : V_{OH} / V_{OL} = 2.0V / 0.8V.
10. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
    D_{OUT} reference levels : V_{OH} / V_{OL} = 2.0V / 0.8V.
11. $t_{OFF\ (max.)}$, $t_{OEZ\ (max.)}$, $t_{OFFP\ (max.)}$ and $t_{SEZ\ (max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}$ / $\overline{WE}$ leading edge in $\overline{OE}$-controlled-write cycles and read-modify-write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS\ (min.)}$, the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geq t_{RWD\ (min.)}$, $t_{CWD} \geq t_{CWD\ (min.)}$ and $t_{AWD} \geq t_{AWD\ (min.)}$ the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the $t_{RCD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can he met.
    $t_{RCD\ (max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
16. Operation within the $t_{RAD\ (max.)}$ limit insures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.
17. t_{OFFP} timing is specified from either $\overline{RAS}$ or $\overline{CAS}$ rising edge, whichever occurs last.

TIMING WAVEFORM

READ CYCLE



WRITE CYCLE (EARLY WRITE)

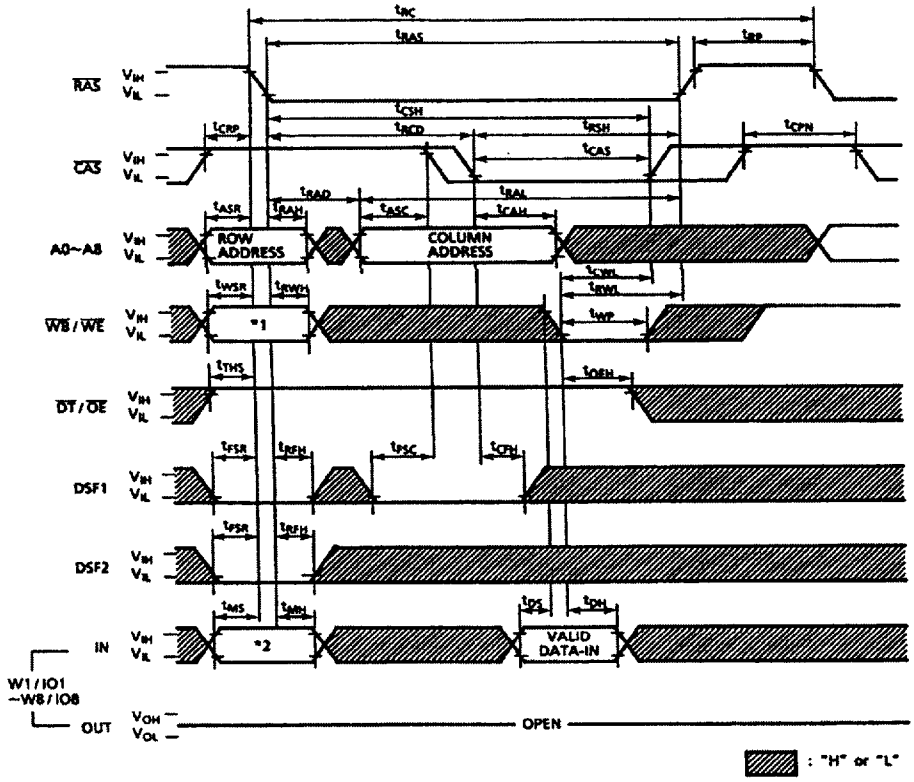


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

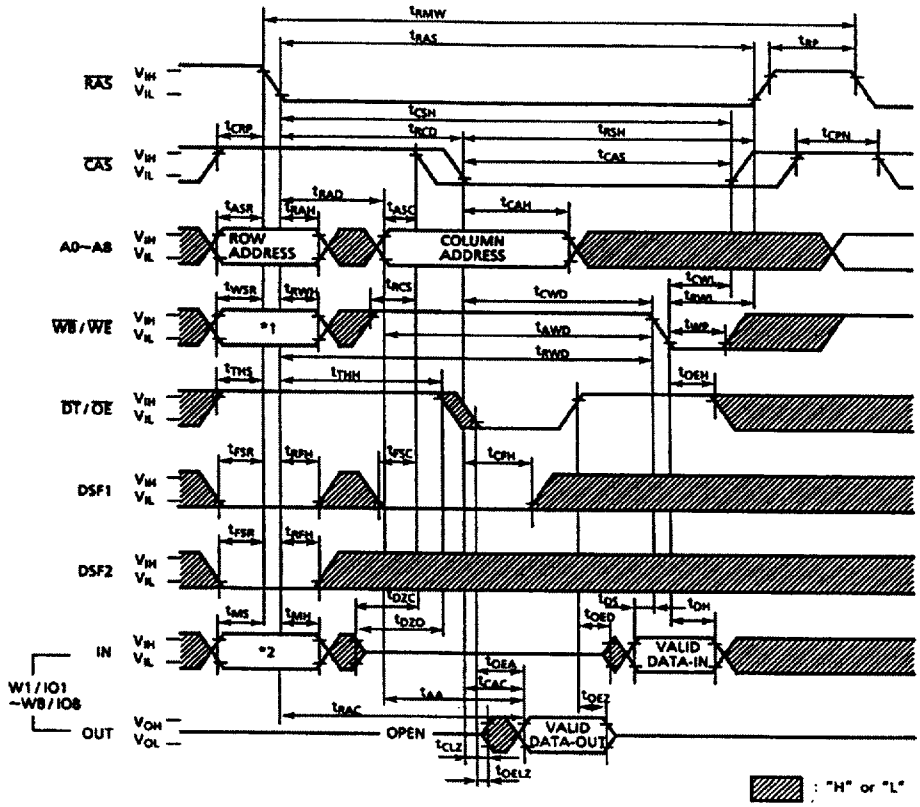


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

READ-MODIFY-WRITE CYCLE

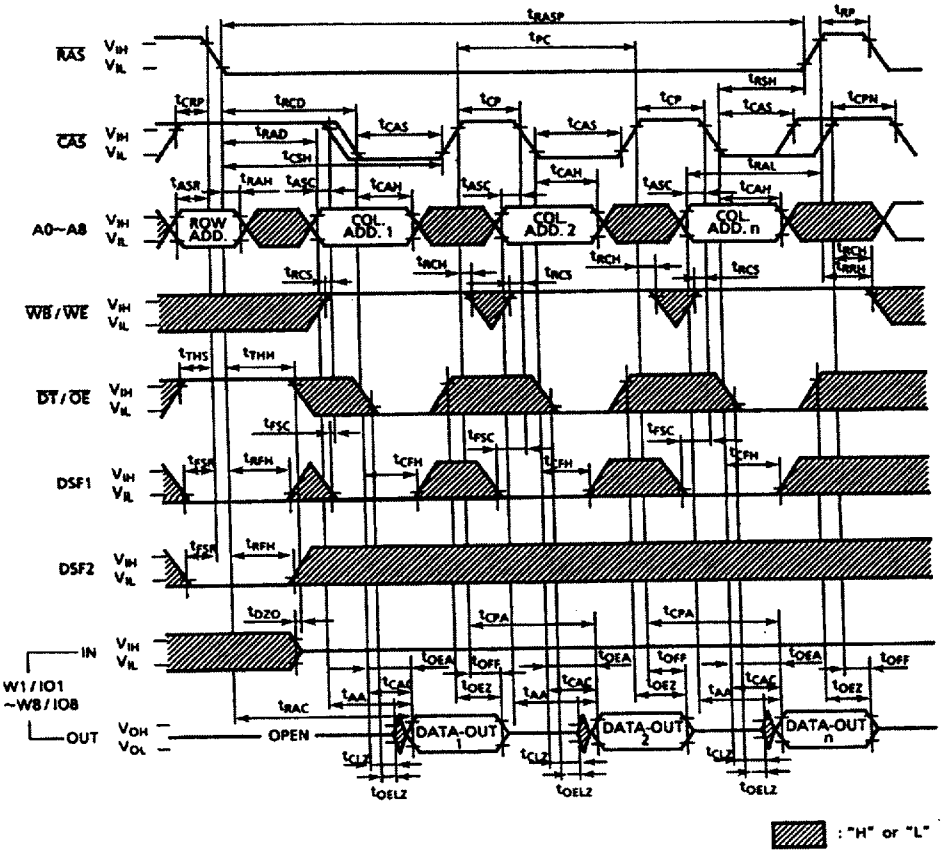


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

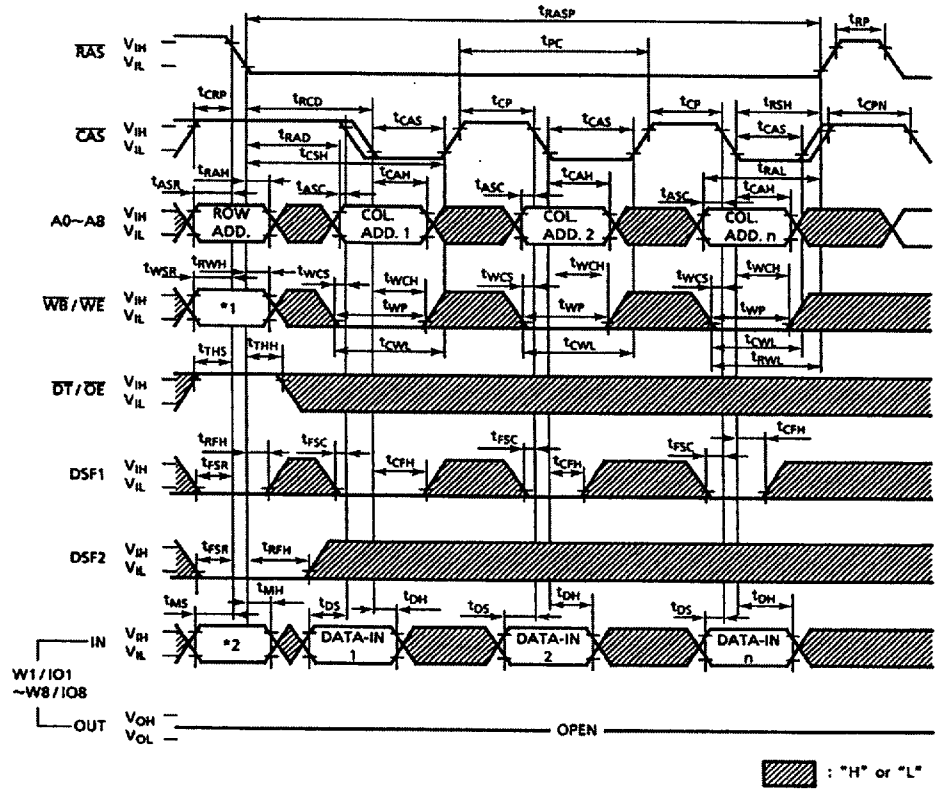
WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

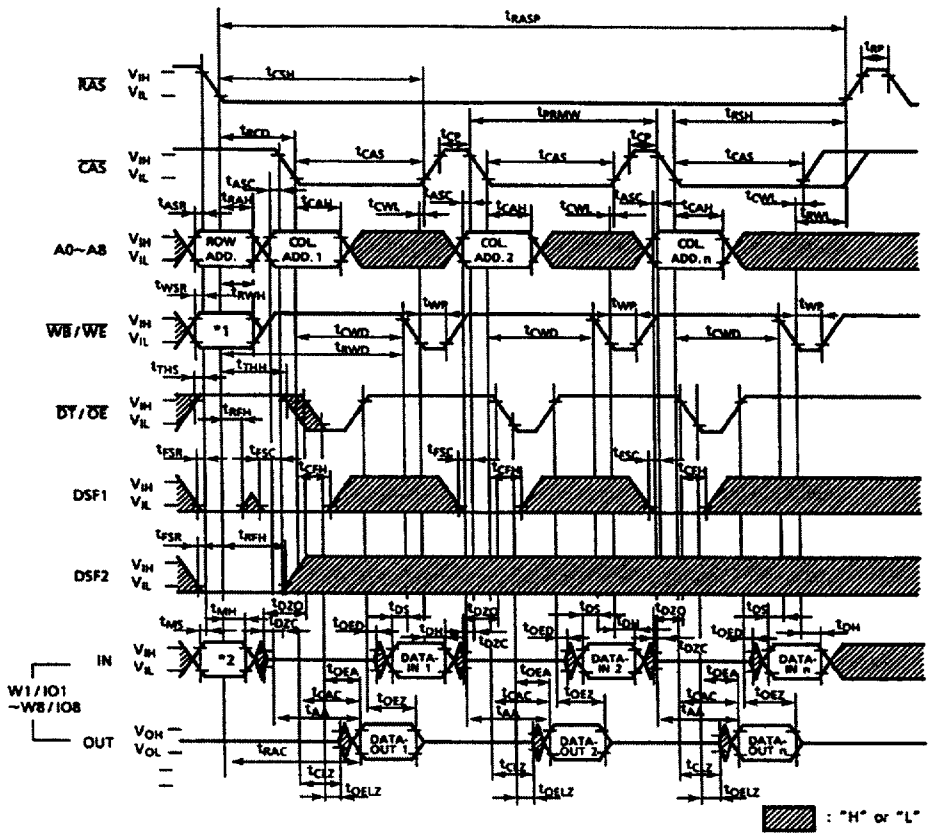


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

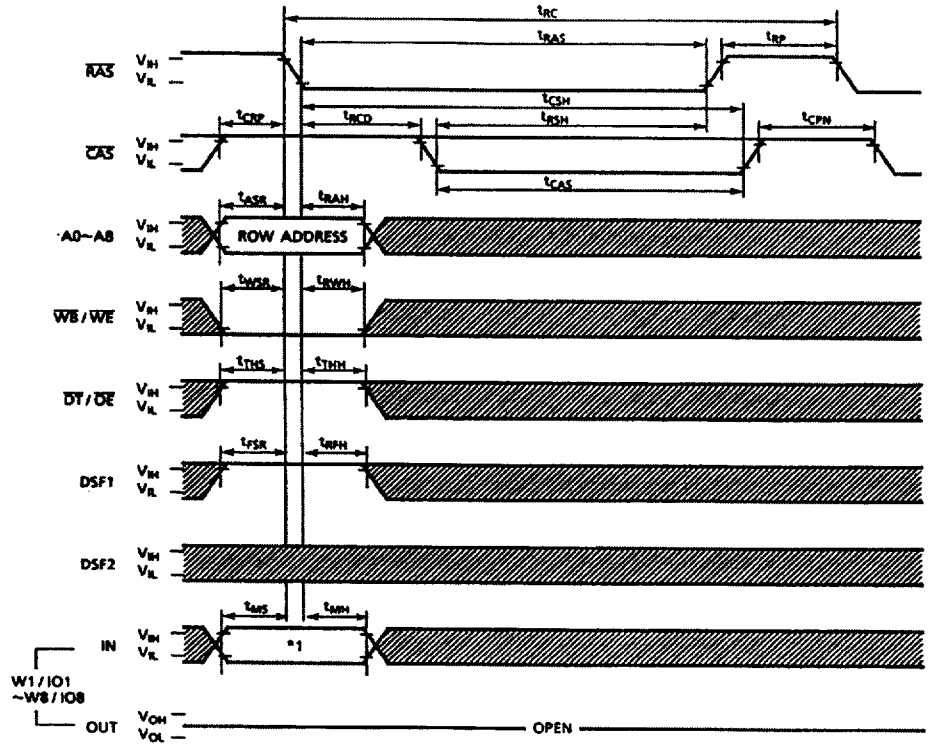
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable
Don't care : '1' or '0'

FLASH WRITE CYCLE

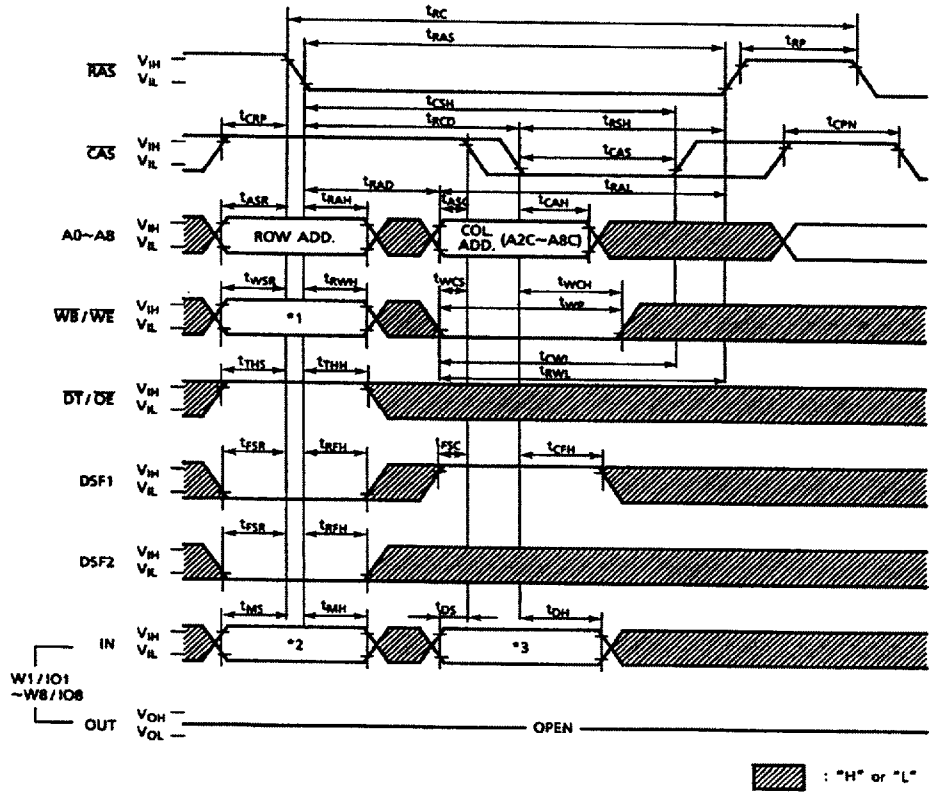


Mask Mode	Cycle
New Mask Mode	WM1 data
Old Mask Mode	Don't care

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

BLOCK WRITE CYCLE (EARLY WRITE)



Mask Mode	*1	*2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

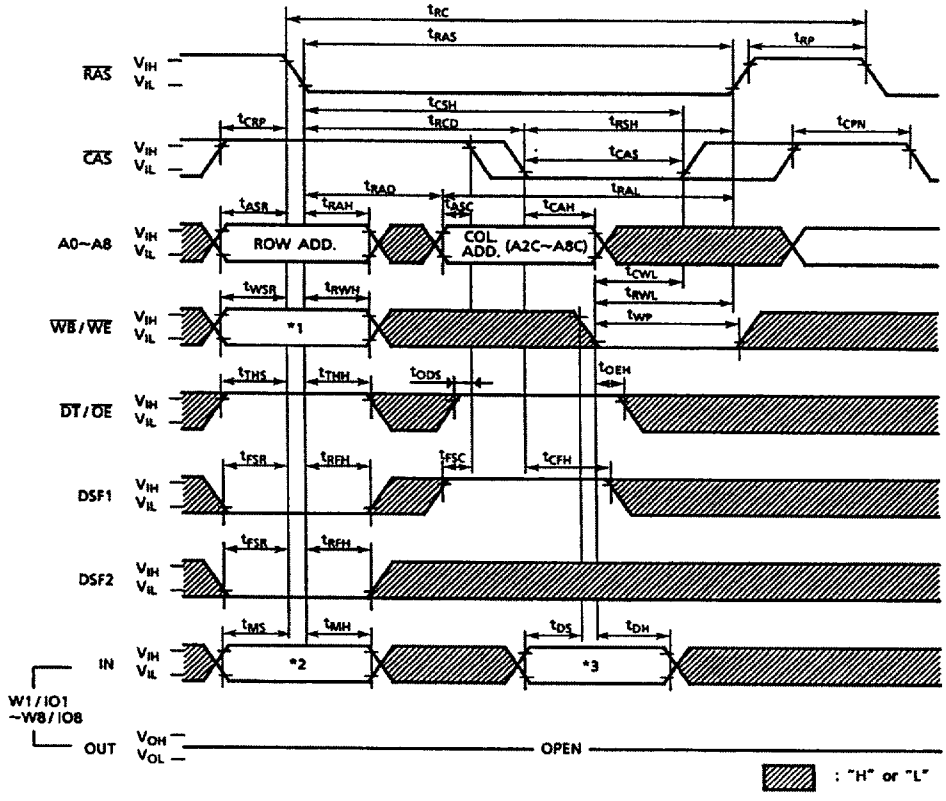
WM1 data 0: Write Disable
1: Write Enable
Don't care : '1' or '0'

***3 COLUMN SELECT**

W1/IO1 - Column 0 ($A_{1C} = 0$, $A_{0C} = 0$)
W2/IO2 - Column 1 ($A_{1C} = 0$, $A_{0C} = 1$)
W3/IO3 - Column 2 ($A_{1C} = 1$, $A_{0C} = 0$)
W4/IO4 - Column 3 ($A_{1C} = 1$, $A_{0C} = 1$)

} Wn/IOn
= 0 : Disable
= 1 : Enable

BLOCK WRITE CYCLE (DELAYED WRITE)



Mask Mode	*1	*2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

WM1 data 0: Write Disable
1: Write Enable

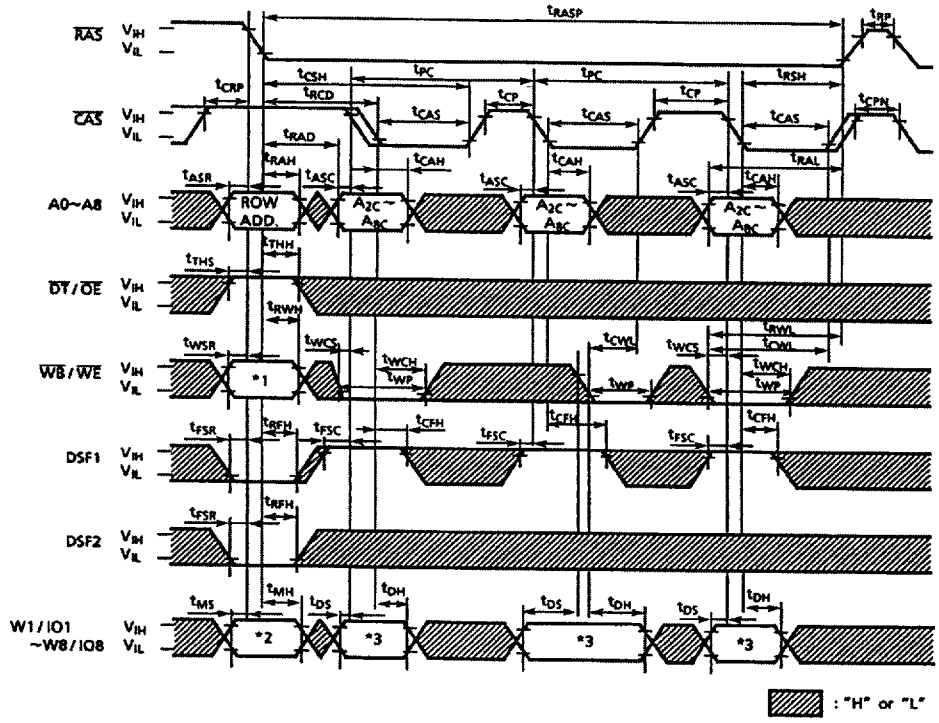
Don't care : '1' or '0'

*3 COLUMN SELECT

W1/IO1 - Column 0 ($A_{1C} = 0$, $A_{0C} = 0$)
W2/IO2 - Column 1 ($A_{1C} = 0$, $A_{0C} = 1$)
W3/IO3 - Column 2 ($A_{1C} = 1$, $A_{0C} = 0$)
W4/IO4 - Column 3 ($A_{1C} = 1$, $A_{0C} = 1$)

} Wn/IOn
= 0 : Disable
= 1 : Enable

FAST PAGE MODE BLOCK WRITE CYCLE



Mask Mode	*1	*2
No Mask Mode	1	Don't care
New Mask Mode	0	WM1 data
Old Mask Mode	0	Don't care

WM1 data 0: Write Disable
1: Write Enable

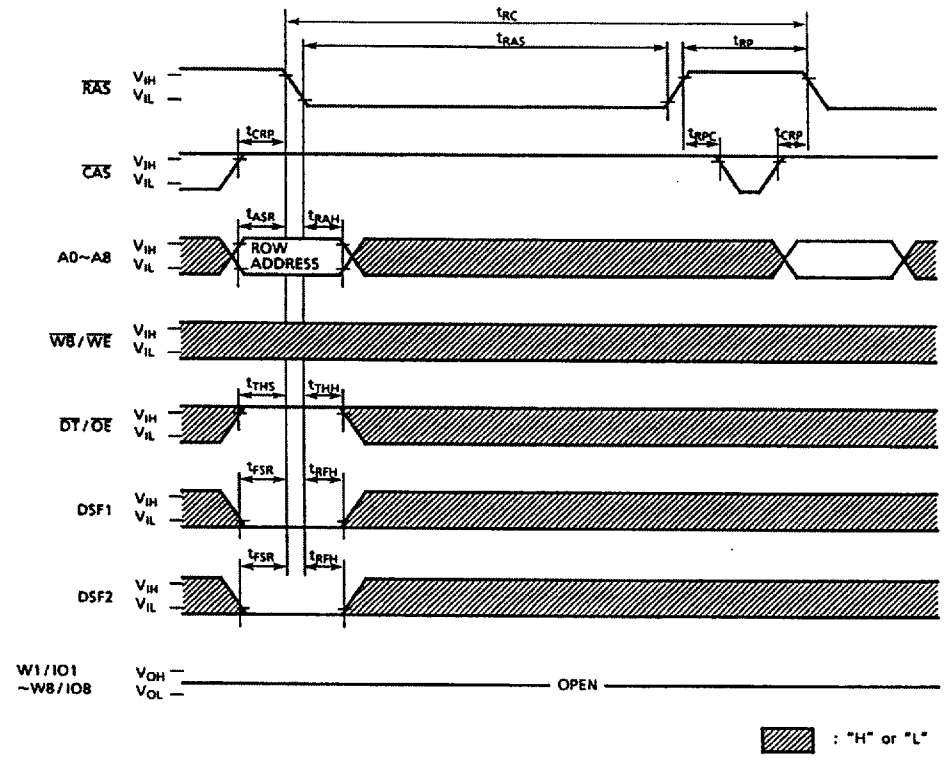
Don't care : '1' or '0'

*3 COLUMN SELECT

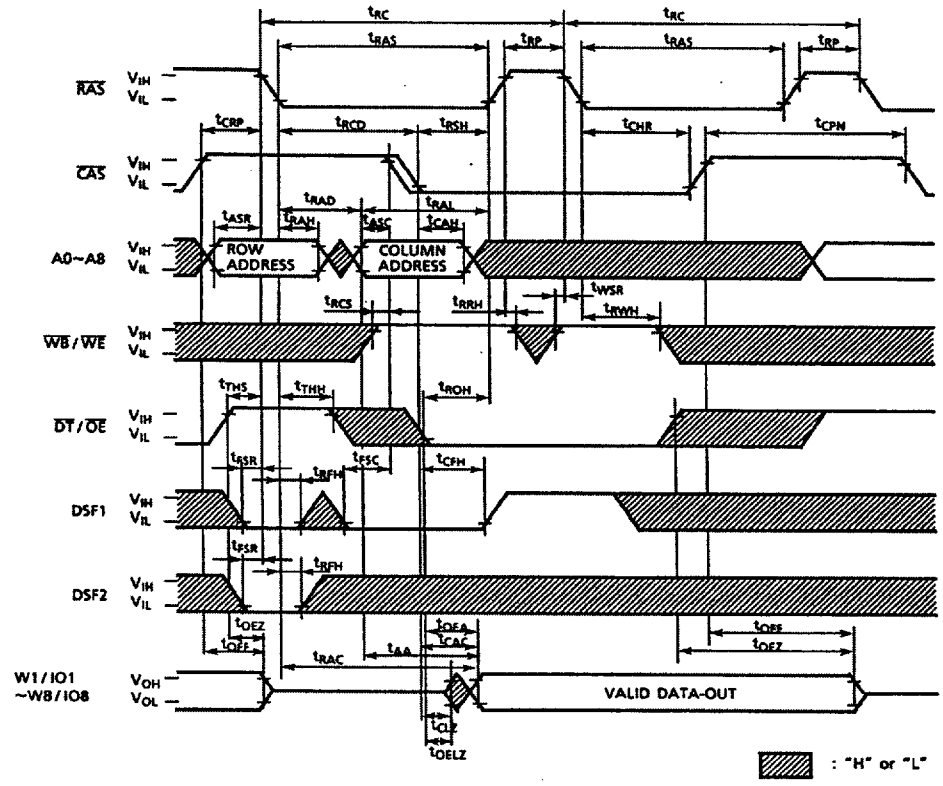
W1/IO1 - Column 0 ($A_{1C} = 0$, $A_{0C} = 0$)
W2/IO2 - Column 1 ($A_{1C} = 0$, $A_{0C} = 1$)
W3/IO3 - Column 2 ($A_{1C} = 1$, $A_{0C} = 0$)
W4/IO4 - Column 3 ($A_{1C} = 1$, $A_{0C} = 1$)

} Wn/IOn
= 0 : Disable
= 1 : Enable

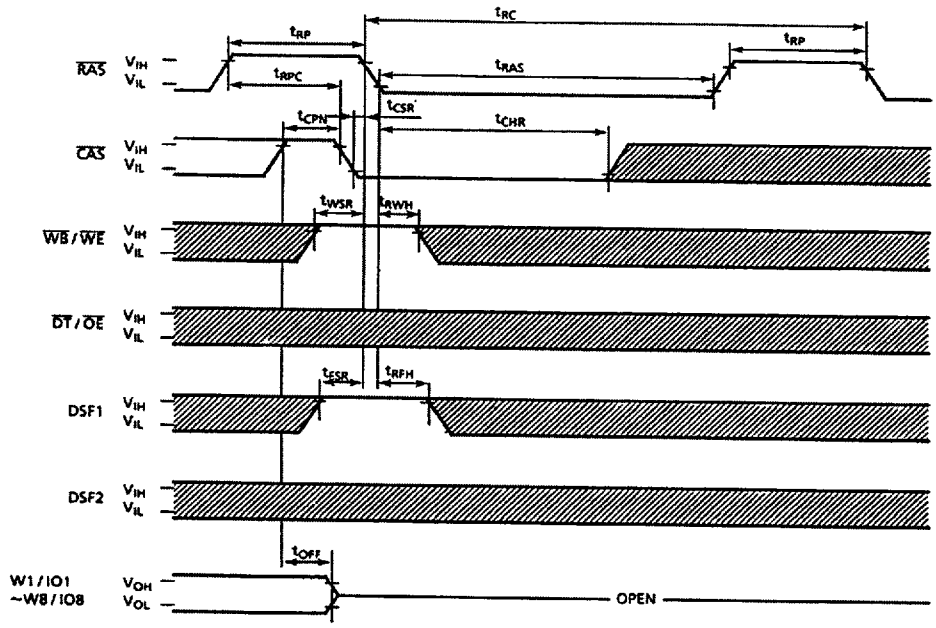
$\overline{RAS}$ ONLY REFRESH CYCLE



HIDDEN REFRESH CYCLE



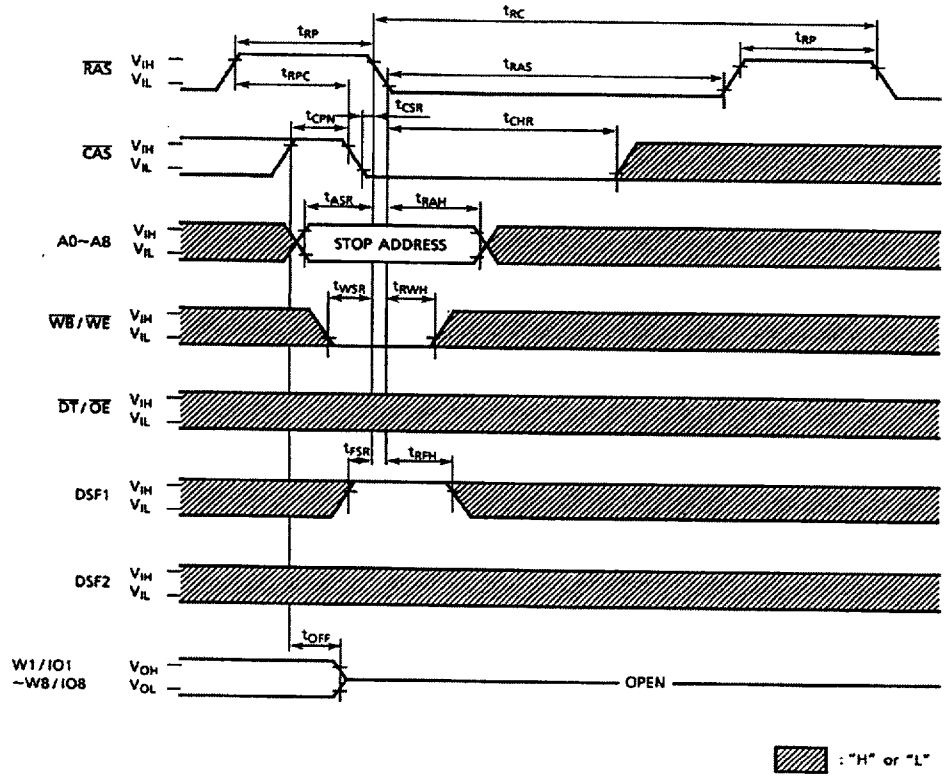
CBR AUTO REFRESH CYCLE



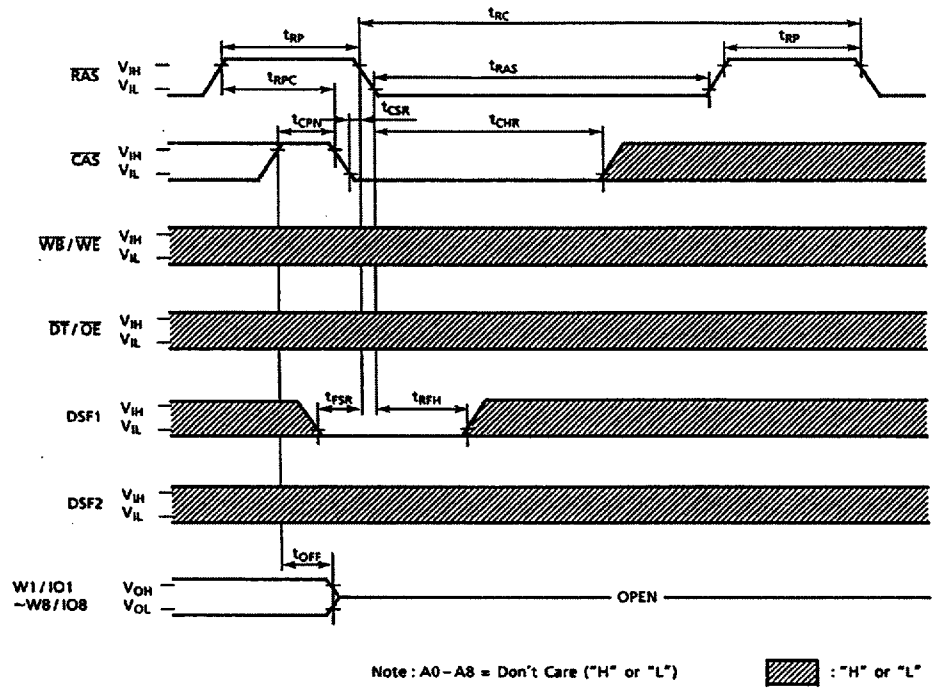
Note : A0 – A8 = Don't Care ("H" or "L")

: "H" or "L"

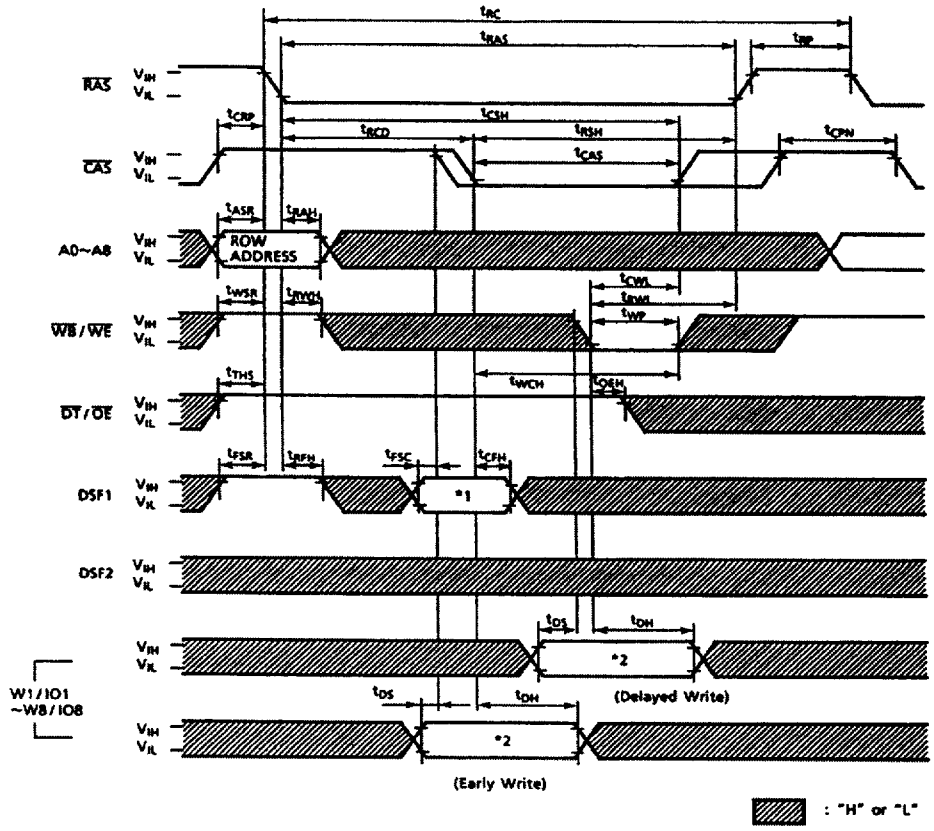
CBR AUTO REFRESH & STOP REGISTER SET CYCLE



CBR AUTO REFRESH & RESET CYCLE

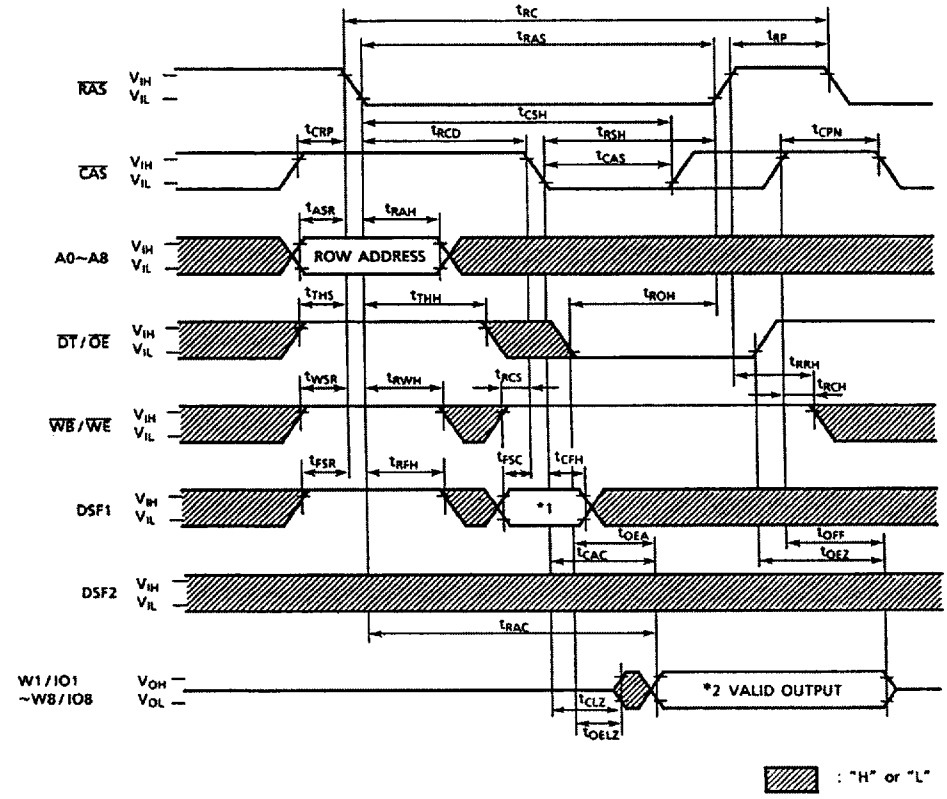


LOAD MASK/COLOR REGISTER CYCLE



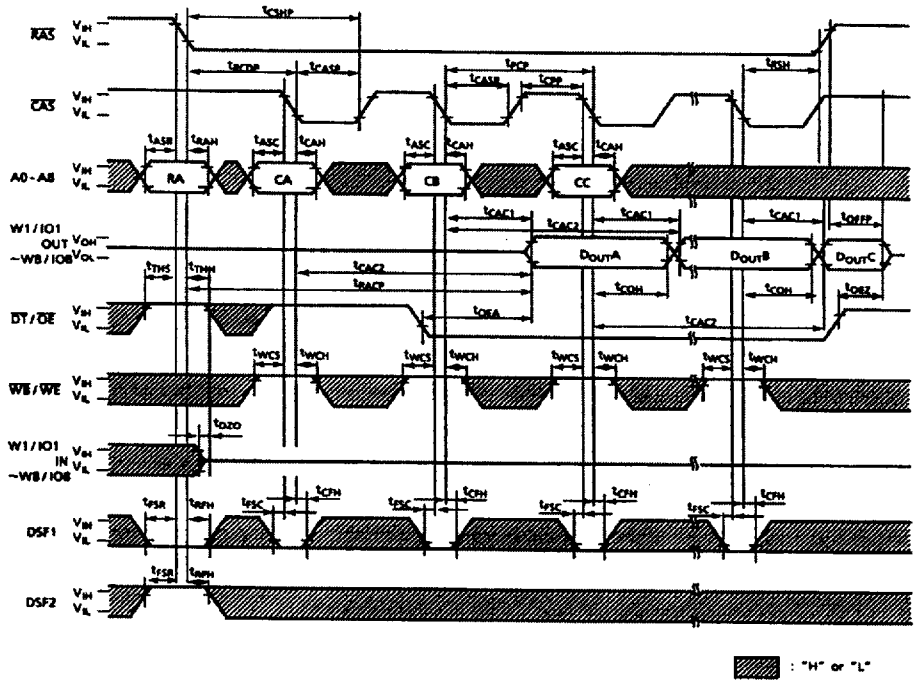
*1	*2	Function
0	Mask data	Load Mask Register Cycle
1	Color data	Load Color Register Cycle

READ MASK/COLOR REGISTER CYCLE

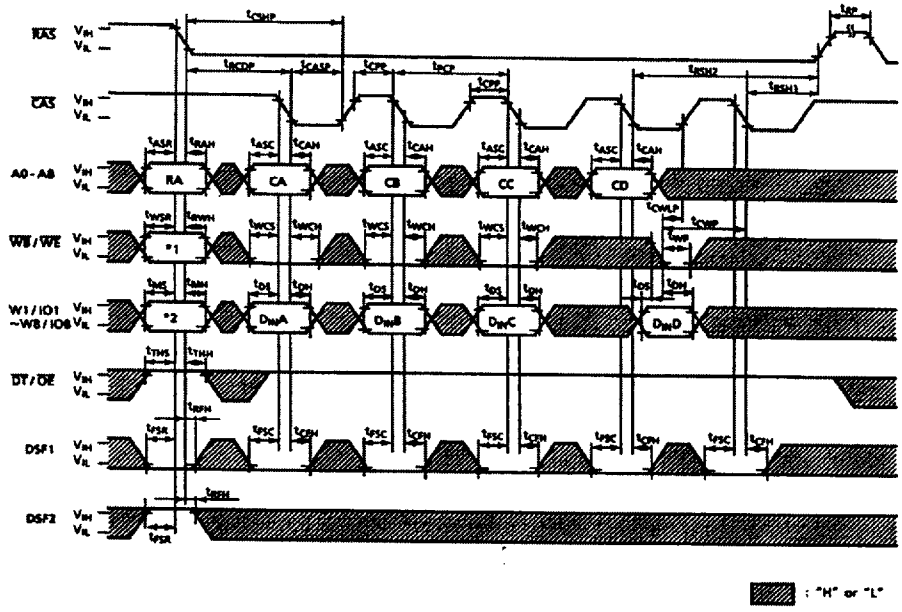


*1	*2	Function
0	Mask data	Load Mask Register Cycle
1	Color data	Load Color Register Cycle

PIPELINED FAST PAGE READ CYCLE



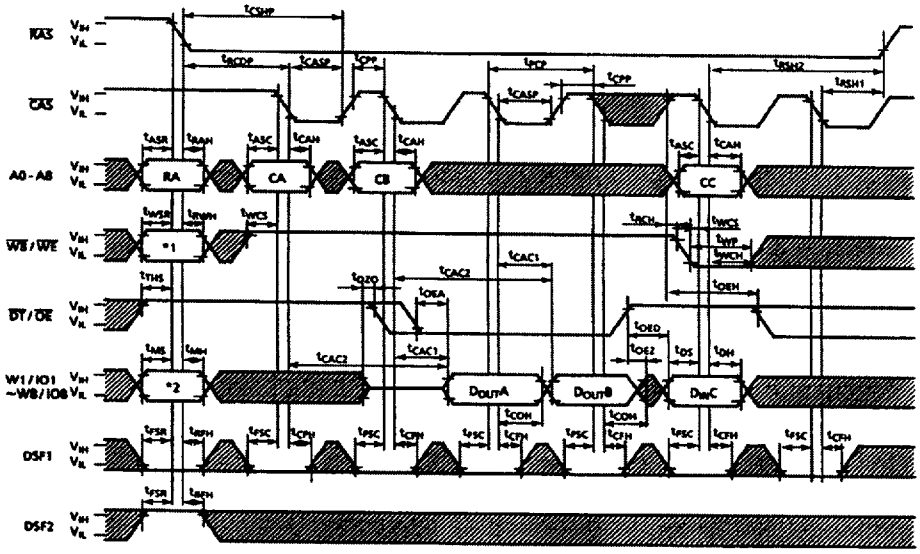
PIPELINED FAST PAGE WRITE CYCLE



Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable
Don't care : '1' or '0'

PIPELINED FAST PAGE READ-WRITE CYCLE

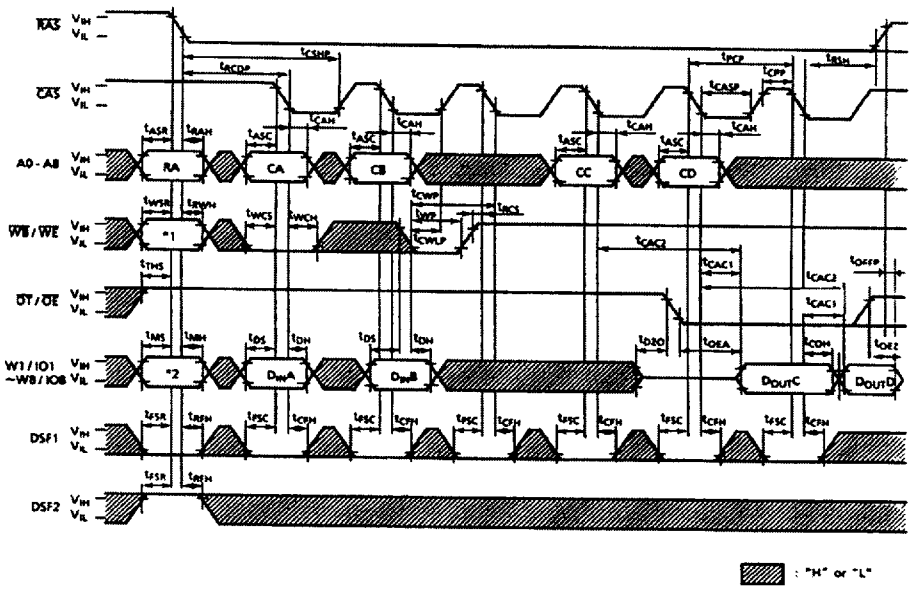


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

PIPELINED FAST PAGE WRITE-READ CYCLE

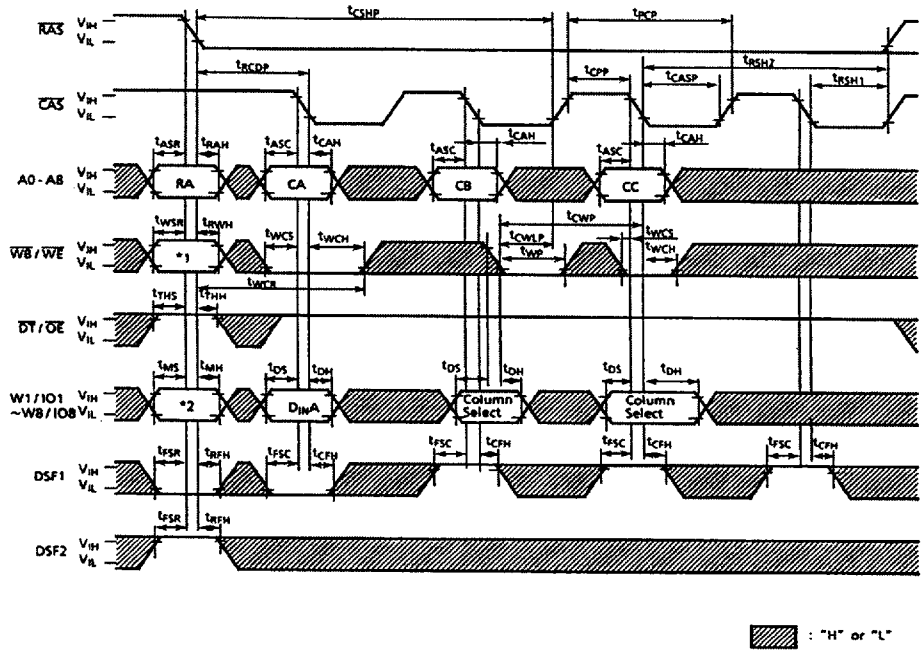


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

PIPELINED FAST PAGE WRITE-BLOCK WRITE CYCLE

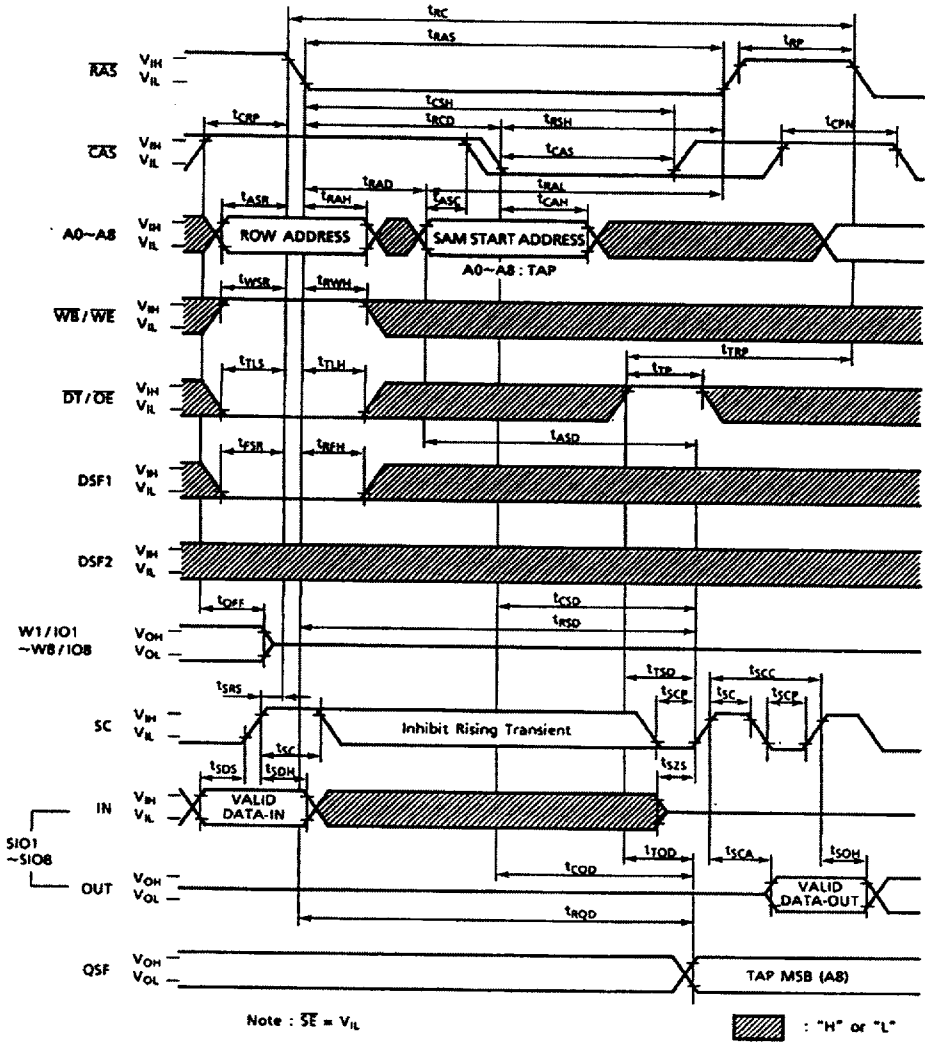


Mask Mode	*1	*2	Cycle
No Mask Mode	1	Don't care	Normal Write
New Mask Mode	0	WM1 data	Write per Bit
Old Mask Mode	0	Don't care	Write per Bit

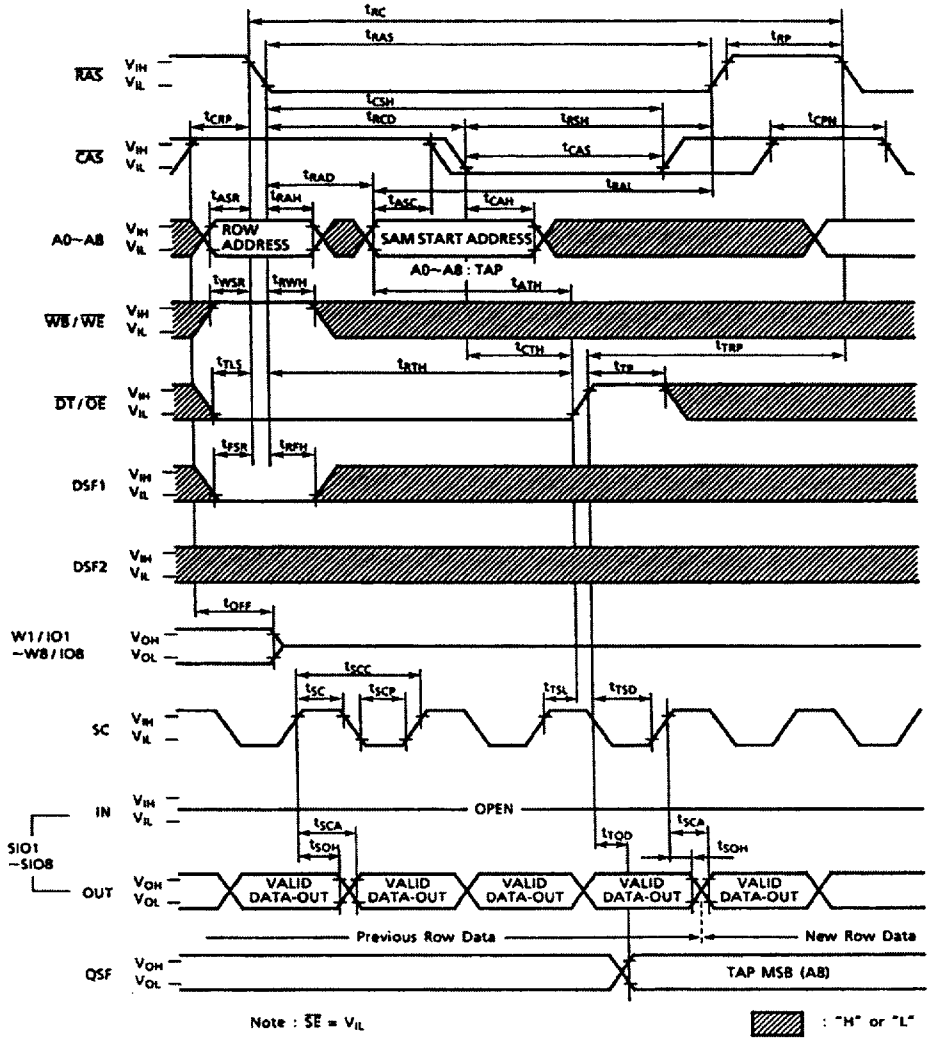
WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

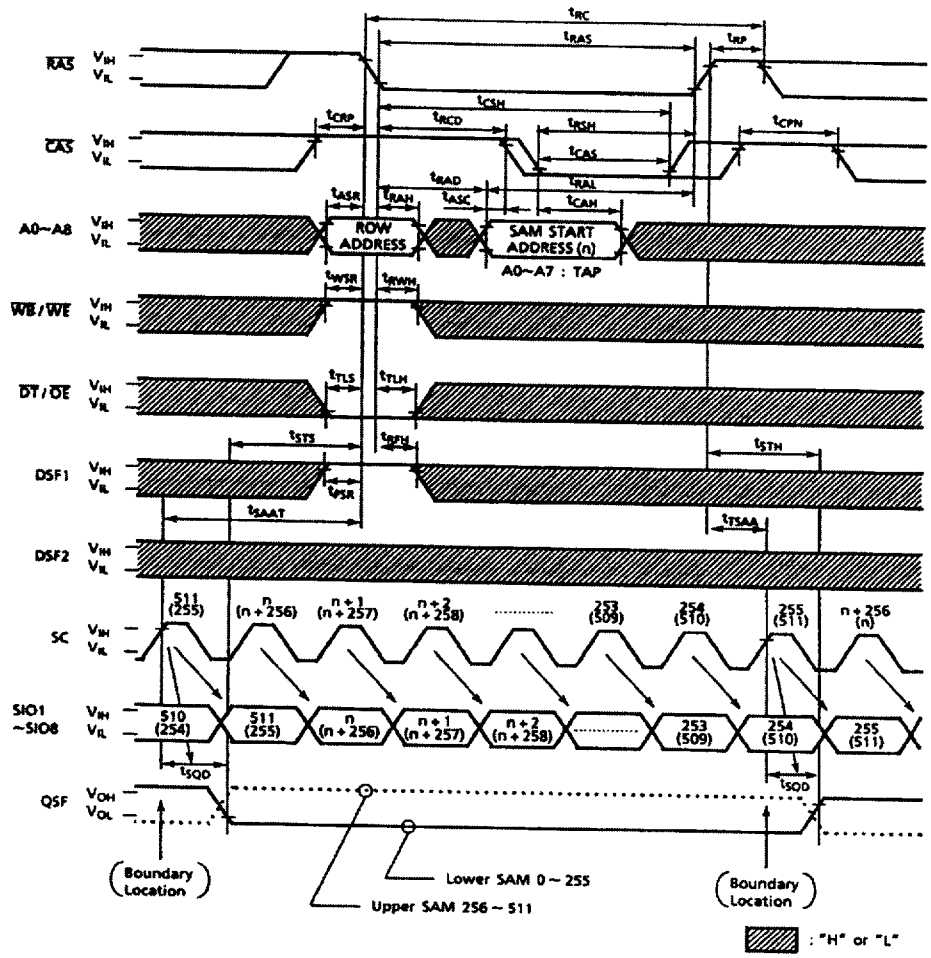
READ TRANSFER CYCLE (Previous Transfer is Write Transfer Cycle)



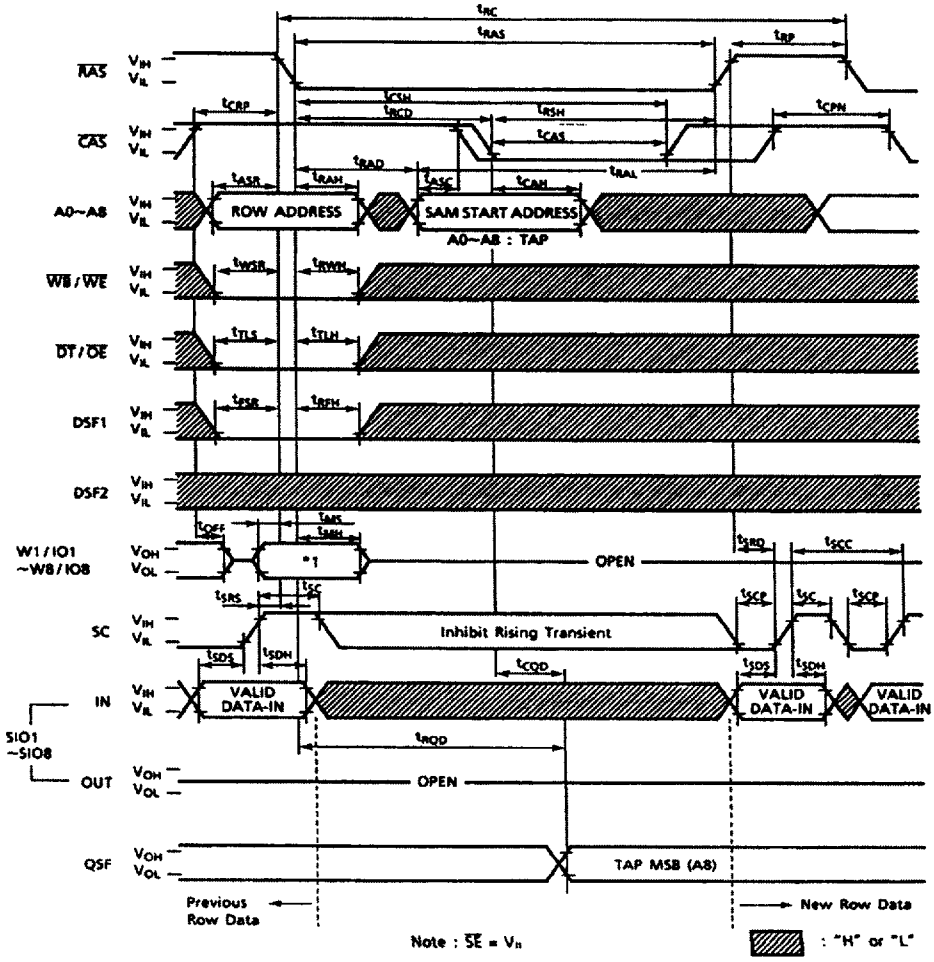
REAL TIME READ TRANSFER CYCLE



SPLIT READ TRANSFER CYCLE



MASKED WRITE TRANSFER CYCLE

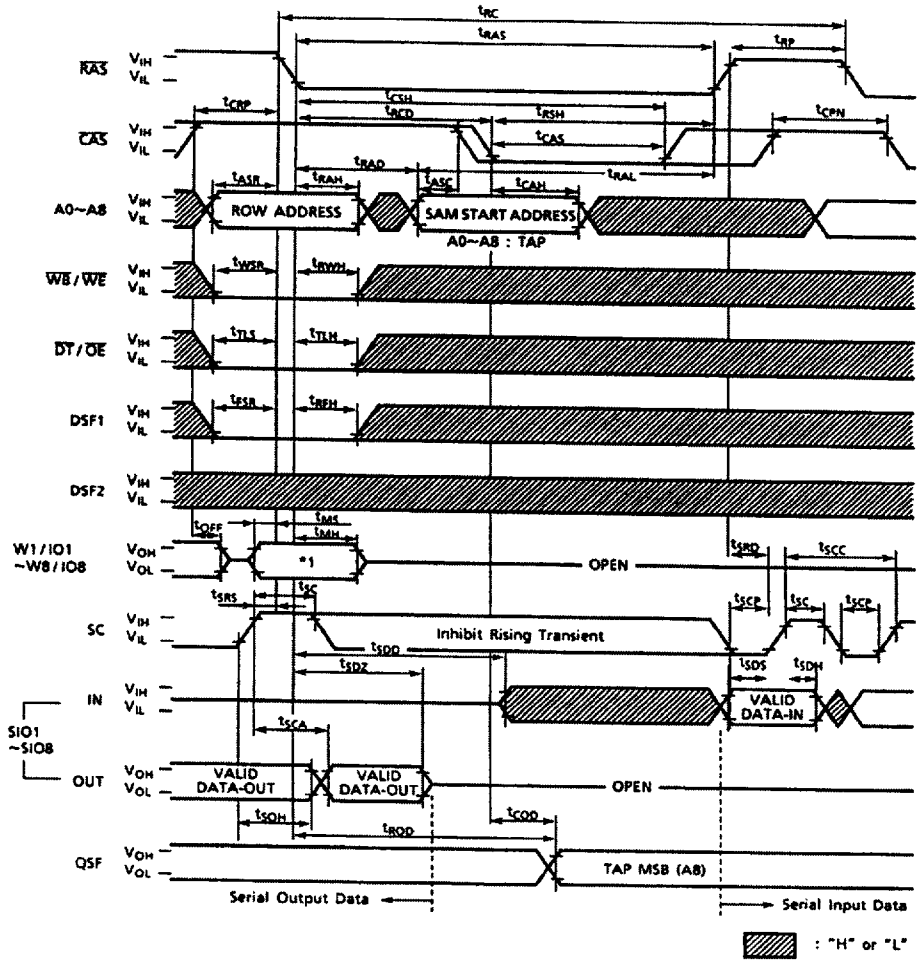


Mask Mode	*1
New Mask Mode	WM1 data
Old Mask Mode	Don't care

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

MASKED WRITE TRANSFER CYCLE (Previous Transfer is Read Transfer Cycle)

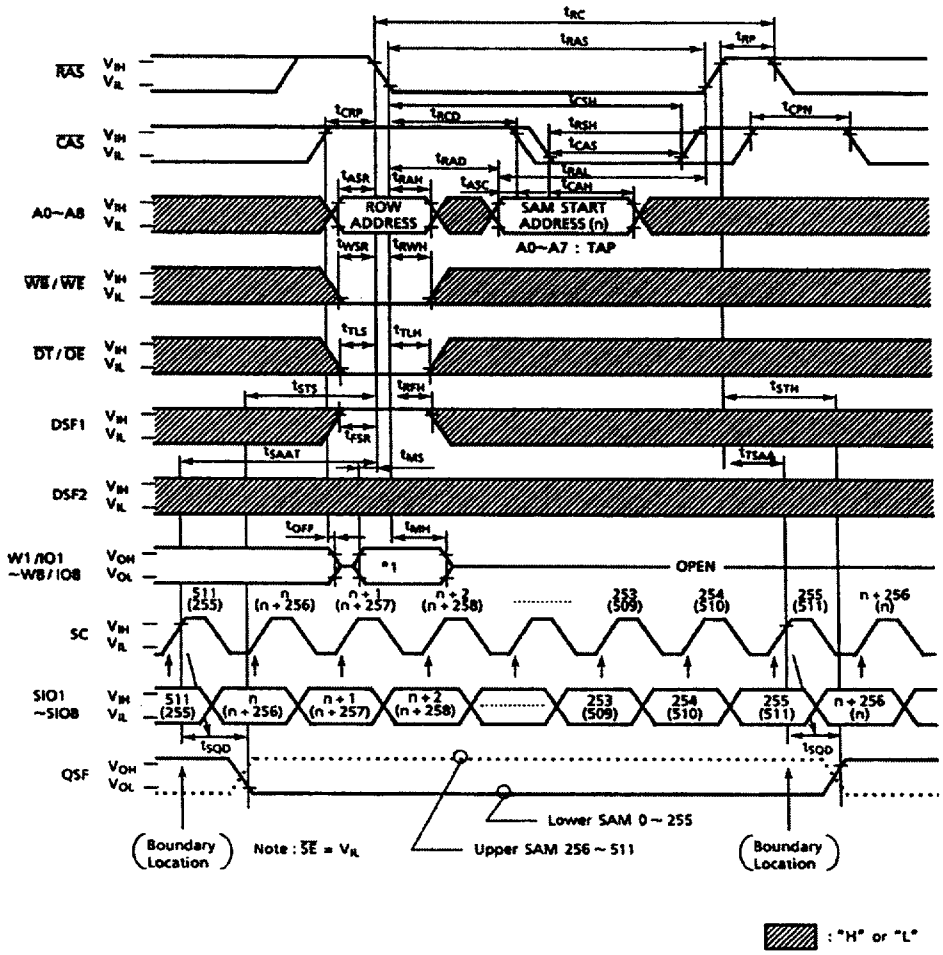


Mask Mode	*1
New Mask Mode	WM1 data
Old Mask Mode	Don't care

WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

MASKED SPLIT WRITE TRANSFER CYCLE

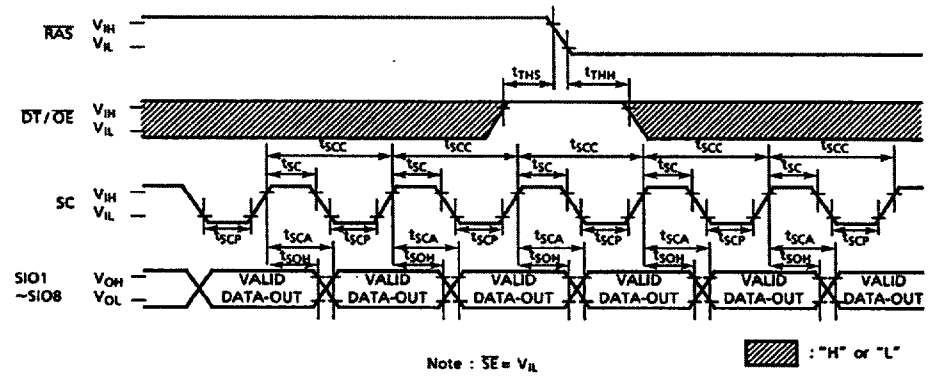


Mask Mode	*1
New Mask Mode	WM1 data
Old Mask Mode	Don't care

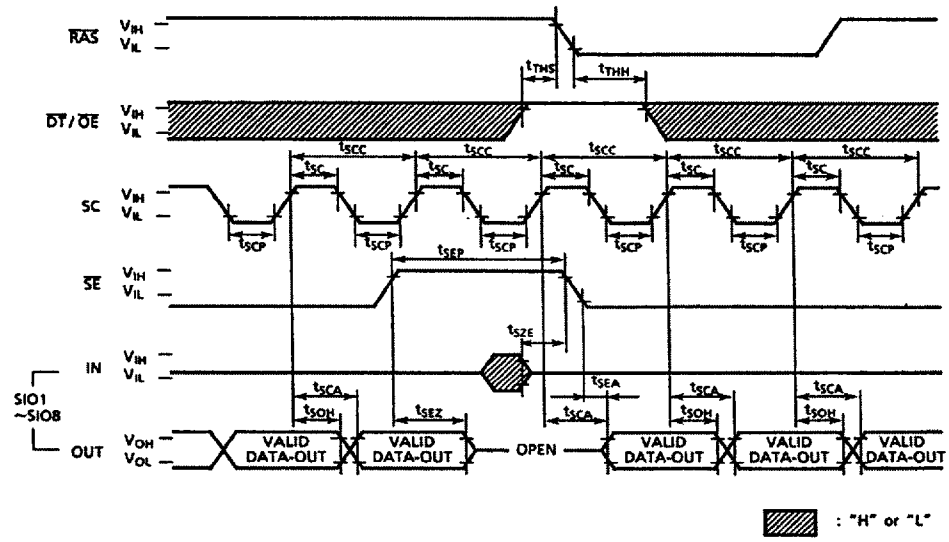
WM1 data 0: Write Disable
1: Write Enable

Don't care : '1' or '0'

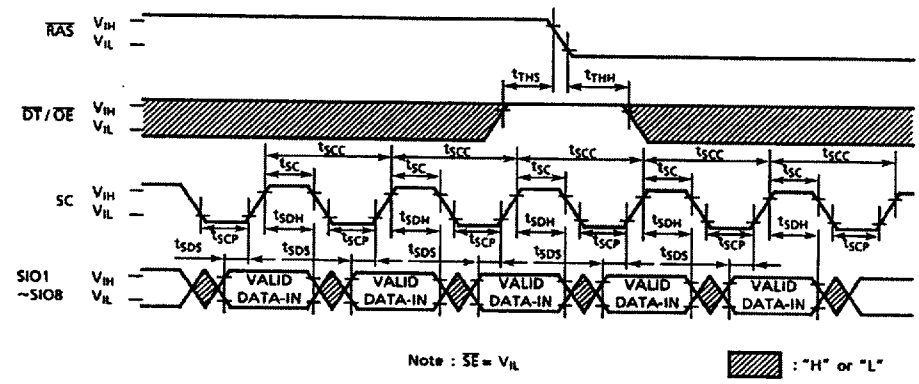
SERIAL READ CYCLE ($\overline{SE} = V_{IL}$)



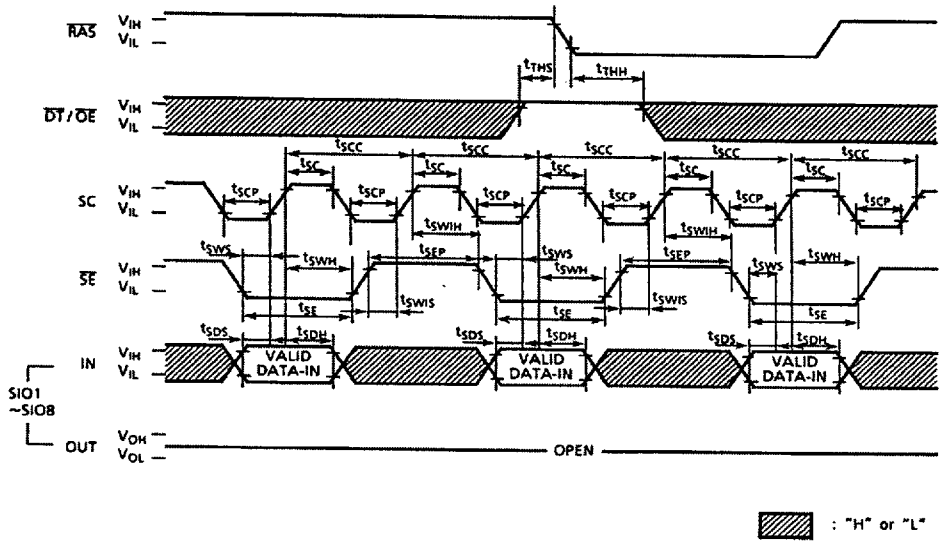
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



SERIAL WRITE CYCLE ($\overline{SE}$ = V_{IL})



SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



PIN FUNCTION

ADDRESS INPUTS : A_0~A_8

The 18 address bits required to decode 8 bits of the 2,097,152 cell locations within the dynamic RAM memory array and they are multiplexed onto 9 address input pins (A_0~A_8). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

ROW ADDRESS STROBE : $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$, DSF1 and DSF2 to invoke the various random access and data transfer operating modes shown in Table 1. $\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

COLUMN ADDRESS STROBE : $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits which are also used for the tap address during the transfer operations. The state of the special function input DSF1 is read at the $\overline{CAS}$ falling edge to select the block write mode or load register functions in conjunction with the $\overline{RAS}$ control. $\overline{CAS}$ before $\overline{RAS}$ refresh operations are selected if the signal is "low" at the $\overline{RAS}$ falling edge.

DATA TRANSFER/OUTPUT ENABLE : $\overline{DT/OE}$

The $\overline{DT/OE}$ input is a multifunction pin. When $\overline{DT/OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT/OE}$ is used as an output enable control. If it is "low", a data transfer operation is activated between the RAM and the SAM.

WRITE PER BIT/WRITE ENABLE : $\overline{WB}/\overline{WE}$

The $\overline{WB}/\overline{WE}$ input is also a multifunction pin. When the signal is "high" at the falling edge of $\overline{RAS}$, during the RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. If the signal is "low" at the $\overline{RAS}$ falling edge, the write-per-bit function is enabled. The $\overline{WB}/\overline{WE}$ input also determines the direction of data transfer between the RAM array and the SAM.

WRITE MASK DATA/DATA INPUT AND OUTPUT: $W_1/IO_1 \sim W_8/IO_8$

Data is written into the RAM through $W_1/IO_1 \sim W_8/IO_8$ pins during a write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs late. In a read cycle data is read out of the RAM on the W_i / IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and column address. The 4 least bits are also used as the column address mask during a block write cycle.

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register at the falling edge of $\overline{RAS}$. In a load mask and color register cycles, the data on the W_i/IO_i pins is stored into the write mask register and the color register respectively.

SERIAL CLOCK : SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. The serial clock SC also increments the 9-bits serial pointer which is used to select the SAM address. The SC pin must be held at a constant V_{IH} or V_{IL} level during read and masked write transfer operations and should not be clocked while the SAM is in standby mode to prevent the SAM pointer from being incremented.

SERIAL ENABLE : $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer is still incremented while SC is clocked.

SPECIAL FUNCTION CONTROL INPUT: DSF 1, DSF 2

DSF1 is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the various TC528257J/Z/FT/TR operations. If the signal is kept "low", the basical functions featured in conventional multi-port DRAM are enabled. To use the block write, the flash write and the load register functions or the split transfer operations, the DSF1 signal needs to be controlled as shown in Table 1.

When the DSF2 signal is "high" at the falling edge of $\overline{RAS}$, pipelined page mode operations are enabled. The pipeline mode is supported with the read, write and block write functions.

SPECIAL FUNCTION OUTPUT: QSF

QSF is an output signal which, during split register mode, indicates which half of the split SAM is being accessed. QSF "low" indicates that the lower split SAM (Bit 0~255) is being accessed and QSF "high" indicates that the upper split SAM (Bit 256~511) is being accessed. QSF is monitored so that after it toggles and after allowing for a delay of t_{STS}, split read/write transfer operation can be performed on the non-active split SAM.

SERIAL INPUT/OUTPUT : SIO_1, SIO_8

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read or masked write transfer cycle. After a read cycle, the SI/Oi pin is in the output mode. When a masked write transfer cycle is performed, the SI/Oi is switched from output mode to input mode,

OPERATION MODE

The RAM port and data transfer operating of the TG528257 are determined by the state of $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$, DSF1 and DSF2 at the falling edge of $\overline{RAS}$ and by the state of DSF1 at the falling edge of $\overline{CAS}$. The Table 1 shows the functional truth table for a listing of all available RAM port and transfer operations.

Table 1. Operaton Truth Table

$\overline{RAS}$ ↓					$\overline{CAS}$ ↓	Mnemonic Code	Function
CAS	$\overline{DT/OE}$	$\overline{WB/WE}$	DSF1	DSF2	DSF1		
0	*	*	0	*	-	CBR	CBR Auto Refresh & Option Reset [1), 2)]
0	*	0	1	*	-	CBRS	CBR Auto Refresh & Stop Register Set[2)]
0	*	1	1	*	-	CBRN	CBR Auto Refresh
1	0	0	0	*	*	MWT	Write Transer (New/Old Mask)[1)]
1	0	0	1	*	*	MSWT	Split Write Transfer (New/Old Mask)[1)]
1	0	1	0	*	*	RT	Read Transfer
1	0	1	1	*	*	SRT	Split Read Transfer
1	1	0	0	0	0	RWM	Read Write (New/Old Mask)[1)]
1	1	0	0	0	1	BWM	BlockWrite (New/Old Mask)[1)]
1	1	0	1	*	*	FWM	FlashWrite (New/Old Mask)[1)]
1	1	1	0	0	0	RW	Read Write (No Mask)
1	1	1	0	0	1	BW	Block Write (No Mask)
1	1	0	0	1	0	RWM(P)	PFP[3)] Read Write (New/Old Mask)[1)]
1	1	0	0	1	1	BWM(P)	PFP[3)] Block Write (New/Old Mask)[1)]
1	1	1	0	1	0	RW(P)	PFP[3)] Read Write (No Mask)
1	1	1	0	1	1	BW(P)	PFP[3)] Block Write (No Mask)
1	1	1	1	*	0	LMR	Load (Old) Mask Register[1)]
1	1	1	1	*	1	LCR	Load Color Register

Note : * =0 or 1, - = Not applicable

1) After LMR operation, MWT, MSWT, RWM, BWM, FWM, RWM (P), BWM (P) use old mask. CBR operation resets the old mask mode to new mask mode.

2) CBRS operation determines binary boundaries in the SAM. CBR operation resets the boundaries.

3) PFP stands for pipelined fast page mode

RAM PORT OPERATION

1. READ WRITE FUNCTION : RW

The TC528257 is equipped with the read write function which is identical to the conventional dynamic RAM's one and supports read, early write, $\overline{OE}$ controlled write and read-modify-write cycles as shown in the timing charts. Fast page and pipelined page modes are available with the read write cycles by performing multiple $\overline{CAS}$ cycles during a single active $\overline{RAS}$ cycle, a page.

2. WRITE-PER-BIT (MASKED WRITE) FUNCTION : RWM

The write-per-bit (masked write) function selectively controls the internal write enable circuits of the RAM port. When $\overline{WB}/\overline{WE}$ is held "low" at the falling edge of $\overline{RAS}$, during the RWM cycle, the write mask is enabled. At the same time, the mask data on the Wi/IOi pins is latched into the write-mask register. The I/O mask data maintains in a single $\overline{RAS}$ cycle, a page (New Mask Mode). When a load mask register function (LMR) is performed, the write mask data on the Wi/IOi pins is latched into the write-mask register. After the LMR operation, the data at the falling edge of $\overline{RAS}$ during the RWM cycle is ignored and the I/O mask data that was stored in the write-mask register is used (Old Mask Mode) until the mode is reset by CBR operation The truth table of the write-per-bit functon is shown in Table 2.

Table 2. Truth table for write-per-bit function

At the falling edge of $\overline{RAS}$				Write Mask Register	Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	W_i/IO_i (i=1~8)		
H	H	L	1	←	Write Enable
			0	←	Write Disable (New Mask)
			*	1	Write Enable
			*	0	Write Disable (Old Mask)

Note: * = 1 or 0 , ← = The data on Wi/IOi is latched.

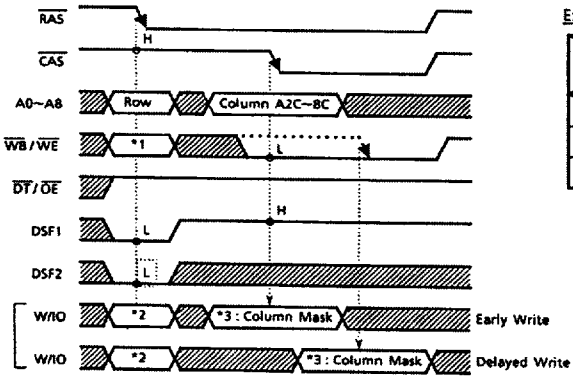
3. BLOCK WRITE AND MASKED BLOCK WRITE : BW & BWM

Block write is a special RAM port write operation which, in a page, allows for the data in the color register to be written into 4 consecutive column address locations starting from a selected column address in a selected row. The block write operation can be selectively disabled on an I/O basis and a column mask capability is also available.

A block write cycle is performed by holding $\overline{CAS}$, $\overline{DT/OE}$ "high" and DSF1 "low" at the $\overline{RAS}$ falling edge and by holding DSF1 "high" at the $\overline{CAS}$ falling edge. If the DSF signal is "low" at the $\overline{CAS}$ falling edge, a read write operation will occur. Therefore, a combination of block write, read and write operations can be performed during a fast page mode cycle. The state of $\overline{WB/WE}$ input at the falling edge of $\overline{RAS}$ determines whether or not the I/O mask is enabled ($\overline{WB/WE}$ must be "low" to enable the I/O mask, BMW mode or "high" to disable it, BW mode). The I/O mask is provided on the Wi/IOi input at the $\overline{RAS}$ falling edge. After LMR operation, however, the old mask is used for the I/O mask function. The column mask data on the Wi/IOi input must be provided at the $\overline{CAS}$ or $\overline{WB/WE}$ falling edge whichever is late, while the seven most significant colunm address (A2C~A8C) are latched at the falling edge of $\overline{CAS}$.

An example of the block write function is shown in Figure 1 with a mask on W_3/IO_3, W_4/IO_4, W_6/IO_6, W_8/IO_8 and column 1. The block write is most effective for window clear and fill operation in frame buffer applications.

Figure 1. Block Write Operation



Example

	W/IO							
	1	2	3	4	5	6	7	8
WM1 Register	1	1	(0)	(0)	1	(0)	1	(0)
Column Select	1	(0)	1	1	–	–	–	–
Color Register	1	0	1	0	1	1	0	0

Result

	W/IO							
	1	2	3	4	5	6	7	8
Column 0	1	0			1		0	
Column 1								
Column 2	1	0			1		0	
Column 3	1	0			1		0	

*1	*2	Mask Mode
1	Don't Care	No Mask Mode
0	WM1	New Mask Mode
0	Don't Care	Old Mask Mode

***3 COLUMN SELECT**

W_1/IO_1 - Column 0 (A1C = 0, A0C = 0
W_2/IO_2 - Column 1 (A1C = 0, A0C = 1
W_3/IO_3 - Column 2 (A1C = 1, A0C = 0
W_4/IO_4 - Column 3 (A1C = 1, A0C = 1

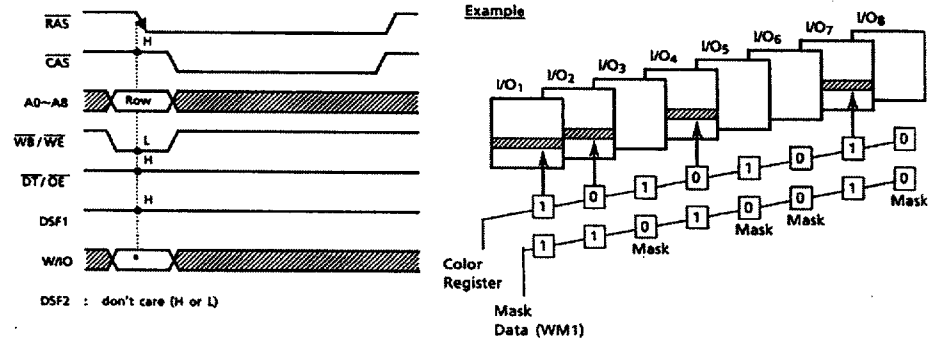
4. FLASH WRITE : FWM

Flash write is also a special RAM port operation which in a single $\overline{RAS}$ cycle, allows for the data in the color register to be written into all the memory locations of a selected row. Each bit of the color register corresponds to one of the DRAM I/O blocks and the flash write operation can be selectively controlled on an I/O basis in the same manner as the write-per-bit operation.

A flash write cycle is performed by holding $\overline{CAS}$ "high", $\overline{WB}/\overline{WE}$ "low" and DSF1 "high" at the falling edge of $\overline{RAS}$. The mask data must also be provided on the Wi/IOi inputs in order to enable the flash write operation for selected I/O blocks. After a LMR operation, however, the old mask in the mask register is used for the I/O block masking.

Flash write is most effective for fast plane clear operations in frame buffer applications. Selected planes can be cleared by performing 512 flash write cycle and by specifying a different row address location during each flash write cycle. Assuming a cycle time of 130ns, a plane clear operation can be completed in less than 66.6 μ sec.

Figure 2. Flash Write Operation



*	Mask Mode
Mask Data	New Mask Mode
Don't Care (H or L)	Old Mask Mode

5. PIPELINED FAST PAGE MODE : RWM (P), BWM (P), RW (P), BW (P)

Pipelined fast page mode allows much faster access to the memory than the conventional page mode. Read, write and block write cycles are available at the pipelined fast page mode timings.

A pipelined fast page mode is performed by holding DSF2 "high" at the falling edge of $\overline{RAS}$. A pipelined fast page read, write and block write operations can run at 30ns cycle time for 70ns version. Also, those mode can be selected every $\overline{CAS}$ cycle by the status of $\overline{DT/OE}$, $\overline{WB/WE}$ and DSF1 pin. There are, however, penalties on the performance as follows

(1) Two $\overline{CAS}$ cycles are required for the read operation. The fast access, hence, takes longer than page mode. Also, one $\overline{CAS}$ cycle is needed to read out the data before the write cycle starts in the same page.

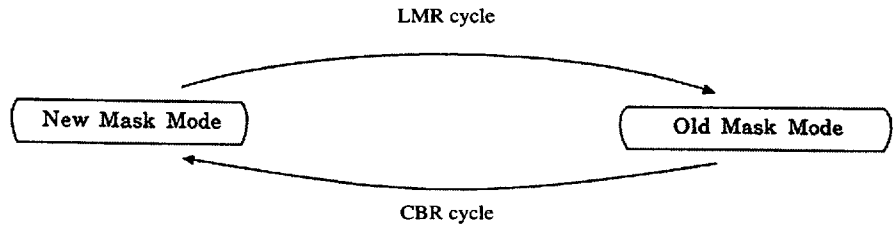
(2) One dummy cycle is needed to complete the write and block write operation. The cycle is, thus, needed between the write and the read operation and is required before the page ends.

A system designer needs to carefully estimate the system performances with the pipelined page mode and the conventional page mode in order to decide which mode should be used.

6. LOAD (OLD) MASK REGISTER : LMR

The TC528257 has an on-chip 8-bit write-mask register which provides the I/O mask data during the masked functions such as the write-per-bit (RWM), masked block write (BWM), flash write (FWM) and write transfer (MWT, MSWT) functions. Each bit of the write-mask register corresponds to one of the DRAM I/O blocks. After the mask data is specified in the write-mask register by using the load mask register (LMR) cycle, the old mask mode is invoked during the masked functions. The I/O mask data in the write-mask register maintains until another LMR operation is performed during the old mask mode. The LMR cycle is initiated by holding $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$ and DSF1 "high" at the falling edge of $\overline{RAS}$ and by DSF1 "low" at the falling edge of $\overline{CAS}$. The data presented on the Wi/IOi lines are subsequently latched into the write-mask register at the falling edge of either $\overline{CAS}$ or $\overline{WB/WE}$, whichever occurs later. The old mask mode is reset to the new mask mode by a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR). During the LMR cycle, the memory calls of the row address which is latched at the falling edge of $\overline{RAS}$ are refreshed.

Figure 3. State Diagram of Mask Mode



7. LOAD COLOR REGISTER : LCR

The TC528257 is provided with an on-chip 8-bits register (color register) for use during the block write or flash write function. Each bit of the color register corresponds to one of the DRAM I/O blocks. The load color register cycle is initiated by holding $\overline{CAS}$, $\overline{WB/WE}$, $\overline{DT/OE}$ and DSF1 "high" at the falling edge of $\overline{RAS}$. The data presented on the Wi/IOi lines is subsequently latched into the color register at the falling edge of either $\overline{CAS}$ or $\overline{WB/WE}$, whichever occurs later. During the load color register cycle, the memory cells on the row address latched at the falling edge of $\overline{RAS}$ are refreshed.

8. REFRESH

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of 512 rows in the DRAM array within the specified 8 ms refresh period. The TC528257 supports the conventional dynamic RAM refresh operations such as $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh and hidden refresh.

8.1 $\overline{CAS}$ before $\overline{RAS}$ Refresh and Option Reset : CBR

The CBR cycle reset the following functions, performing the $\overline{CAS}$ before $\overline{RAS}$ refresh operation at the same time.

- To reset the old mask mode to the new mask mode for the masked functions.
- To reset the stop register and remove the binary boundaries for the split SAM operation,

The systems which implement neither the old mask mode nor the binary boundary in the SAM is recommended to use the CBR cycle for refresh operation.

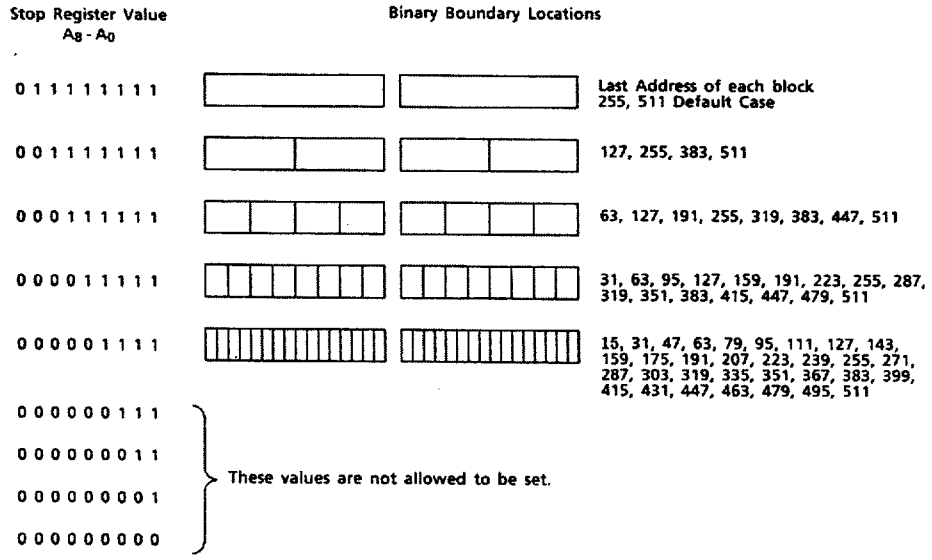
8.2 $\overline{CAS}$ before $\overline{RAS}$ Refresh : CBRN

The CBRN cycle performs only the $\overline{CAS}$ before $\overline{RAS}$ refresh operation. The systems which implement either the old mask mode or the binary boundary in the SAM usually use the CBRN cycle for refresh operation except for at the required stop register set or option reset cycles. The CBRN cycle must not be used during the initialization after power-up.

8.3 $\overline{CAS}$ before $\overline{RAS}$ Refresh and Stop Register Set : CBRS

The CBRS cycle sets the stop register to place binary boundaries in each half SAM, performing the $\overline{CAS}$ before $\overline{RAS}$ refresh operation at the same time. The CBRS cycle is initiated by $\overline{CAS}$ holding "low" and by $\overline{WB}$ /$\overline{WE}$ and DSF1 "high" at the falling edge of $\overline{RAS}$. At the same time the data on the address pins, A_0 - A_8 is latched and the binary boundaries in each half SAM will be available when a split transfer operation is performed.

Figure 4 . Stop Register and Binary Boundary Location



DATA TRANSFER OPERATION

The TC528257 features two types of internal bidirectional data transfer capability between the RAM and the SAM, as shown in Figure 5. During a normal transfer, 512 words by 8-bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer), During a split transfer, 256 words by 8-bits of data can be loaded from the lower / upper half of the RAM into the lower / upper half of the SAM (Split Read Transfer) or from the lower/upper half of the SAM into the lower/upper half of the RAM (Split Write Transfer). The normal transfer and split transfer modes are controlled by the DSF1 input signal

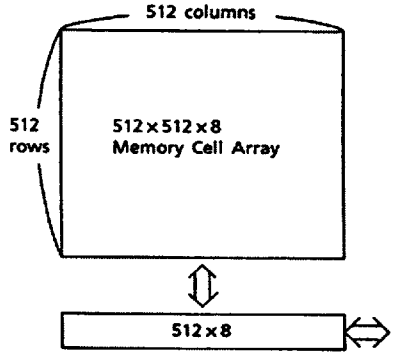
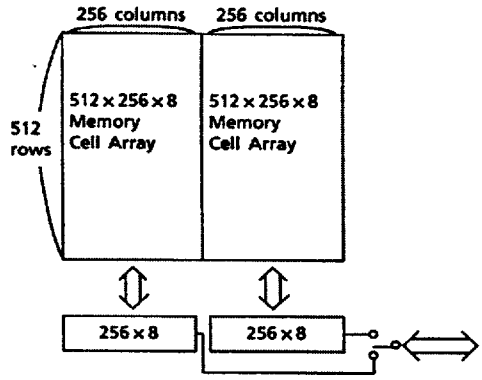


Figure 5. (a) Normal Transfer



(b) Split Transfer

Table 3. Shows the truth table of each Transfer Modes

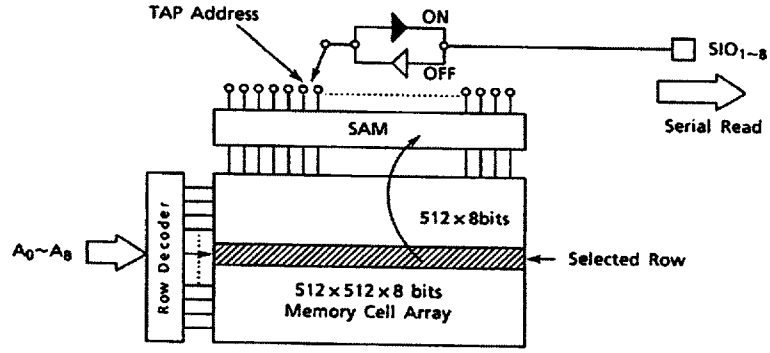
$\overline{RAS}$				Mnemonic Code	Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
CAS	$\overline{DT/OE}$	$\overline{WB/WE}$	DFS1					
H	L	H	L	RT	Read Transfer	RAM → SAM	512x8	Input → Output
H	L	L	L	WT	Write Transfer (New/Old Mask)	SAM → RAM	512x8	Output → Input
H	L	H	H	SRT	Split Read Transfer	RAM → SAM	256x8	Not changed
H	L	L	H	SWT	Split Write Transfer (New/Old Mask)	SAM → RAM	256x8	Not changed

9. READ TRANSFER CYCLE : RT

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT/OE}$ "low" $\overline{WB/WE}$ "high" and DSF1 "low" at the falling edge of $\overline{RAS}$, The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. At the same time, the SAM port is set into the output mode. The start address of the serial pointer of the SAM (TAP address) is determined by the column address selected at the falling edge of $\overline{CAS}$. By doing a tight timing control between the $\overline{DT/OE}$ rising edge and SC falling edge, a real time read transfer operation can also be performed.

Figure 6 shows the operation block diagram for read transfer operation.

Figure 6. Block Diagram for Read Transfer Operation



In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT/OE}$ and the falling edge of $\overline{RAS}$ and $\overline{CAS}$, as shown in READ TRANSFER CYCLE timing chart.

10. WRITE TRANSFER CYCLE : WT

A write transfer cycle consists of loading the content of the SAM register into a selected row of the RAM array. The write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT/OE}$ "low", $\overline{WB/WE}$ "low", and DSF1 "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM (TAP address). After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

The write transfer is selectively controlled per RAM I/O block by setting the mask data on the Wi/IOi lines at the falling edge of $\overline{RAS}$ (some as in the write-per-bit operation). Before the serial clock starts loading the data into the SAM through SIO pins, the write transfer operation with all I/O blocks disabled must be performed in order to change the SAM port from output. Please note that the conventional pseudo write transfer is not available in the TC528257. The mask function is switched between the new and old mask mode by the LMR and CBR cycle.

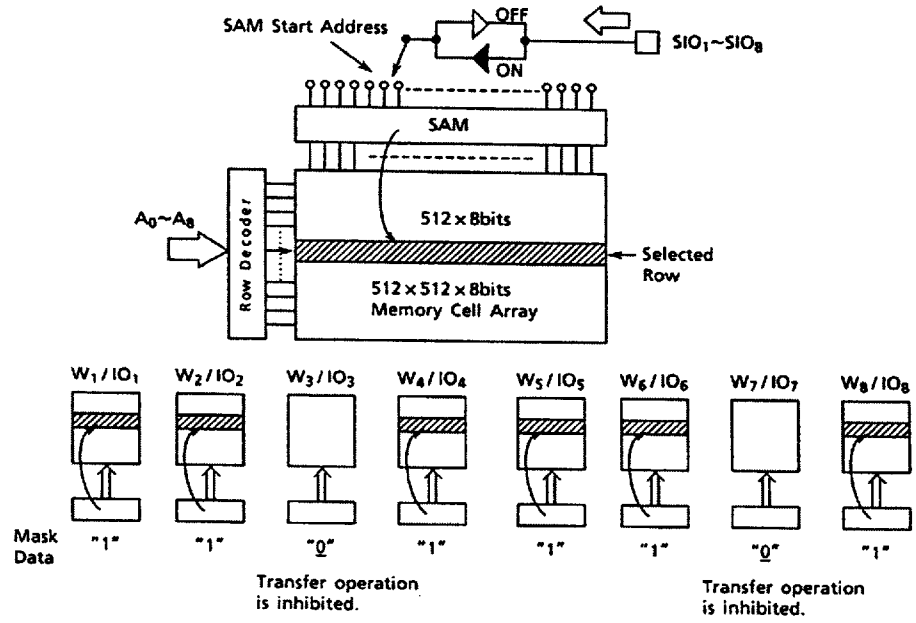


Figure 7. Block Diagram for Write Transfer Operation

When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

11. SPLIT READ TRANSFER CYCLE : SRT

A split read transfer consists of loading 256 words by 8-bits of data from a selected row of the half RAM array into the corresponding half SAM in stand-by mode, Serial data can be shifted out of the other half of the SAM in active mode simultaneously, as shown in Figure 8. The most significant column address (A8C) is controlled internally to determine which half of the SAM will be reloaded from the RAM-array; During the split read transfer operation, the RAM port control signals do not have to be synchronized with the serial clock SC, thus eliminating the timing restrictions as in the case of real time read transfers. Prior to the execution of the split read transfer operation, a (normal) transfer operation must be performed to determine the absolute tap address location. QSF is an output that indicates which half of the SAM is in the active state.

QSF changes state when the last SC clock is applied to the active SAM, as shown in Figure 9.

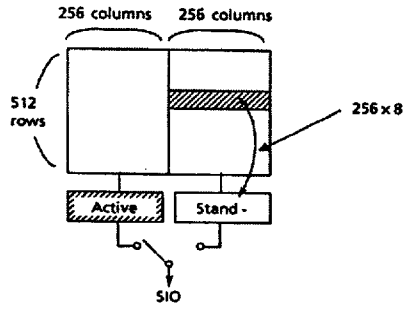


Figure 8. Split Read Transfer

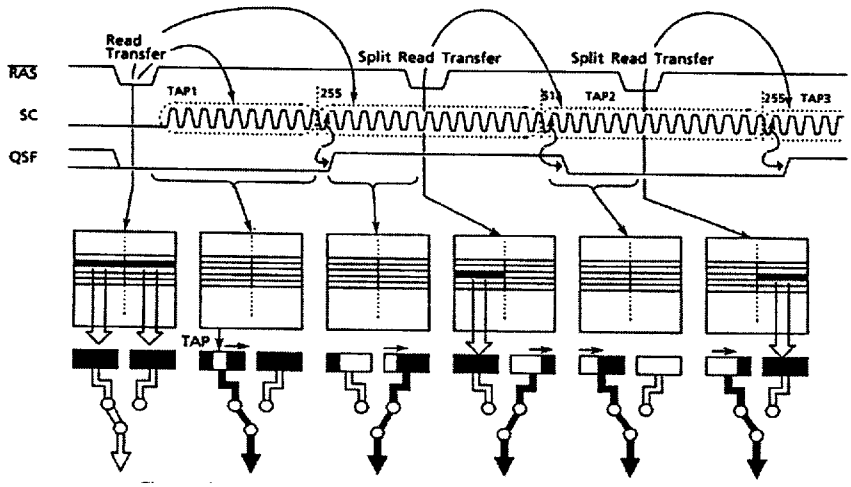


Figure 9. Example of Consecutive Read Transfer Operations

12. SPLIT WRITE TRANSFER : MSWT

A split write transfer is the similar function to the split read transfer. The difference is that the transfer direction is from the stand-by half SAM into a selected row of the corresponding half RAM array, Also, serial data can be shifted into the other half of the SAM simultaneously, as shown in Figure 10. New and old mask capability is supported in the MSWT cycle as is in the write transfer operation. Prior to the execution of the split write transfer operation, a write transfer operation, in which all I/O blocks are usually disabled, must precede to switch the SAM port from output mode to input mode and to set the initial TAP location for the serial input operation.

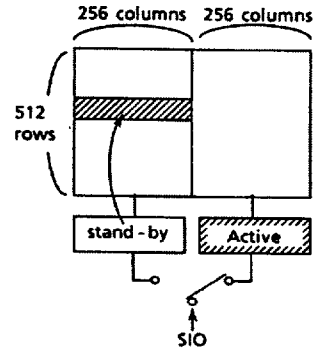


Figure 10. Block Diagram for Split Write Transfer

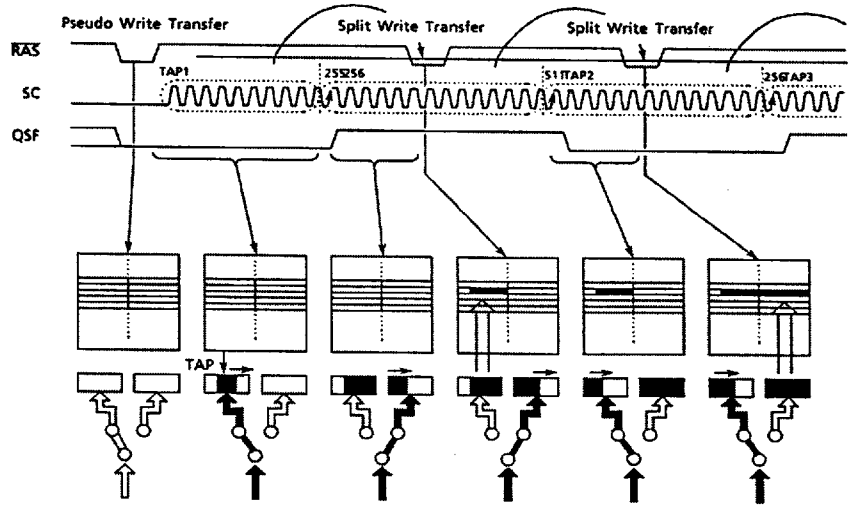
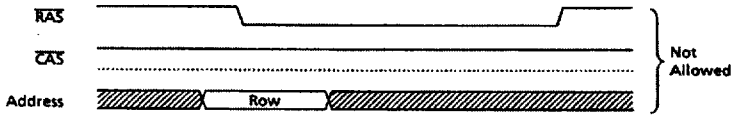


Figure 11. Example of Consecutive Write Transfer Operations

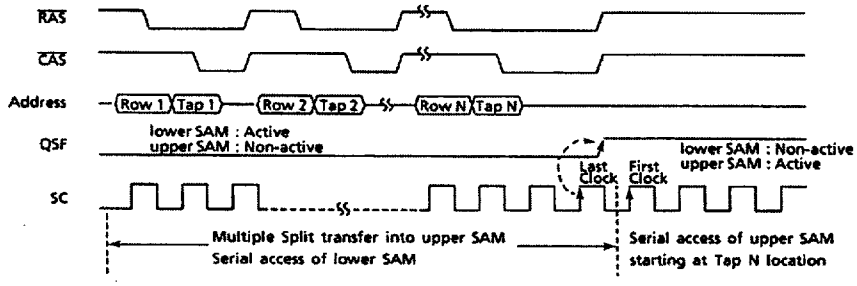
NOTES

(1) Transfer operation without $\overline{CAS}$.

The SAM tap location is undefined if $\overline{CAS}$ is maintained at a constant "high" level during a transfer cycle. A transfer cycle with $\overline{CAS}$ held "high" is, hence, not allowed.



(2) In the case of multiple split transfers performed into the same half SAM, the tap location specified during the last split transfer, before QSF toggles, will prevail, as shown below.



(3) Split transfer operation allowable period.

Figure 12 illustrates the relationship between the serial clock SC and the special function output QSF during split read / write transfers and highlights the time periods where split transfers are allowed, relative to SC and QSF. A split transfer is not allowed during to $t_{STH} + t_{STS}$. In the case that the CBRS operation is executed and the binary boundary in each half SAM is set or updated, an additional period is applied, as shown in Figure 12.

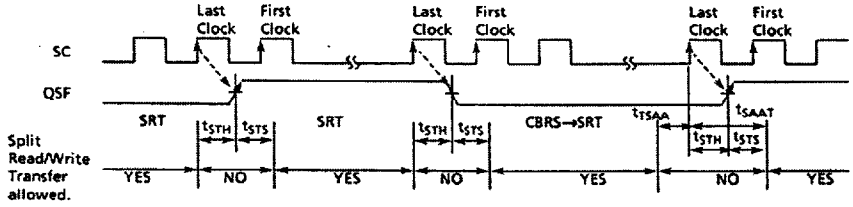
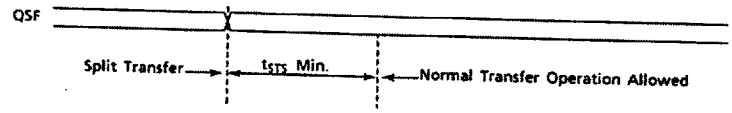


Figure 12. Split Transfer Operation Allowable Periods

The stop register and binary boundary are explained in the CBRS operation and the SAM port operation.

(4) A normal transfer (read/write) may be performed following split transfer operation provided that a t_{STS} minimun delay is satisfied after the QSF signal toggles.



(5) Binary--Boundary SET/RESET Cycle Timing

When the address counter of serial-access-memory (SAM) pointed as the last address of each boundary address, (15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255, 271, 287, 303, 319, 335, 351, 367, 383, 399, 415, 431, 447, 463, 479, 495, 511), the boundary-set or change by CBRS-cycle or the boundary-reset by CBR-cycle may cause the unexpected operation of SAM counter or QSF status.

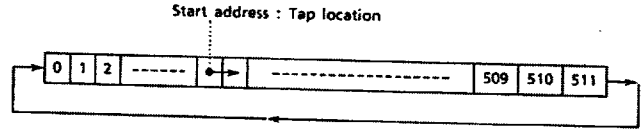
If the system design with these timing is required, please contact to our local sales office.

SAM PORT OPERATION

The TC528257 is provided with 512 words by 8-bits serial access memory (SAM) which can be operated in the single register mode or the split register mode. High speed serial read or write operations can be performed through the SAM port independent of the RAM port operation.

13. SINGLE REGISTER SERIAL READ OPERATION

Serial data can be read out of the SAM port after a read transfer has been performed. The read transfer operation changes the SAM port to the output mode. At every rising edge of the serial clock, the data is read out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit, as illustrated below. Subsequent real - time read transfer may be performed on-the-fly as many times as desired.



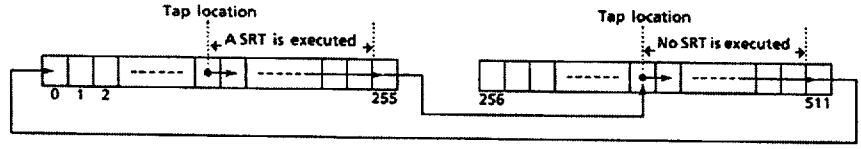
14. SINGLE REGISTER SERIAL WRITE OPERATION

During the serial write operation, the data is written into the SAM at every rising edge of the serial clock. A write transfer cycle, at which all I/Os are usually masked, must be performed to change the SAM port to the input mode. The tap location, which is the start address of the serial write, is set by the column address at the falling edge of $\overline{CAS}$. After the data is filled in the SAM, the serial clock must stop toggling and a write transfer cycle is subsequently used to load the SAM data into the RAM selected by the row address at the falling edge of $\overline{RAS}$. The tap address is set during the same cycle for the next serial write opration.

15. SPLIT REGISTER MODE

The split register mode realizes continuous serial read or write operation. The data can be shifted into or out of one half of the SAM while a split read or write transfer is being performed on the other half of the SAM. Thus, the tight timing control at a real time read operation is eliminated with the split read operation. A normal read / write transfer operation must precede any split read/write transfer operation in order to set the SAM port into output mode or input mode, as the split read or write transfer operations will not change the SAM port mode. Also, a $\overline{CAS}$ before $\overline{RAS}$ refresh and stop register set cycle (CBRS) can be performed to specify the binary boundaries in the SAM.

In the split register mode, serial data can be read from or written into one of the split registers starting from any of the 256 tap locations. The data is read or written sequentially from the tap location to the most significant bit (255 or 511) of the first split SAM and then the SAM pointer moves to the tap location selected for the second split SAM to read or write the data sequentially to the most significant bit (255 or 511) and finally wraps around to the least significant bit, as illustrated in the example below.



16. SPLIT REGISTER MODE WITH BINARY BOUNDARY

After a CBRS cycle is performed, the binary boundary, which is stated in 8.3. $\overline{CAS}$ before $\overline{RAS}$ refresh and stop register set, is set when a SRT cycle is performed. The serial data is read from or written into one half of the SAM starting the tap location to the next binary boundary, while another SRT cycle is performed. Than, the SAM pointer moves to the tap location in the other half SAM and the data is read from or written into the half SAM sequentially. If any SRT operation is not performed before the next boundary, the SAM pointer does not jump to the other half SAM, as illustrated in Figure 12.

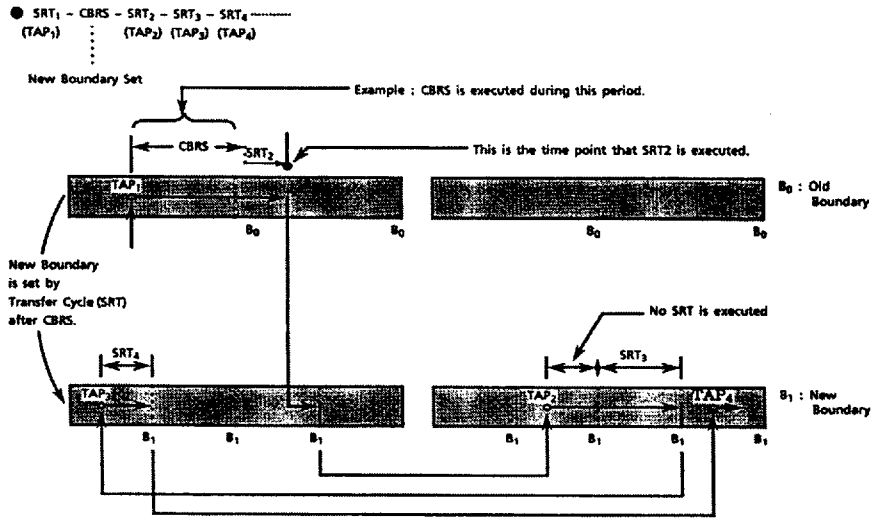


Figure 12. Operation of Split Register Mode with Binary Boundary

The binary boundary is reset by a CBR cycle and the SAM operation mode returns to the normal split register mode, as shown in Figure 13.

Fig. 14 shows the relation between CBR and SC on binary-boundary-reset. When Nth SC clock accesses old binary address is reset and (N + 1)th SC clock accesses old boundary address (old stop address) + 1 on the same split SAM, not jump to TAP address.

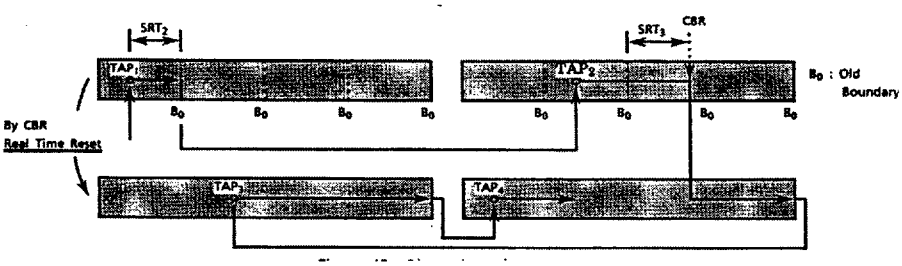


Figure 13. Binary Boundary Reset

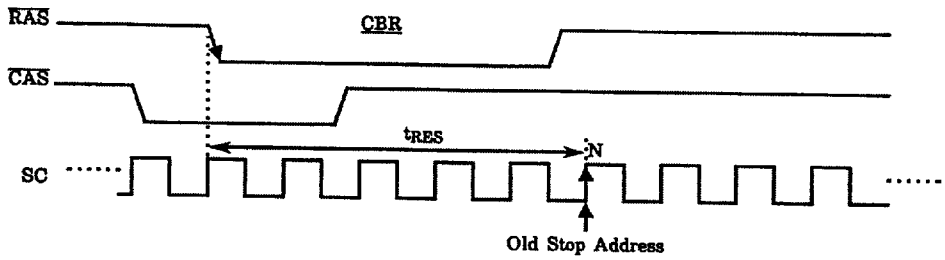


Figure 14. CBR and SC relation of binary-boundary-reset

In an actual system which uses the binary boundary a CBRS cycle is executed to determine a type of the boundary location. Then, a normal RT transfers a row of data into the SAM and set the initial tap location at the same time. An SRT cycle follows it before the SAM pointer reaches to the boundary location. The SRT cycle makes the binary boundary jump effective, as illustrated in Figure 15.

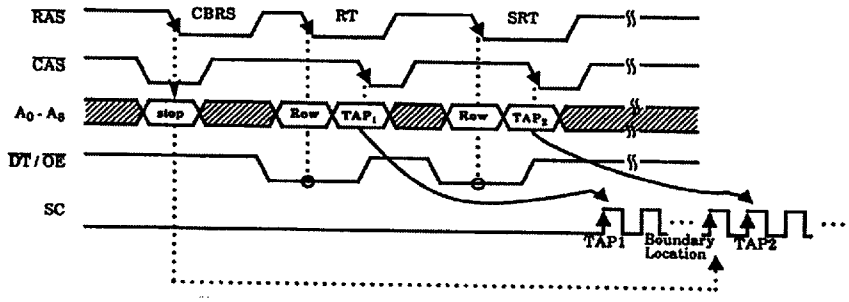


Figure 15. Binary Boundary Jump Set Sequence

There are additional timing specifications, t_{TSAA} and t_{SAAT} to determine the period that does not allow a split transfer, as illustrated in Figure 16.

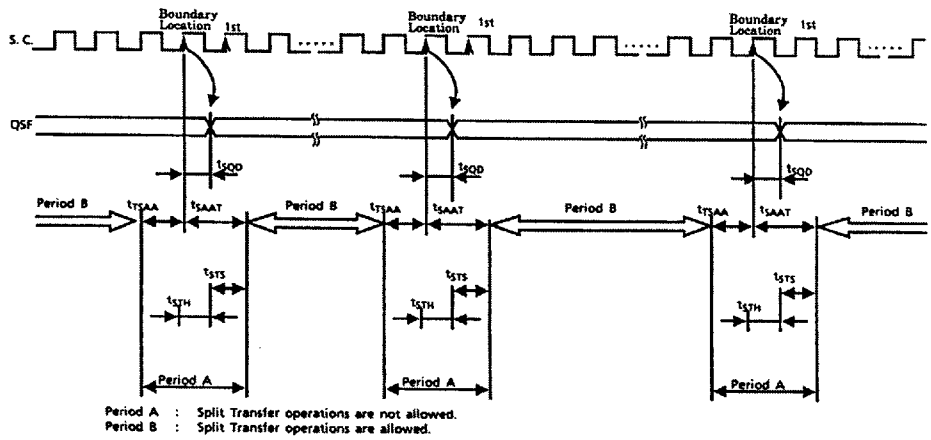


Figure 16. Timing Specification to allow SRT operation

POWER-UP

Power must be applied to the $\overline{RAS}$ and $\overline{DT/OE}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200 μseconds minimum is required with $\overline{RAS}$ and $\overline{DT/OE}$ held "high". After the pause, a minimum of 8 CBR dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT/OE}$ signal must be held "high".

INITIAL STATE AFTER POWER-UP

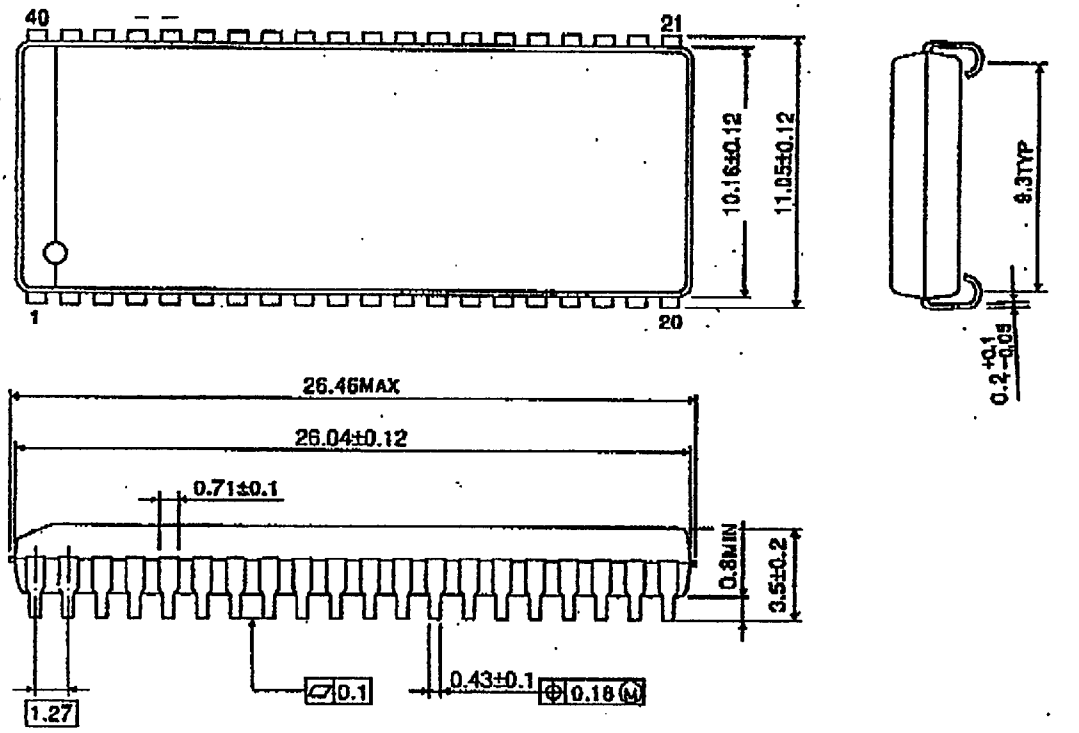
When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT/OE}$ and $\overline{WB/WE}$ held "high", the internal state of the TC528257 is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 μseconds pause followed by a minimum of 8 CBR cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
QSF	High-Impedance
Color Register	all "0"
Write Mask Register	Write Enable
TAP pointer	Invalid
Sto Register	Default Case

OUTLINE DRAWING (SOJ40-P-400)

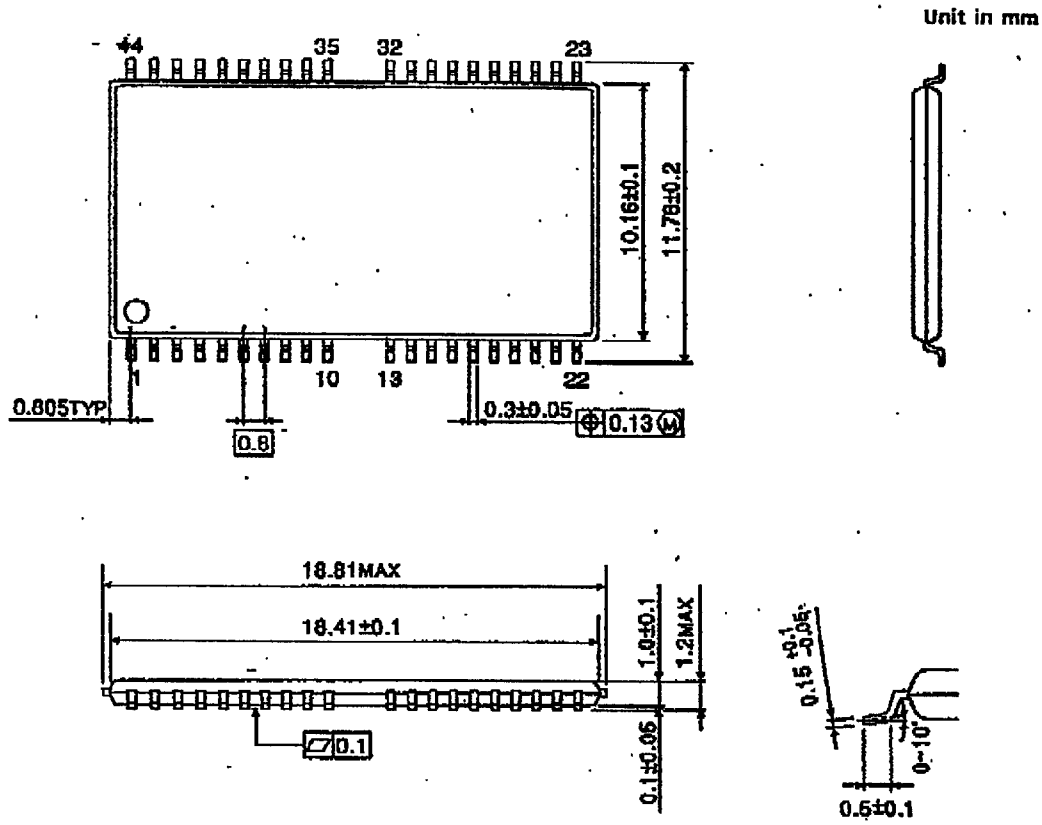
Unit in mm



Weight : 1.55g (TYP.)

OUTLINE DRAWING (TSOP44-P-400B)

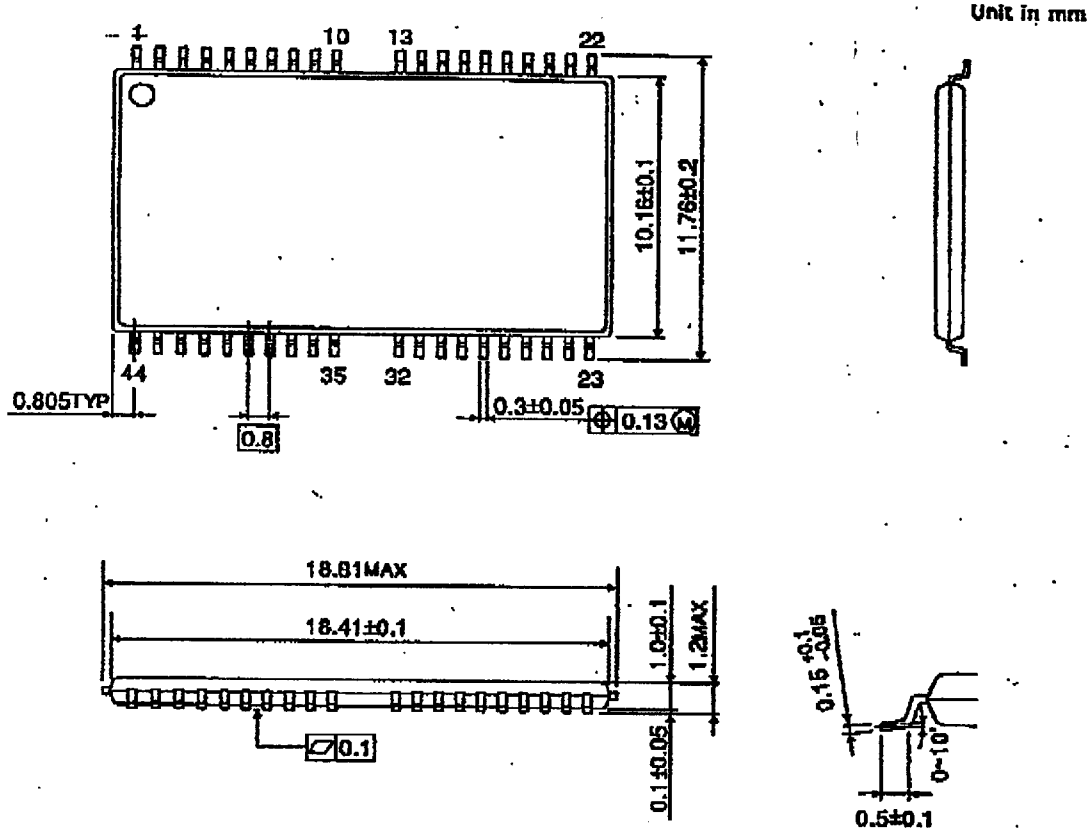
Unit in mm



Weight : 0.48g (TYP.)

OUTLINE DRAWING (TSOP44-P-400C)

Unit in mm



Weight : 0.48g (TYP.)