IS61LV256

32K x 8 LOW VOLTAGE CMOS STATIC RAM

FEBRUARY 1996

FEATURES

- High-speed access time: 12, 15, 20, 25 ns
- Automatic power-down when chip is deselected
- CMOS low power operation
  - — 345 mW (max.) operating
  - — 7 mW (max.) CMOS standby
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three-state outputs

DESCRIPTION

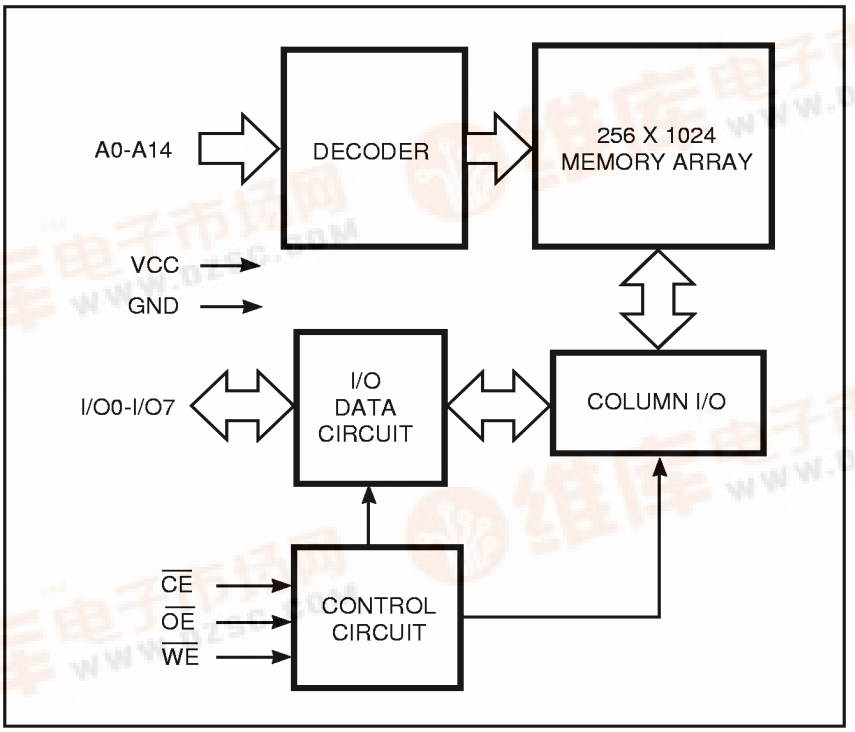
The *ISSI* IS61LV256 is a very high-speed, low power, 32,768-word by 8-bit static RAM. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 12 ns maximum.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation is reduced to 50 µW (typical) with CMOS input levels.

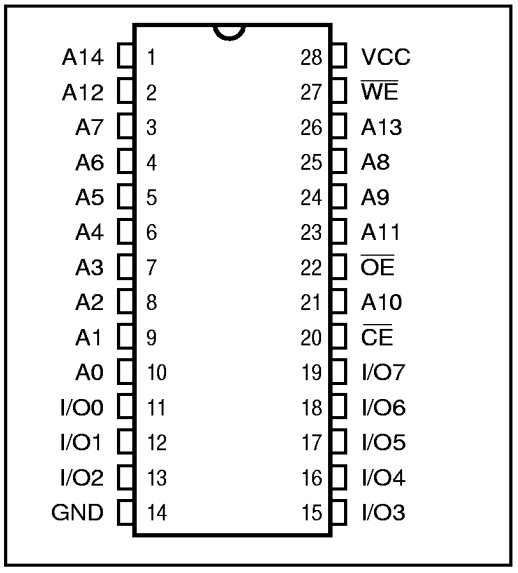
Easy memory expansion is provided by using an active LOW Chip Enable ($\overline{CE}$). The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS61LV256 is available in the JEDEC standard 28-pin, 300-mil DIP and SOJ, plus the 450-mil TSOP package.

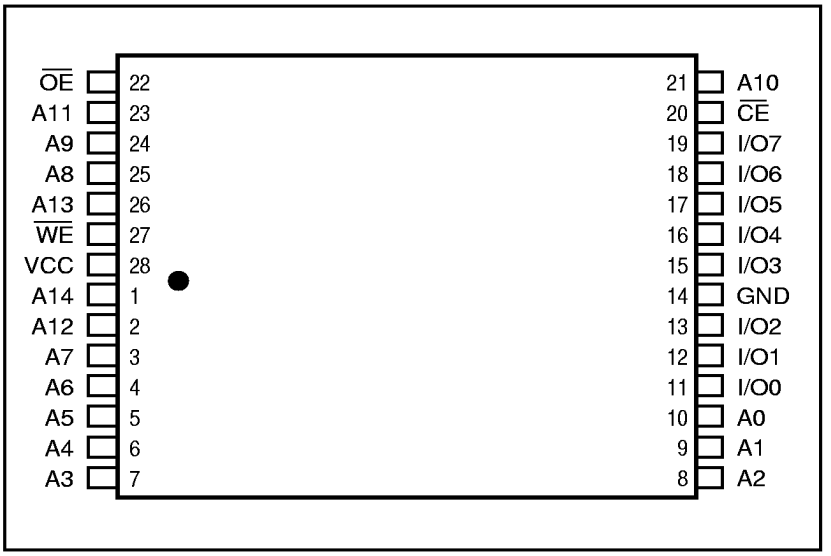
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
28-Pin DIP and SOJ



PIN CONFIGURATION
28-Pin TSOP



PIN DESCRIPTIONS

A0-A14	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	3.3V +10%, –5%
Industrial	–40°C to +85°C	3.3V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	Com. Ind.	–2 –5	2 5	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	Com. Ind.	–2 –5	2 5	µA

Notes:
1. V_{IL} = –3.0V for pulse width less than 10 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

				-12 ns		-15 ns		-20 ns		-25 ns		
Symbol	Parameter	Test Conditions		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
I_{CC1}	Vcc Operating Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = 0	Com. Ind.	— —	50 —	— —	50 60	— —	50 60	— —	50 60	mA
I_{CC2}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	— —	100 —	— —	90 100	— —	80 90	— —	70 80	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ ≥ V_{IH}, f = 0	Com. Ind.	— —	10 —	— —	10 20	— —	10 20	— —	10 20	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE}$ ≤ V_{CC} – 0.2V, V_{IN} > V_{CC} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com. Ind.	— —	2 —	— —	2 5	— —	2 5	— —	2 5	mA

Notes:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 3.3V.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-12 ns Min.	-12 ns Max.	-15 ns Min.	-15 ns Max.	-20 ns Min.	-20 ns Max.	-25 ns Min.	-25 ns Max.	Unit
t_{RC}	Read Cycle Time	12	—	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	—	25	ns
t_{OHA}	Output Hold Time	2	—	2	—	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	12	—	15	—	20	—	25	ns
t_{DOE}	$\overline{OE}$ Access Time	—	6	—	7	—	8	—	9	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	7	—	8	—	9	—	10	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	—	5	—	6	—	9	—	10	ns
t_{PU}[3]	$\overline{CE}$ to Power-Up	0	—	0	—	0	—	0	—	ns
t_{PD}[3]	$\overline{CE}$ to Power-Down	—	13	—	15	—	18	—	20	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1a and 1b

AC TEST LOADS

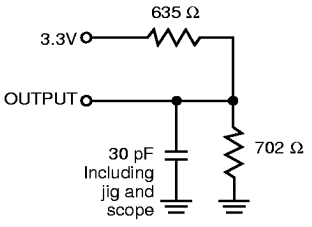


Figure 1a.

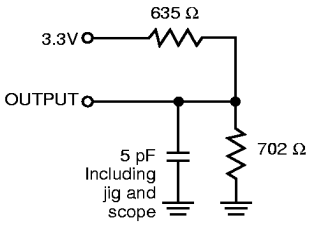
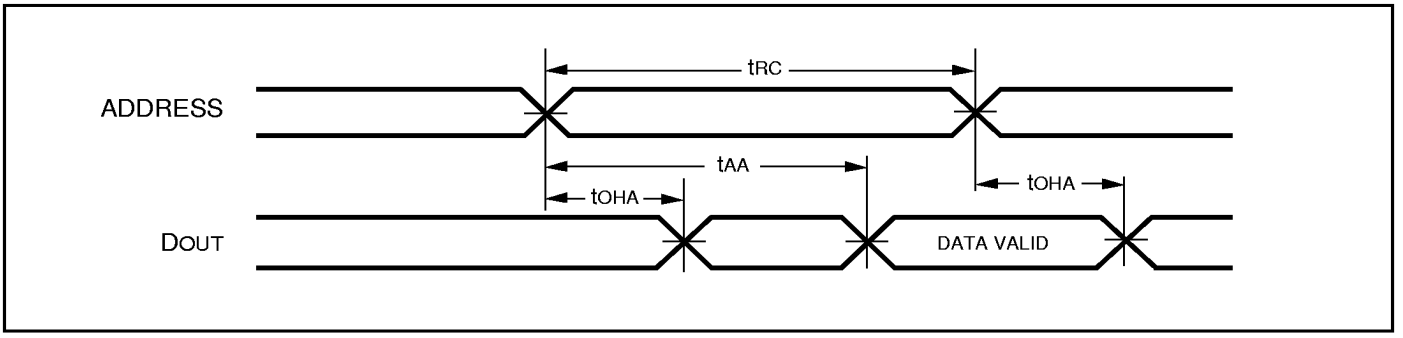


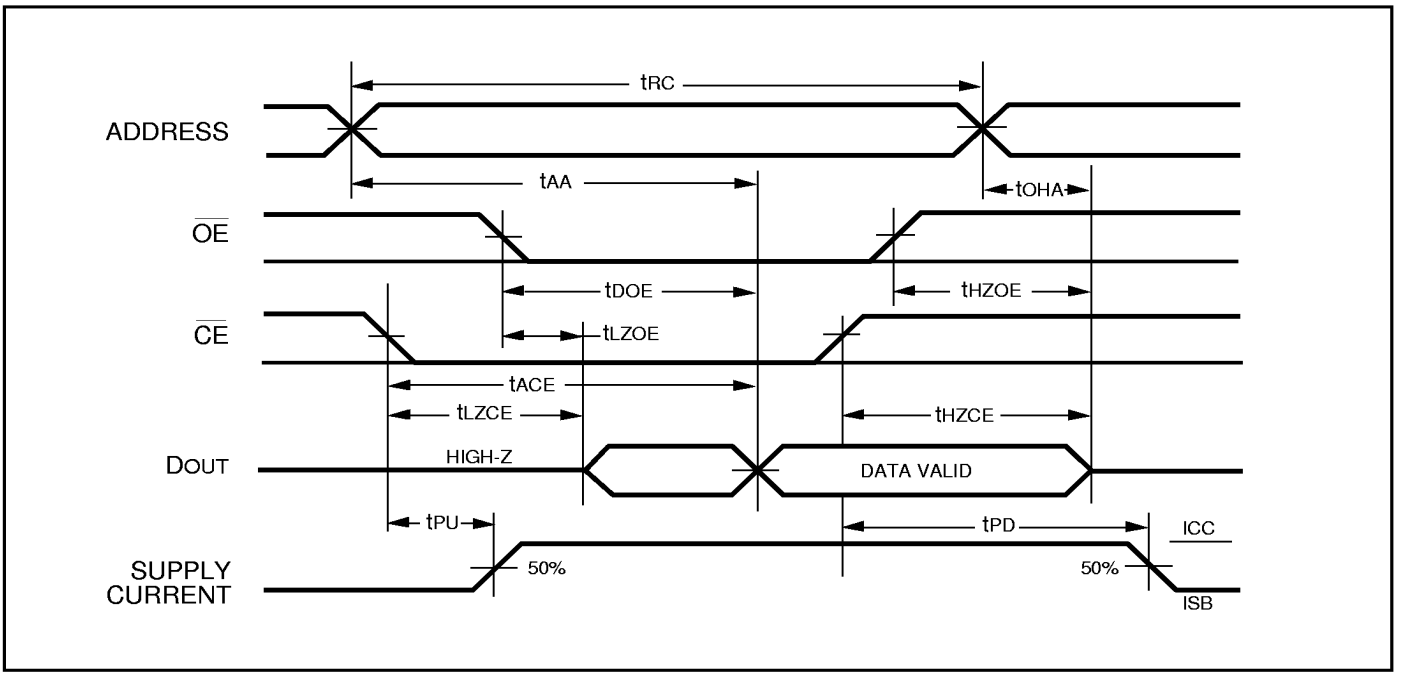
Figure 1b.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

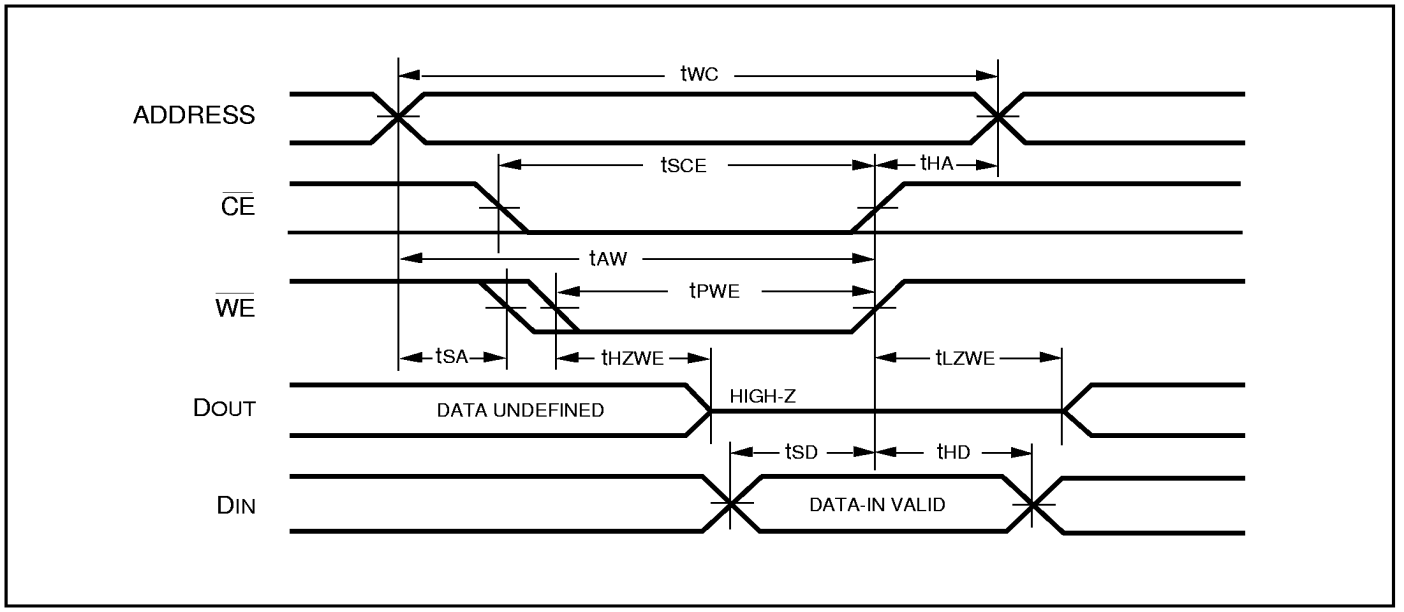
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-12 ns Min.	-12 ns Max.	-15 ns Min.	-15 ns Max.	-20 ns Min.	-20 ns Max.	-25 ns Min.	-25 ns Max.	Unit
t_{WC}	Write Cycle Time	12	—	15	—	20	—	25	—	ns
t_{SCE}	$\overline{CE}$ to Write End	8	—	10	—	13	—	15	—	ns
t_{AW}	Address Setup Time to Write End	8	—	10	—	15	—	20	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	8	—	10	—	13	—	15	—	ns
t_{SD}	Data Setup to Write End	6	—	8	—	10	—	12	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	6	—	7	—	8	—	10	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	0	—	0	—	ns

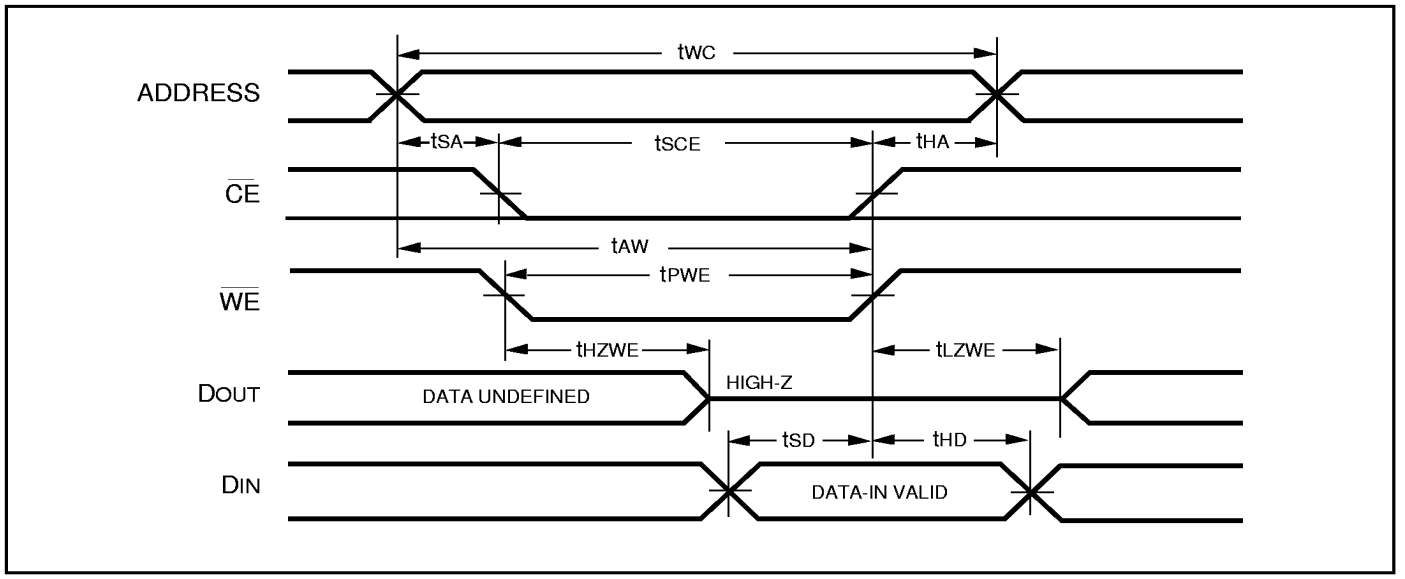
Notes:
1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with $\overline{OE}$ HIGH.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



WRITE CYCLE NO. 2 ($\overline{CE}$ Controlled)[1,2]



Notes:
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
12	IS61LV256-12N	300-mil Plastic DIP
12	IS61LV256-12T	TSOP - 450 mil
12	IS61LV256-12J	300-mil Plastic SOJ
15	IS61LV256-15N	300-mil Plastic DIP
15	IS61LV256-15T	450-mil TSOP
15	IS61LV256-15J	300-mil Plastic SOJ
20	IS61LV256-20N	300-mil Plastic DIP
20	IS61LV256-20T	450-mil TSOP
20	IS61LV256-20J	300-mil Plastic SOJ
25	IS61LV256-25N	300-mil Plastic DIP
25	IS61LV256-25T	450-mil TSOP
25	IS61LV256-25J	300-mil Plastic SOJ

ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
12	IS61LV256-12NI	300-mil Plastic DIP
12	IS61LV256-12TI	TSOP - 450 mil
12	IS61LV256-12JI	300-mil Plastic SOJ
15	IS61LV256-15NI	300-mil Plastic DIP
15	IS61LV256-15TI	450-mil TSOP
15	IS61LV256-15JI	300-mil Plastic SOJ
20	IS61LV256-20NI	300-mil Plastic DIP
20	IS61LV256-20TI	450-mil TSOP
20	IS61LV256-20JI	300-mil Plastic SOJ
25	IS61LV256-25NI	300-mil Plastic DIP
25	IS61LV256-25TI	450-mil TSOP
25	IS61LV256-25JI	300-mil Plastic SOJ