

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4538B

MSI

Dual precision monostable multivibrator

Product specification
File under Integrated Circuits, IC04

January 1995

Dual precision monostable multivibrator

HEF4538B MSI

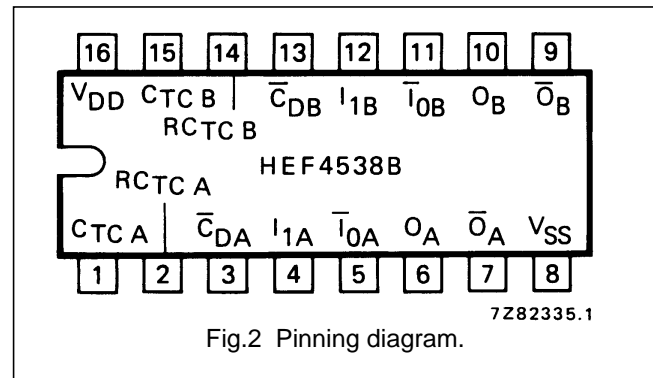
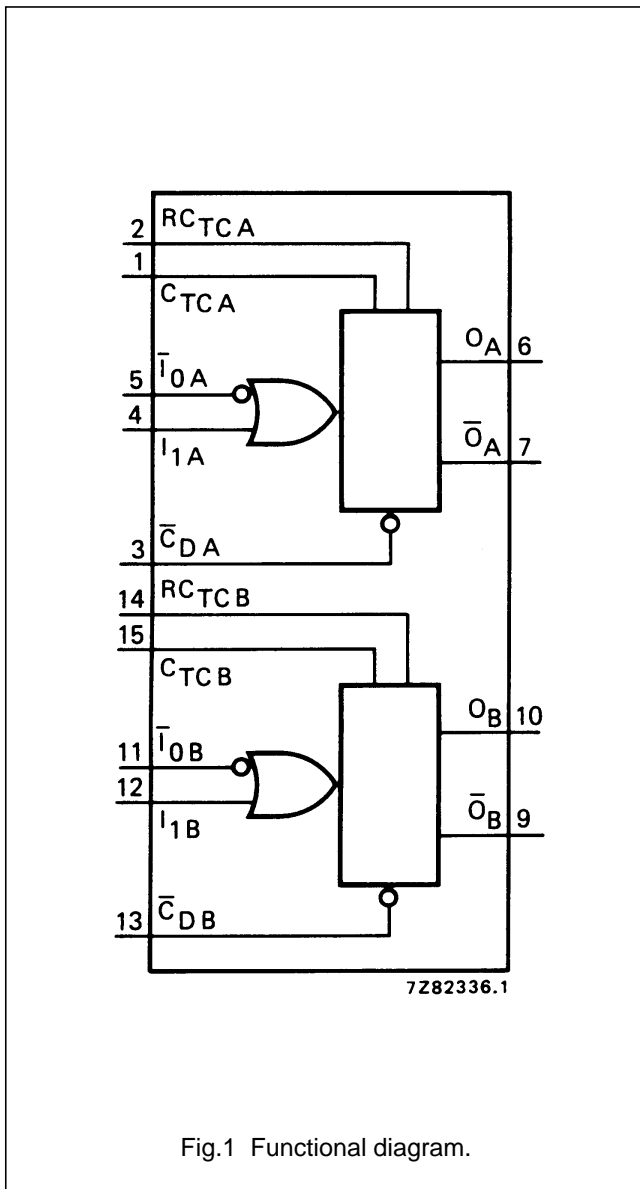
DESCRIPTION

The HEF4538B is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has an active LOW trigger/retrigger input (\bar{I}_0), an active HIGH trigger/retrigger input (I_1), an overriding active LOW direct reset input (\bar{C}_D), an output (O) and its complement (\bar{O}), and two pins (C_{TC} ,⁽¹⁾ R_{TC}) for connecting the external timing components C_t and R_t . Typical pulse width variation over temperature range is $\pm 0,2\%$.

The HEF4538B may be triggered by either the positive or the negative edges of the input pulse and will produce an

accurate output pulse with a pulse width range of 10 μ s to infinity. The duration and accuracy of the output pulse are determined by the external timing components C_t and R_t . The output pulse width (T) is equal to $R_t \times C_t$. The linear design techniques in LOC MOS guarantee precise control of the output pulse width.

A LOW level at \bar{C}_D terminates the output pulse immediately. Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.



- HEF4538BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4538BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4538BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

- $\bar{I}_{0A}, \bar{I}_{0B}$ input (HIGH to LOW triggered)
- I_{1A}, I_{1B} input (LOW to HIGH triggered)
- $\bar{C}_{DA}, \bar{C}_{DB}$ direct reset input (active LOW)
- O_A, O_B output
- \bar{O}_A, \bar{O}_B complementary output (active LOW)
- $C_{TC A}, C_{TC B}$ external capacitor connections⁽¹⁾
- $R_{TC A}, R_{TC B}$ external capacitor/ resistor connections

Note

1. Always connected to ground.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family specifications.

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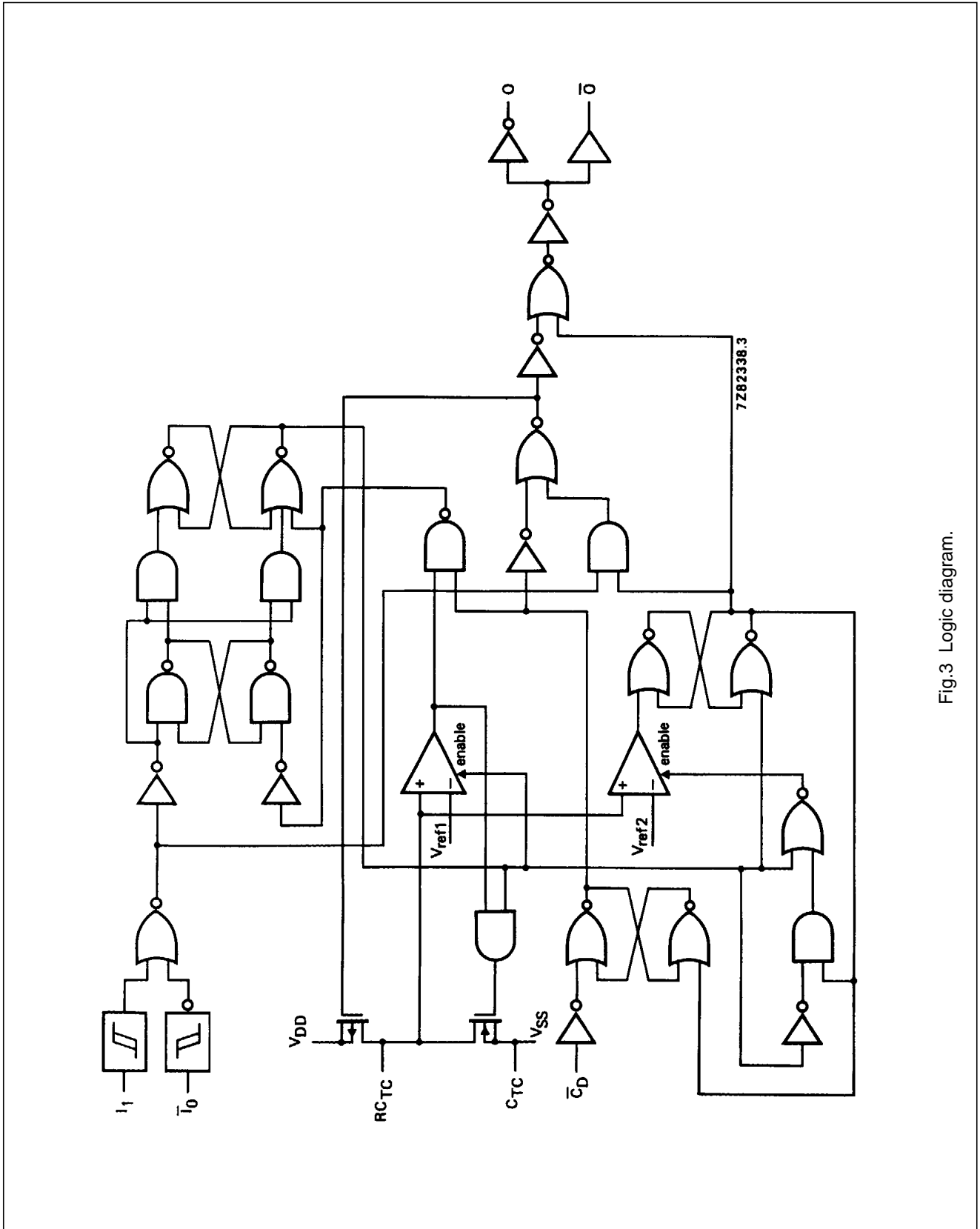


Fig.3 Logic diagram.

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FUNCTION TABLE

INPUTS			OUTPUTS	
\bar{I}_0	I_1	\bar{C}_D	O	\bar{O}
\searrow	L	H	\sqcap	\sqcup
H	\swarrow	H	\sqcap	\sqcup
X	X	L	L	H

Notes

- 1. H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial
- \sqcap = positive output pulse
- \sqcup = negative output pulse
- \swarrow = positive-going transition
- \searrow = negative-going transition

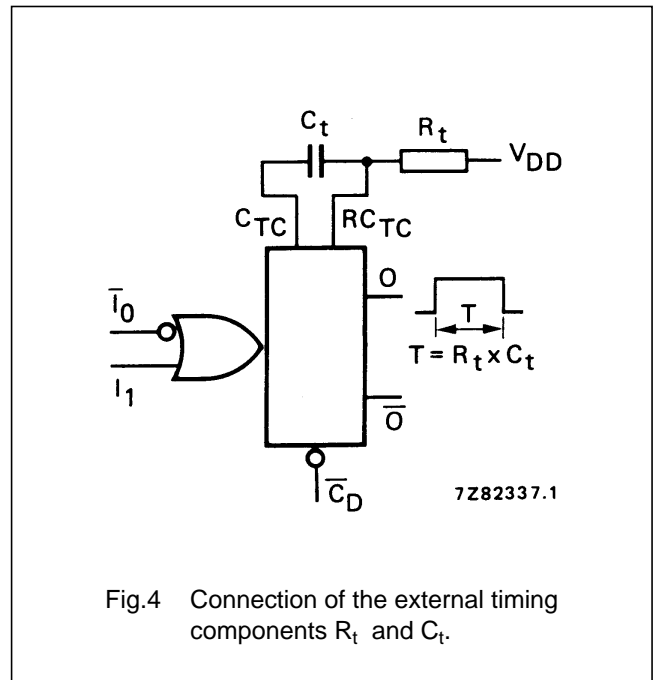


Fig.4 Connection of the external timing components R_t and C_t .

DC CHARACTERISTICS

$V_{SS} = 0\text{ V}$

	V_{DD} V	SYMBOL	$T_{amb} (\text{°C})$					
			- 40		+ 25		+ 85	
			TYP.	MAX.	TYP.	MAX.	TYP.	MAX.
Supply current	5							
active state	10	I_D			55			μA
(see note)	15				150			μA
Input leakage					220			μA
current	15	$\pm I_{IN}$			300		1000	nA
(pins 2 and 14)								

Note

- 1. Only one monostable is switching: current present during output pulse (output O is HIGH).

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AC CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays	$\bar{I}_0, I_1 \rightarrow O$ HIGH to LOW	t_{PHL}		200	460 ns	$173 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
				90	180 ns	$79 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
				60	120 ns	$52 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	$\bar{I}_0, I_1 \rightarrow \bar{O}$ LOW to HIGH	t_{PLH}		220	440 ns	$193 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
				85	190 ns	$74 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
				60	120 ns	$52 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
	$\bar{C}_D \rightarrow O$ HIGH to LOW	t_{PHL}		125	250 ns	$98 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
				55	110 ns	$44 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
				40	80 ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
$\bar{C}_D \rightarrow \bar{O}$ LOW to HIGH	t_{PLH}		125	250 ns	$98 \text{ ns} + (0,55 \text{ ns/pF}) C_L$	
			55	110 ns	$44 \text{ ns} + (0,23 \text{ ns/pF}) C_L$	
			40	80 ns	$32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$	
Recovery times $\bar{C}_D \rightarrow \bar{I}_0, I_1$	t_{RCD}			20	40 ns	
				10	20 ns	
				5	10 ns	
Retrigger times $O, \bar{O} \rightarrow \bar{I}_0, I_1$	t_{RO}		0		ns	
			0		ns	
			0		ns	
Minimum \bar{I}_0 pulse width; LOW	t_{WI0L}		90	45	ns	
			30	15	ns	
			24	12	ns	
Minimum I_1 pulse width; HIGH	t_{WI1H}		50	25	ns	
			24	12	ns	
			20	10	ns	
Minimum \bar{C}_D pulse width; LOW	$t_{WC DL}$		55	25	ns	
			25	12	ns	
			20	10	ns	
Output O or \bar{O} pulse width	t_{WO}		218	230	242 μ s	$R_t = 100 \text{ k}\Omega$ $C_t = 0,002 \text{ }\mu\text{F}$
			213	224	235 μ s	
			211	223	234 μ s	
Output O or \bar{O} pulse width	t_{WO}		10,3	10,8	11,3 ms	$R_t = 100 \text{ k}\Omega$ $C_t = 0,1 \text{ }\mu\text{F}$
			10,2	10,7	11,2 ms	
			10,1	10,6	11,1 ms	
Output O or \bar{O} pulse width	t_{WO}		1,01	1,09	1,11 s	$R_t = 100 \text{ k}\Omega$ $C_t = 10 \text{ }\mu\text{F}$
			0,99	1,04	1,09 s	
			0,99	1,04	1,09 s	

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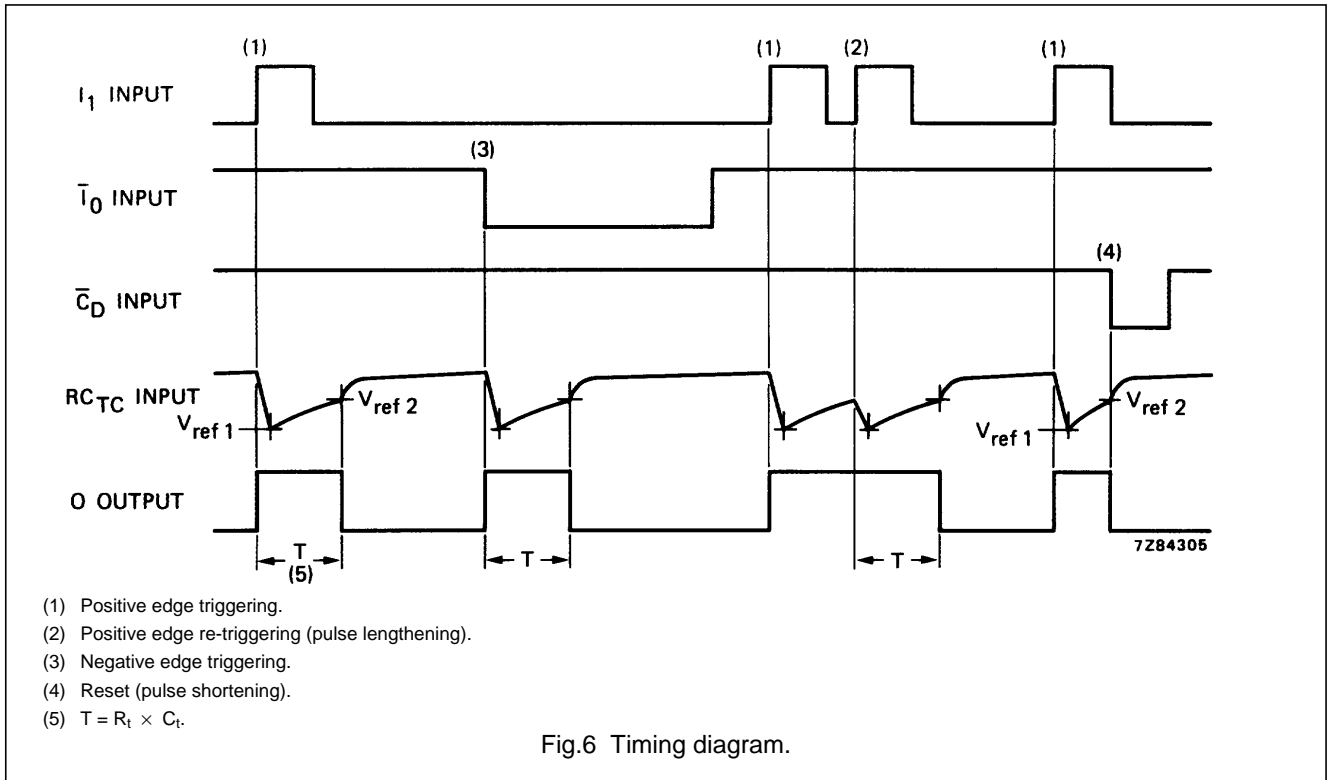
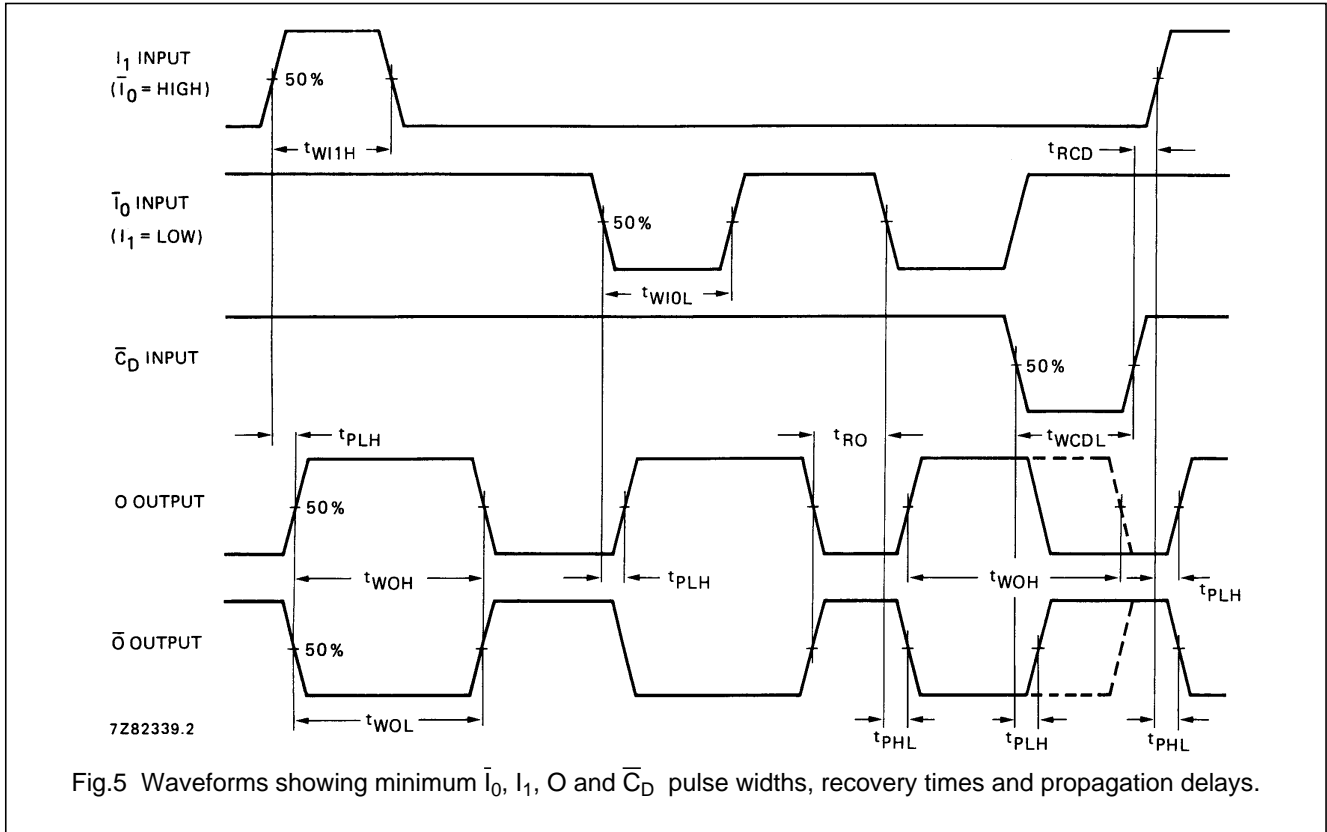
	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Change in output O pulse width over temperature (T_{amb})	5	Δt_{WO}		$\pm 0,2$		%
	10			$\pm 0,2$		%
	15			$\pm 0,2$		%
Change in output O pulse width over V_{DD} range 5 to 15 V		Δt_{WO}		$\pm 1,5$		%
Pulse width variation between circuits in same package	5	Δt_{WO}		± 1		%
	10			± 1		%
	15			± 1		%
External timing resistor		R_t	5	–	(1)	k Ω
External timing capacitor		C_t	2000	–	no limits	pF
Input capacitance (pin 2 or 14)		C_{IN}		15		pF

Note

1. The maximum permissible resistance R_t , which holds the specified accuracy of t_{WO} , depends on the leakage current of the capacitor C_t and the leakage of the HEF4538B.

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