

System Reset Monolithic IC PST600

Outline

This IC operates in a variety of CPU systems and other logic systems by detecting power supply voltage, so that the system can be reset accurately when power is turned on or when power is momentarily cut. PST572 and others perform the same function as does this series, but this IC is a low reset type system resetting IC which follows load current so that circuit current flow increases for ON, and has low current consumption for both ON and OFF.

Features

1. Follows load current so that circuit current flow increases for ON, and has low current consumption for both ON and OFF.
2. Low operating limit voltage
3. Hysteresis voltage provided in detection voltage
4. The following 10 ranks of detection voltages are available.

No load : $I_{OCL}=7\mu A$ typ.; $I_{OCH}=5\mu A$ typ.

0.65V typ.

50mV typ.

PST600 C : 4.5V typ. H : 3.1V typ.

D : 4.2V typ. I : 2.9V typ.

E : 3.9V typ. J : 2.7V typ.

F : 3.6V typ. K : 2.5V typ.

G : 3.3V typ. L : 2.3V typ.

Package

MMP-3A (PST600□M)

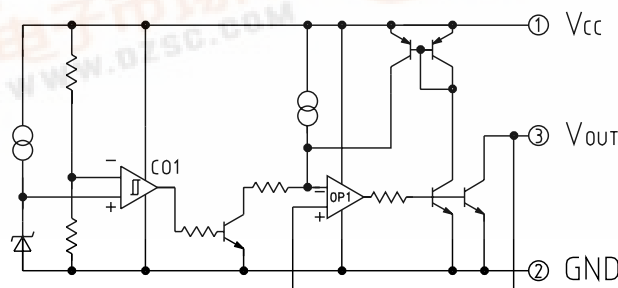
TO-92A (PST600□)

*□ contains detection voltage rank.

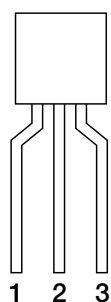
Applications

1. Microcomputers, CPU, MPU reset circuits
2. Logic circuit reset circuits
3. Battery voltage check circuits
4. Back-up power supply switching circuits
5. Level detection circuits

Equivalent Circuit

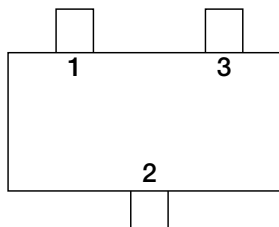


Pin Assignment



TO-92A

1	V _{CC}
2	GND
3	V _{OUT}



MMP-3A
(TOP VIEW)

1	V _{CC}
2	GND
3	V _{OUT}

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T _{STG}	-40~+125	°C
Operating temperature	T _{OPR}	-20~+75	°C
Power supply voltage	V _{CC} max.	-0.3~10	V
Allowable loss	P _d	200 (MMP-3A) 300 (TO-92A)	mW

Electrical Characteristics (Ta=25°C) (unless otherwise indicated resistance unit is Ω)

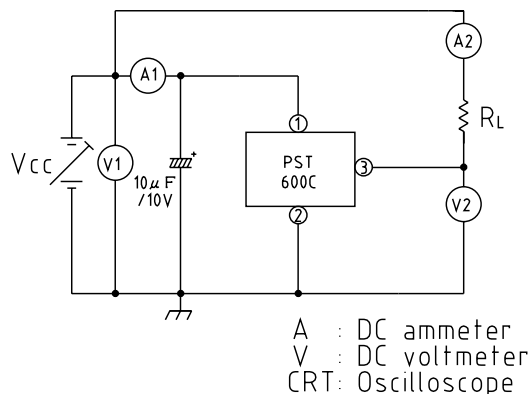
Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units
Detection voltage	V _S	1	R _L =470 V _{OL} ≤ 0.4V V _{CC} =H→L	PST600C	4.3	4.5	4.7
				PST600D	4.0	4.2	4.4
				PST600E	3.7	3.9	4.1
				PST600F	3.4	3.6	3.8
				PST600G	3.1	3.3	3.5
				PST600H	2.9	3.1	3.3
				PST600I	2.75	2.90	3.05
				PST600J	2.55	2.70	2.85
				PST600K	2.35	2.50	2.65
				PST600L	2.15	2.30	2.45
Hysteresis voltage	ΔV _S	1	R _L =470, V _{CC} =L→H→L	30	50	100	mV
Detection voltage temperature coefficient	V _S /ΔT	1	R _L =470, Ta=-20°C~+75°C		±0.01		%/°C
Low level output voltage	V _{OL}	1	V _{CC} =V _S min. -0.05V, R _L =470		0.3	0.4	V
Output leak current	I _{OH}	1	V _{CC} =10V			±0.1	μA
Circuit current for ON	I _{CC} L	1	V _{CC} =V _S min. -0.05V	I _{OL} =0mA	7	14	μA
				I _{OL} =8mA	50	130	
Circuit current for OFF	I _{CC} H	1	V _{CC} =V _S typ./0.85V, R _L =∞		5	10	μA
H transmission delay time	t _{PLH}	2	R _L =4.7k, C _L =100pF *1	20	40	80	μs
L transmission delay time	t _{PHL}	2	R _L =4.7k, C _L =100pF *1	10	20	40	μs
Operating limit voltage	V _{op} L	1	R _L =4.7k, V _{OL} ≤ 0.4V		0.65	0.85	V
Output current 1 for ON	I _{OL} 1	1	V _{CC} =V _S min. -0.05V, R _L =0	8			mA
Output current 2 for ON	I _{OL} 2	1	Ta=-20°C~+75°C, R _L =0 *2	6			mA

*1 t_{PLH} : V_{CC}= (V_S typ. -0.4V) → (V_S typ.+0.4V), t_{PLH} : V_{CC}= (V_S typ.+0.4V) → (V_S typ.-0.4V)

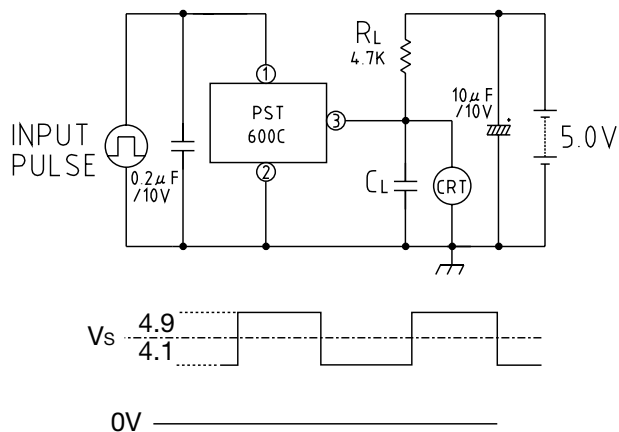
*2 V_{CC}=V_S min. -0.15V

Measurement Circuit

[1]



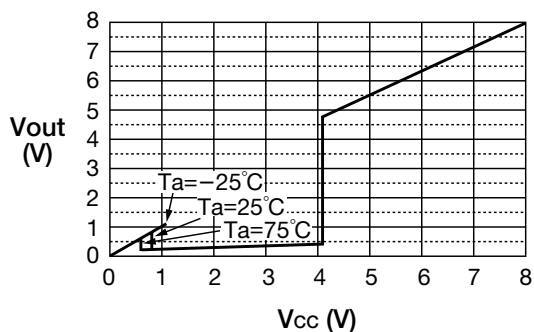
[2]



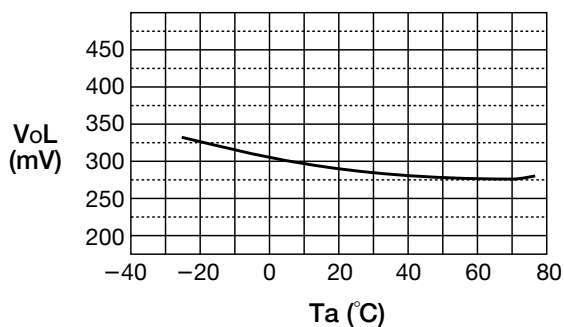
* The input model is an example of PST600C (MMP-3P).

Characteristics (PST600C is used as the representative model for characteristics examples.)

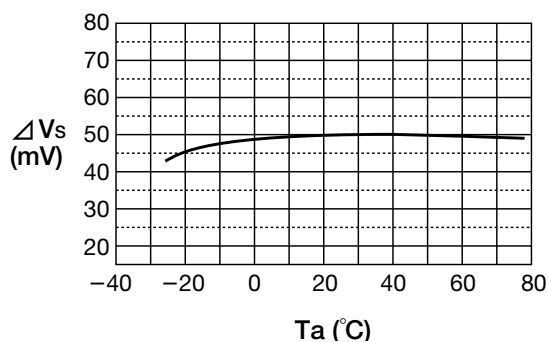
Vcc vs. Vout



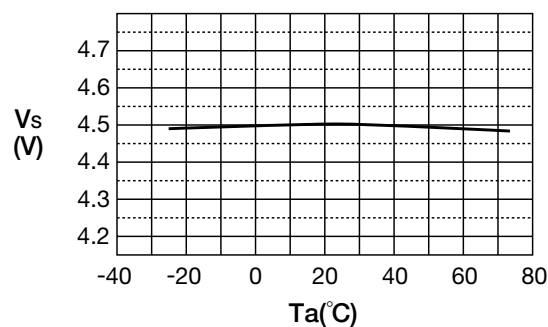
Vol vs. Ta



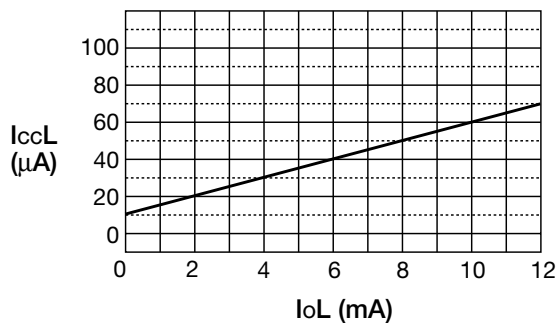
ΔVs vs. Ta



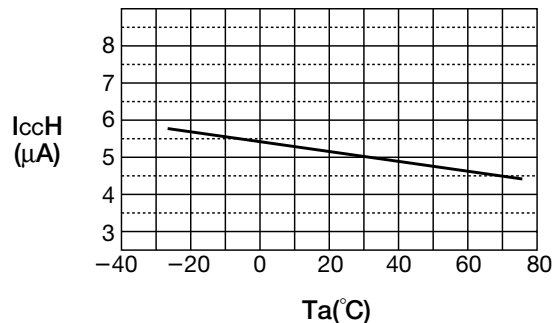
Vs vs. Ta



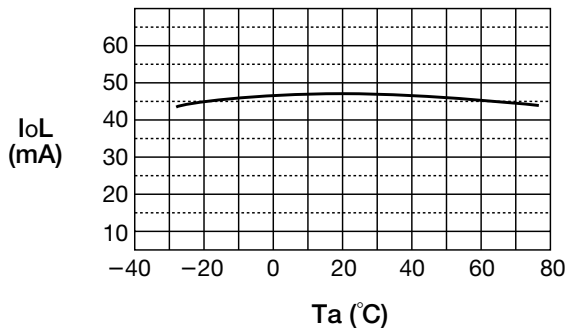
IccL vs. IoL



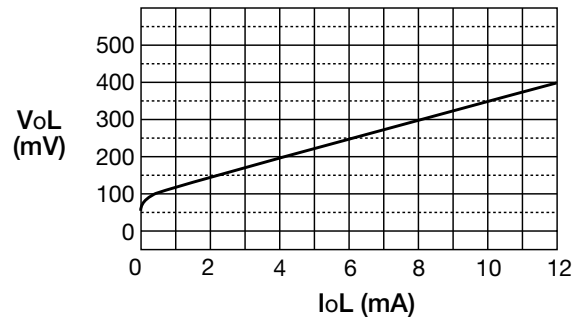
IccH vs. Ta



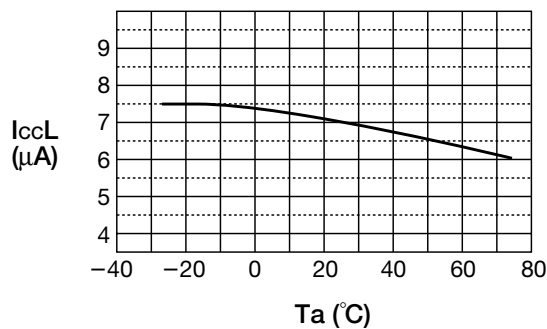
■ I_{oL} vs. T_a



■ V_{oL} vs. I_{oL}

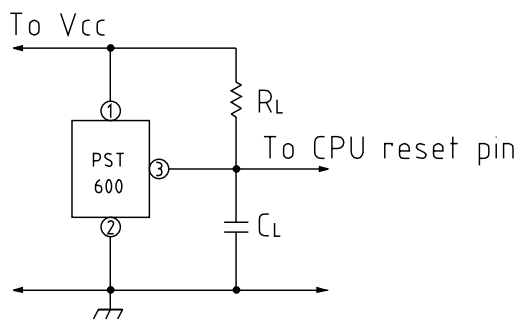


■ I_{ccL} ($I_{oL}=0\text{mA}$) vs. T_a



Application Circuits

1. Normal hard reset



Delay Time (t_{PLH})

$$\approx C_L \times R_L \times \left[\ln \frac{V_{CC}}{V_{CC} - (V_{S_{CPU}} + 0.2)} \right] + 0.040 \text{ (ms)}$$

C_L : μF

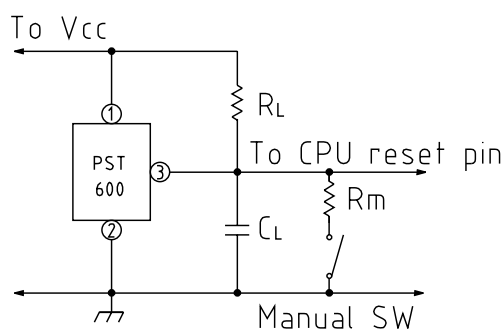
$V_{S_{CPU}}$: CPU, MPU reset threshold voltage

R_L : $\text{k}\Omega$

Voltage : V

Note : When V_{CC} line impedance is high, connect a capacitor between IC Pins 1 and 2.

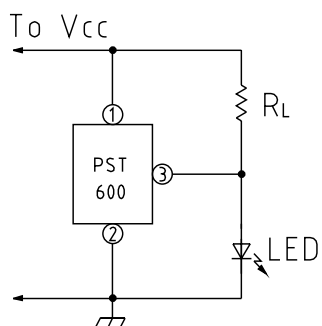
2. Manual Reset



Note : Prevent Manual SW chattering by using R_L , C_L and R_m . R_m setting conditions are as follows :
 $R_m \leq 1/20 R_L$

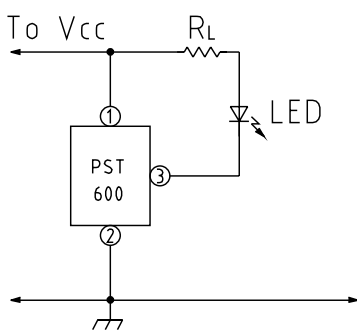
Note : When V_{CC} line impedance is high, connect a capacitor between IC Pins 1 and 2.

3. Battery Checker (LED ON for High voltage)



Note : When V_{CC} line impedance is high, connect a capacitor between IC Pins 1 and 2.

4. Battery Checker (LED ON for Low voltage)



Note : When V_{CC} line impedance is high, connect a capacitor between IC Pins 1 and 2.