SHARP

SPEC No. EL068106
ISSUE: Aug. 31. 1994

To ;

SPECIFICATIONS

Product Type 100 Output LCD Common Driver

Model No. LH1513AF

※This tentative specifications contains 17 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

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SHARP CORPORATION IC GROUP 2.17'95 MAIL DATE

Contents

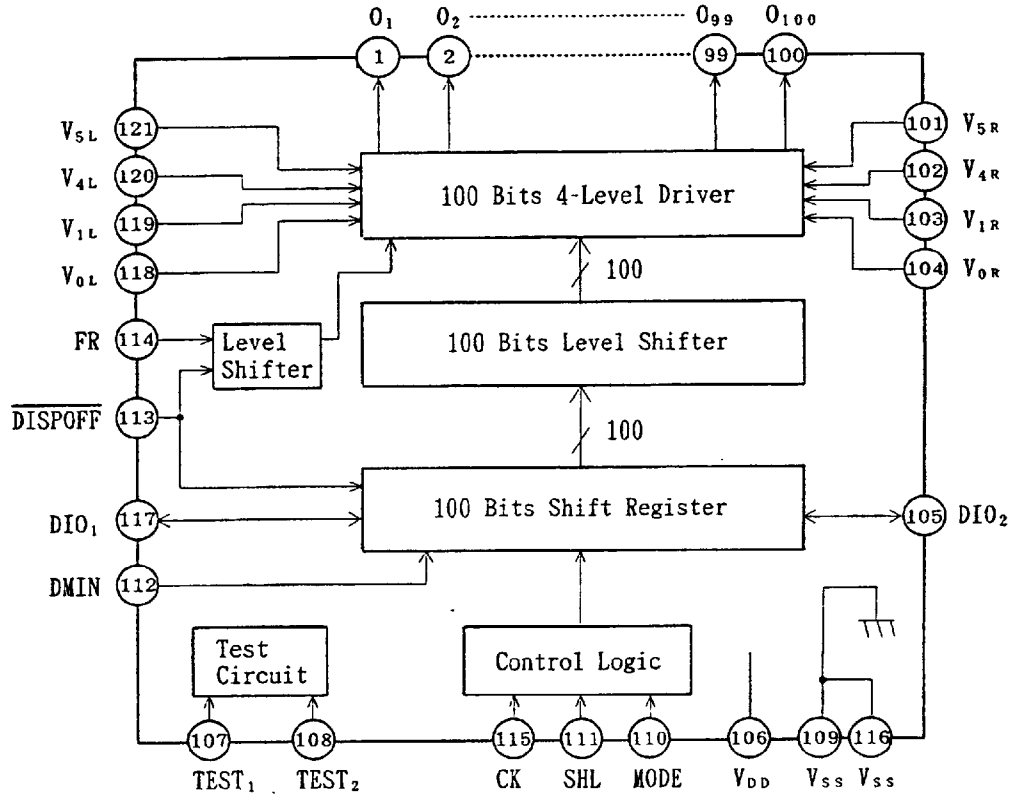
1. Summary

The LH1513AF is a 100 output common driver LSI suitable for driving black and white dot matrix LC panels.
Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LC module.
The LH1513AF is particularly well suited to driving black and white LC panels used for palmtop personal computers because of its low-voltage operation (Supply voltage for logic system : -5.5 to -2.5 V).
When combined with the LH1514A Segment Driver, a low power consuming, high-precision LC panel display can be assembled.
Data input/output pins are bidirectional, four data shift directions are pin-selectable.

2. Features

- Supply voltage for the logic system : -5.5 to -2.5 V
- Supply voltage for LC drive : -28.0 to -10.0 V
  (absolute maximum rating -30.0 V)
- Number of LC drive outputs : 100
- Low output impedance : 1.5 kΩ (Max.)
- Shift Clock frequency : 2.0 MHz (Max.)
- Low power consumption
- Built-in 100-bits bidirectional shift register (divisible into 50-bits x2)
- Available in a single mode (100-bits shift register) or in a dual mode (50-bits shift register x2)
  ① $O_1 \rightarrow O_{100}$ Single mode
  ② $O_{100} \rightarrow O_1$ "
  ③ $O_1 \rightarrow O_{50}$, $O_{51} \rightarrow O_{100}$ Dual mode
  ④ $O_{100} \rightarrow O_{51}$, $O_{50} \rightarrow O_1$ "
  The above 4 shift directions are pin-selectable
- Shift register circuit reset function when DISPOFF active
- Supports high capacity LC panel display when combined with the LH1514A Segment Driver
- CMOS process (N-type Silicon Substrate)
- Package : 121 pin TCP (Tape Carrier Package)
- Not designed or rated as radiation hardened

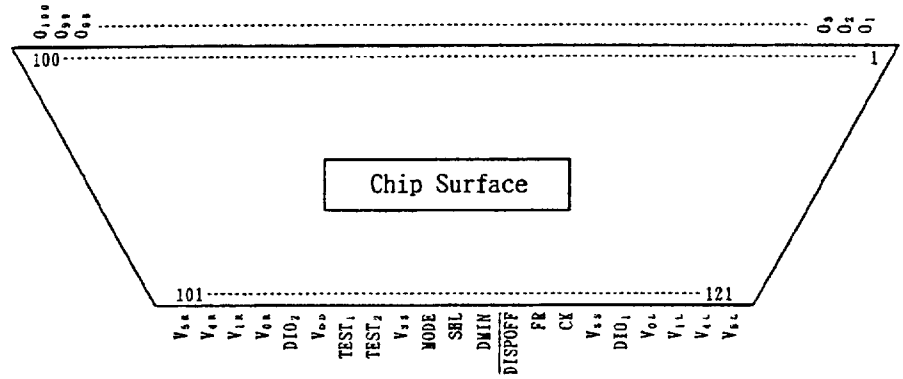
3. Block Diagram



4. Functional Operation of Each Block

Block	Function
Shift Register	Shifts data in from the data input pin on the falling edge of the CK signal, based on the data shift direction and mode setting received from the control logic block.
Level Shifter	The logic voltage signal is level-shifted to the LC drive voltage level, and outputs to the driver block.
4-Level Driver	Drives the LC driver output pins from the shift register data, selecting one of 4 levels (V_0, V_1, V_4, V_5) based on the FR and $\overline{\text{DISPOFF}}$ signals.
Control Logic	Controls the shift register's direction of data shift and mode setting in response to a SHL and MODE signal input.

5. Pin Configuration

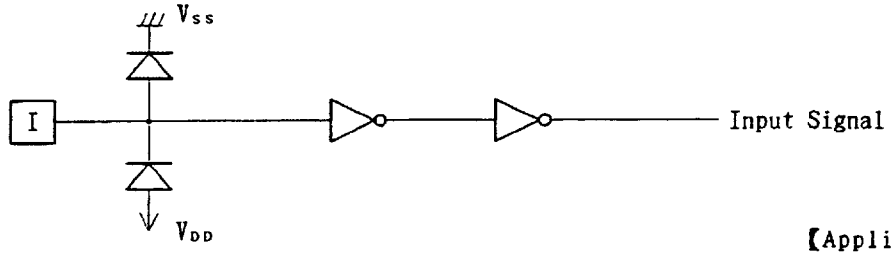


6. Pin Descriptions

6-1. Pin Designations

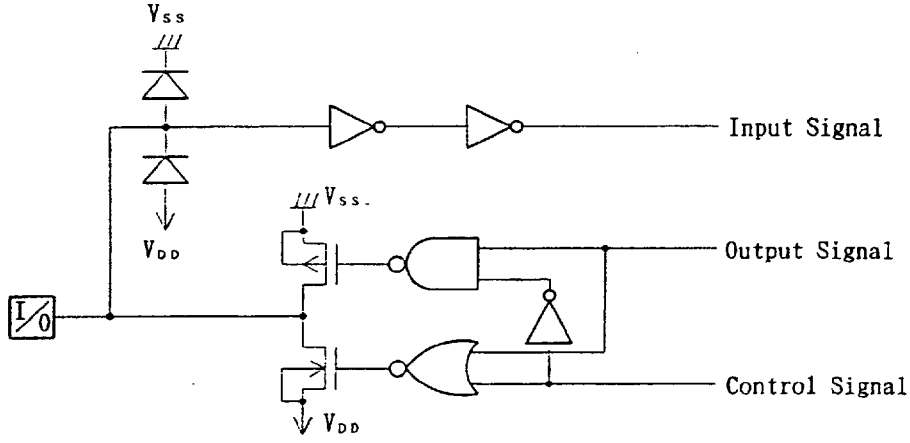
Pin No.	Symbol	I/O	Designation
1 to 100	O_1-O_{100}	O	LC drive output
101, 121	V_{5R}, V_{5L}	-	Power supply for LC drive
102, 120	V_{4R}, V_{4L}	-	Power supply for LC drive
103, 119	V_{1R}, V_{1L}	-	Power supply for LC drive
104, 118	V_{0R}, V_{0L}	-	Power supply for LC drive
105, 117	DIO_2, DIO_1	I/O	Data input/output for shift register
106	V_{DD}	-	Power supply for logic system (-5.5 to -2.5 V)
107	$TEST_1$	I	Test mode selection input
108	$TEST_2$	I	Test mode selection input
109, 116	V_{SS}	-	Ground (0 V)
110	MODE	I	Mode selection input
111	SHL	I	Shift direction selection for shift register
112	DMIN	I	Dual mode data input
113	$\overline{DISPOFF}$	I	Control input for deselect output level
114	FR	I	AC-converting signal input for LC drive waveform
115	CK	I	Shift clock input for shift register

6-2. Input/Output Circuits



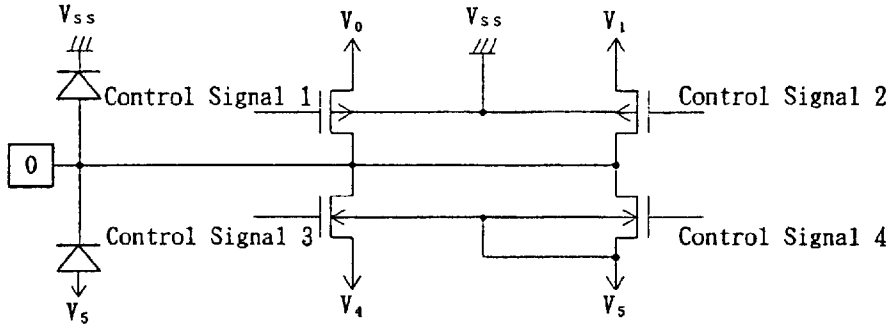
【Applicable pins】
SHL, MODE, $\overline{DISPOFF}$
FR, CK, DMIN
$TEST_1$, $TEST_2$

Fig.1 Input Circuit



【Applicable pins】
DIO_1, DIO_2

Fig.2 Input/Output Circuit



【Applicable pins】
O_1-O_{100}

Fig.3 LC Drive Output Circuit

7. Description of Functional Operations

7-1. Pin Functions

Symbol	Function
V_{DD}	Logic system power supply pin connects to -5.5 to -2.5 V
V_{SS}	Ground pin connects to 0 V
V_{0R}, V_{0L} V_{1R}, V_{1L} V_{4R}, V_{4L} V_{5R}, V_{5L}	Power supply pin for LC driver voltage bias. ·Normally, the bias voltage used is set by a resistor divider. ·Ensure that voltages are set such that $V_{SS} \geq V_0 > V_1 > V_4 > V_5$. ·To further reduce the difference between the output waveforms of LC driver output pins O_1 and O_{100}, externally connect V_{iR} and V_{iL} (i=0, 1, 4, 5).
DIO_1	Bidirectional shift register shift data input/output pin ·Input pin for right shift, output pin for left shift.
DIO_2	Bidirectional shift register shift data input/output pin ·Input pin for left shift, output pin for right shift.
CK	Bidirectional shift register shift clock pulse input pin ·Data is shifted on the falling edge of the clock pulse.
SHL	Bidirectional shift register shift direction selection pin ·Data is shifted right when set to V_{DD} level "L", and data is shifted left when set to V_{SS} level "H".
$\overline{DISPOFF}$	Control input pin for output deselect level ·The input signal is level-shifted from logic voltage level to LC drive voltage level,and controls LC drive circuit. ·When set to V_{DD} level "L", the LC drive output pins (O_1-O_{100}) are set to level V_0. ·While set to "L", the contents of shift register are reset not reading data. When the $\overline{DISPOFF}$ function is canceled,the driver output deselect level (V_1 or V_4), and the shift data is reading on the falling edge of the CK. That time,if $\overline{DISPOFF}$ removal time can not keep regulation what is shown AC characteristics (Page12),the shift data is not reading correctly.
FR	AC signal input for LC driving waveform ·The input signal is level-shifted from logic voltage level to LC drive voltage level, and Controls LC drive circut. ·Normally,inputs a frame inversion signal. ·The LC driver output pin's output voltage level can be set using the shift register output signal and the FR signal. ·Truth table is shown in 7-2-1.
MODE	Mode select pin ·When set V_{DD} level "L", Single Mode operation is selected, when set to V_{SS} level "H", Dual Mode operation is selected.
DMIN	Dual Mode data input pin ·According to the data shift direction of the data shift register, data can be input starting from the 51st bit.
$TEST_1$ $TEST_2$	Test mode select pin ·During normal operation, tie to V_{DD} level "L".

Symbol	Function
O_1-O_{100}	LC driver output pins ·Corresponding directly to each bit of the shift register, one level (V_0, V_1, V_4, or V_5) is selected and output.

7-2. Functional Operations

7-2-1. Truth Table

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (O_1-O_{100})
L	L	H	V_1
L	H	H	V_5
H	L	H	V_4
H	H	H	V_0
x	x	L	V_0

Here, $V_{SS} \geq V_0 > V_1 > V_4 > V_5$, L : V_{DD}(-5.5 to -2.5 V), H : V_{SS}(0 V), x : Don't care

【Note】"Don't care" should be fixed to "H" or "L", avoiding floating.

There are two kinds of power supply (logic level voltage,LC drive voltage) for LCD driver,please supply regular voltage which assigned by specification for each power pin.

7-2-2. Relationship between the Data I/O Pins and Data Transfer Direction

MODE	SHL	DIO_1	DIO_2	DMIN	Data Transfer Direction
L (Single)	L(shift to right)	Input	Output	x	$O_1 \rightarrow O_{100}$
	H(shift to left)	Output	Input	x	$O_{100} \rightarrow O_1$
H (Dual)	L(shift to right)	Input	Output	Input	$O_1 \rightarrow O_{50}$
					$O_{51} \rightarrow O_{100}$
	H(shift to left)	Output	Input	Input	$O_{100} \rightarrow O_{51}$
					$O_{50} \rightarrow O_1$

Here, L : V_{DD}(-5.5 to -2.5 V), H : V_{SS}(0 V), x : Don't care

【Note】"Don't care" should be fixed to "H" or "L", avoiding floating.

7-2-3. Connection Examples for Plural Common Drivers

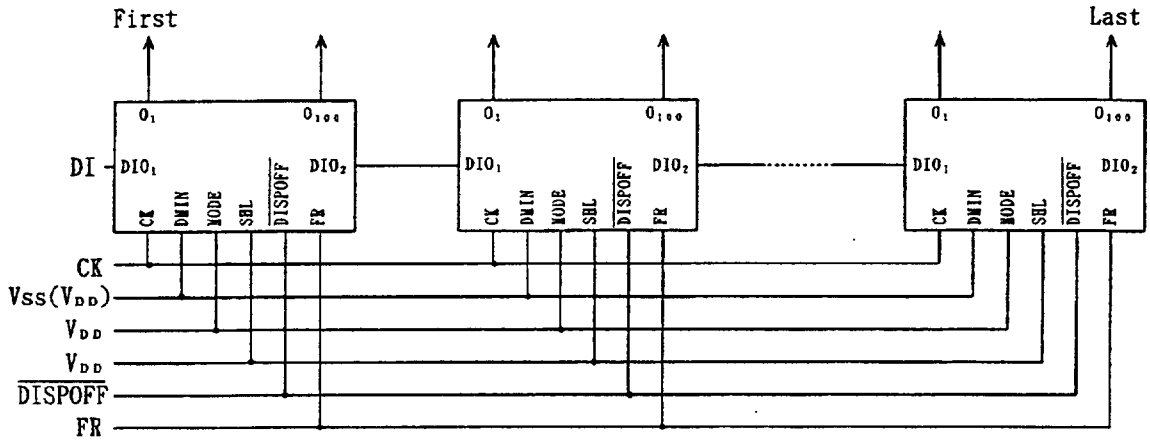


Fig. 1 Single Mode (Shifting toward right)

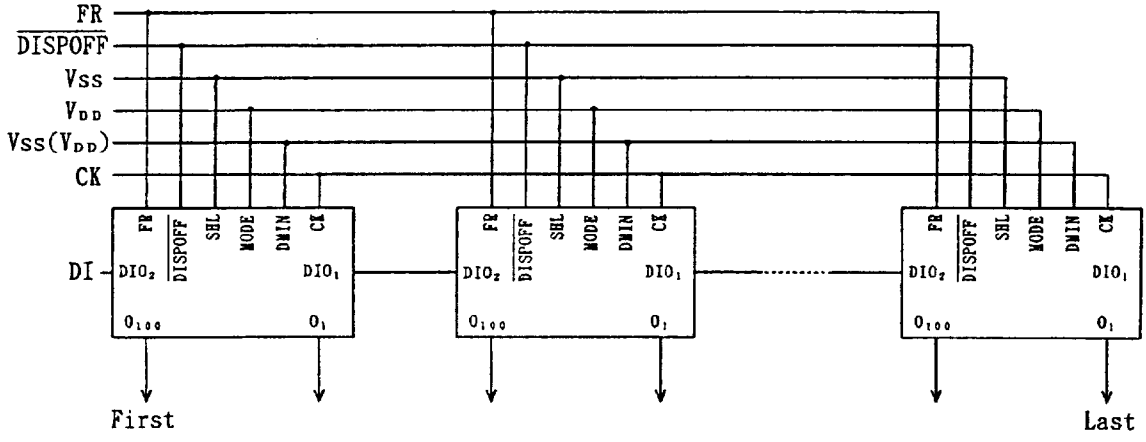


Fig. 2 Single Mode (Shifting toward left)

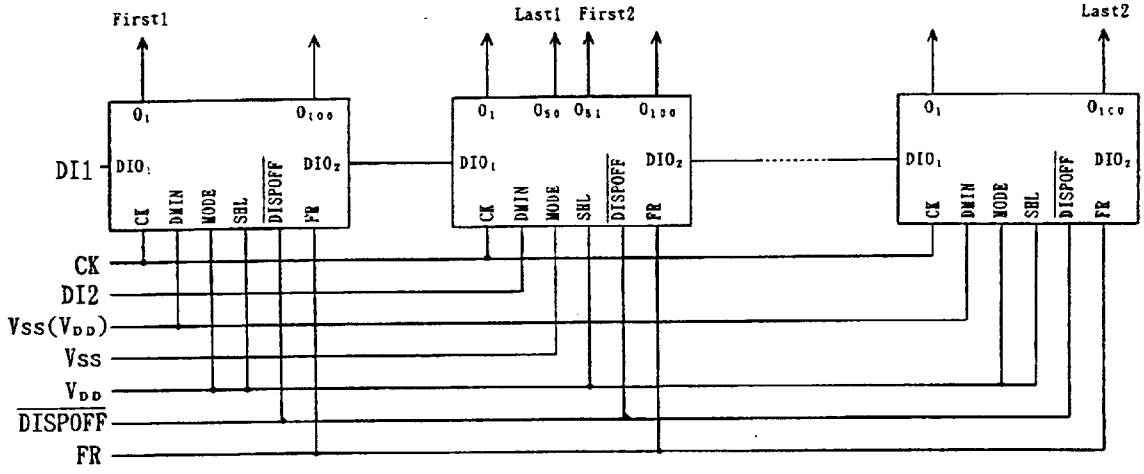


Fig. 3 Dual Mode (Shifting toward right)

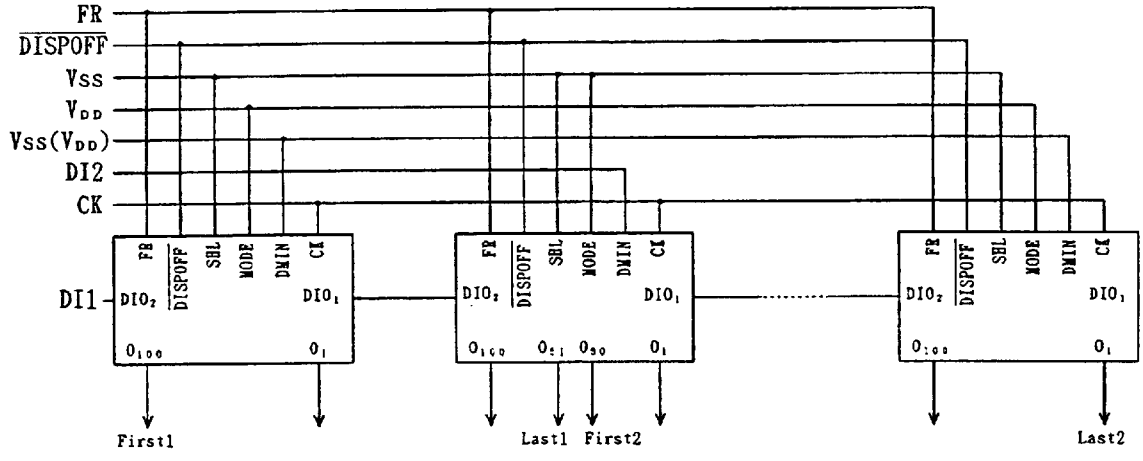


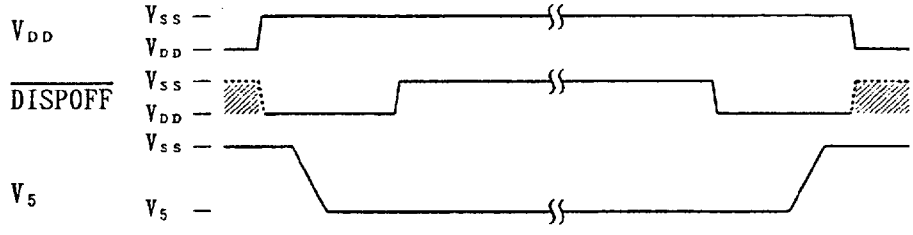
Fig. 4 Dual Mode (Shifting toward left)

8. Precaution

○Precaution when connecting or disconnecting the power
This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LC drive power supply while the logic system power supply is floating.
The detail is as follows.

- When connecting the power supply, connect the LC drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LC drive power.
- We recommend you connecting the serial resistor (50 to 100 Ω) to the LC drive power V_5 of the system as a current limitter resistor. And set up the suitable value of the resistor in consideration of LC display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connecting the LC drive power supply after resetting logic condition of this LSI inside on $\overline{DISPOFF}$ function. After that, cancel the $\overline{DISPOFF}$ function after the LC drive power supply has become stable. Furthermore, when disconnecting the power, set the LC driver output pins to level V_0 on $\overline{DISPOFF}$ function. After that, disconnect the logic system power after disconnecting the LC drive power.
When connecting the power supply, show the following recommend sequence.



9. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	V_{DD}	Ta=25 ℃	V_{DD}	-7.0 to +0.3	V
Supply voltage (2)	V_0	Referenced	V_{0L}, V_{0R}	V_5-0.3 to +0.3	V
	V_1	to V_{SS}(0 V)	V_{1L}, V_{1R}	V_5-0.3 to +0.3	V
	V_4		V_{4L}, V_{4R}	V_5-0.3 to +0.3	V
	V_5		V_{5L}, V_{5R}	-30.0 to +0.3	V
Input voltage	V_I		DIO_1, DIO_2, DMIN, SHL MODE, CK, FR, $\overline{DISPOFF}$	V_{DD}-0.3 to +0.3	V
Storage temperature	T_{stg}			-45 to +125	℃

10. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{DD}	Referenced	V_{DD}	-5.5		-2.5	V
Supply voltage (2)	V_5	to V_{SS}(0 V)	V_{5L}, V_{5R}	-28.0		-10.0	V
Operating temperature	T_{opr}			-20		+85	℃

11. Electrical Characteristics

11-1. DC Characteristics

(V_{SS}=V_0=0 V, V_{DD}=-5.5 to -2.5 V, V_5=-28.0 to -10.0 V, Ta=-20 to +85 ℃)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}		DIO_1, DIO_2, DMIN, SHL	0.2V_{DD}			V
	V_{IL}		MODE, CK, FR, $\overline{DISPOFF}$			0.8V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4 mA	DIO_1, DIO_2	-0.4			V
	V_{OL}	I_{OL}=+0.4 mA				V_{DD}+0.4	V
Input leakage current	I_{LI}	$V_{SS}\leqq V_I \leqq V_{DD}$	DMIN, SHL, MODE, CK FR, $\overline{DISPOFF}$			±10.0	μA
I/O leakage current	$I_{LI/O}$	$V_{SS}\leqq V_I \leqq V_{DD}$	DIO_1, DIO_2			±10.0	μA
Output resistance	R_{ON}	*1	O_1-O_{100}		1.0	1.5	kΩ
Stand-by current	I_{STB}	*2	V_{SS}			50.0	μA
Consumed current (1)	I_{DD}	V_{DD}=-3 V,*3	V_{DD}			20.0	μA
		V_{DD}=-5 V,*3				30.0	μA
Consumed current (2)	I_5	V_{DD}=-3 V,*3	V_{5L}, V_{5R}			50.0	μA
		V_{DD}=-5 V,*3				50.0	μA

【Note】

*1 : V_5=-28.0 to -10.0 V, $|\Delta V_{ON}|$=0.5 V

*2 : V_{DD}=-5.0 V, V_5=-28.0 V, V_{IH}=V_{SS}, V_{IL}=V_{DD}, $TEST_1$=$TEST_2$=V_{DD}

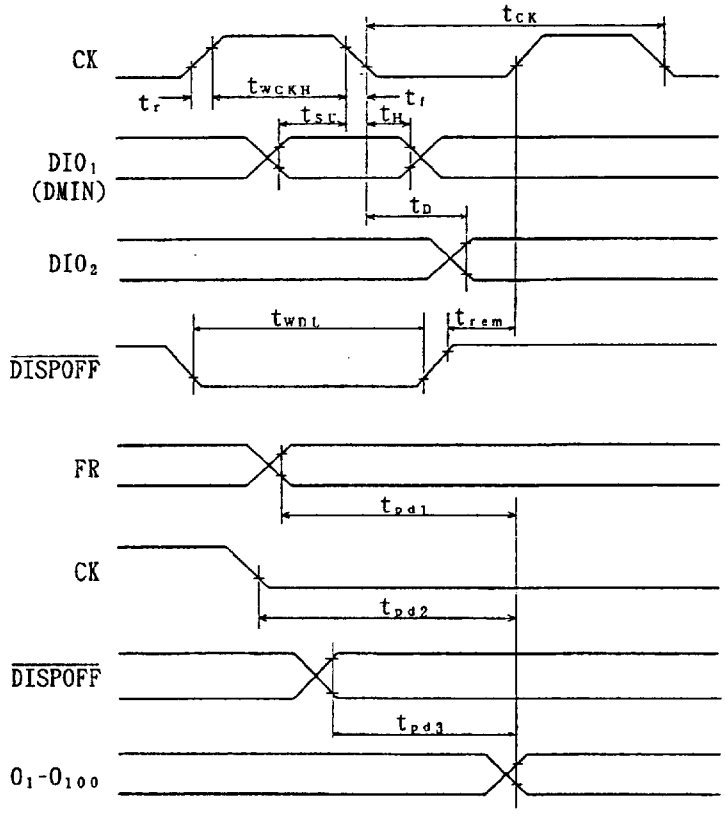
*3 : V_5=-28.0 V, f_{CK}=19.2 kHz, f_{FR}=80 Hz, No-load
(Consumed current is case of 1/240 duty operation)

11-2. AC Characteristics

($V_{SS}=V_0=0$ V, $V_{DD}=-5.5$ to -2.5 V, V5=-28.0 to -10.0 V, Ta=-20 to $+85$ ℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period	t_{CK}		500			ns
Shift clock "H" pulse width	t_{WCKH}		65			ns
Data setup time	t_{SU}		100			ns
Data hold time	t_H		100			ns
$\overline{\text{DISPOFF}}$ "L" pulse width	t_{WDL}		1.2			µs
$\overline{\text{DISPOFF}}$ removal time	t_{rem}		100			ns
Input signal rise time	t_r				50	ns
Input signal fall time	t_f				50	ns
Output delay time (1) CK to DIO_1, DIO_2	t_D	C_L=15 pF			350	ns
Output delay time (2) FR to O_1-O_{100}	tpd_1				1.2	µs
Output delay time (3) CK to O_1-O_{100}	tpd_2				1.2	µs
Output delay time (4) $\overline{\text{DISPOFF}}$ to O_1-O_{100}	tpd_3				1.2	µs

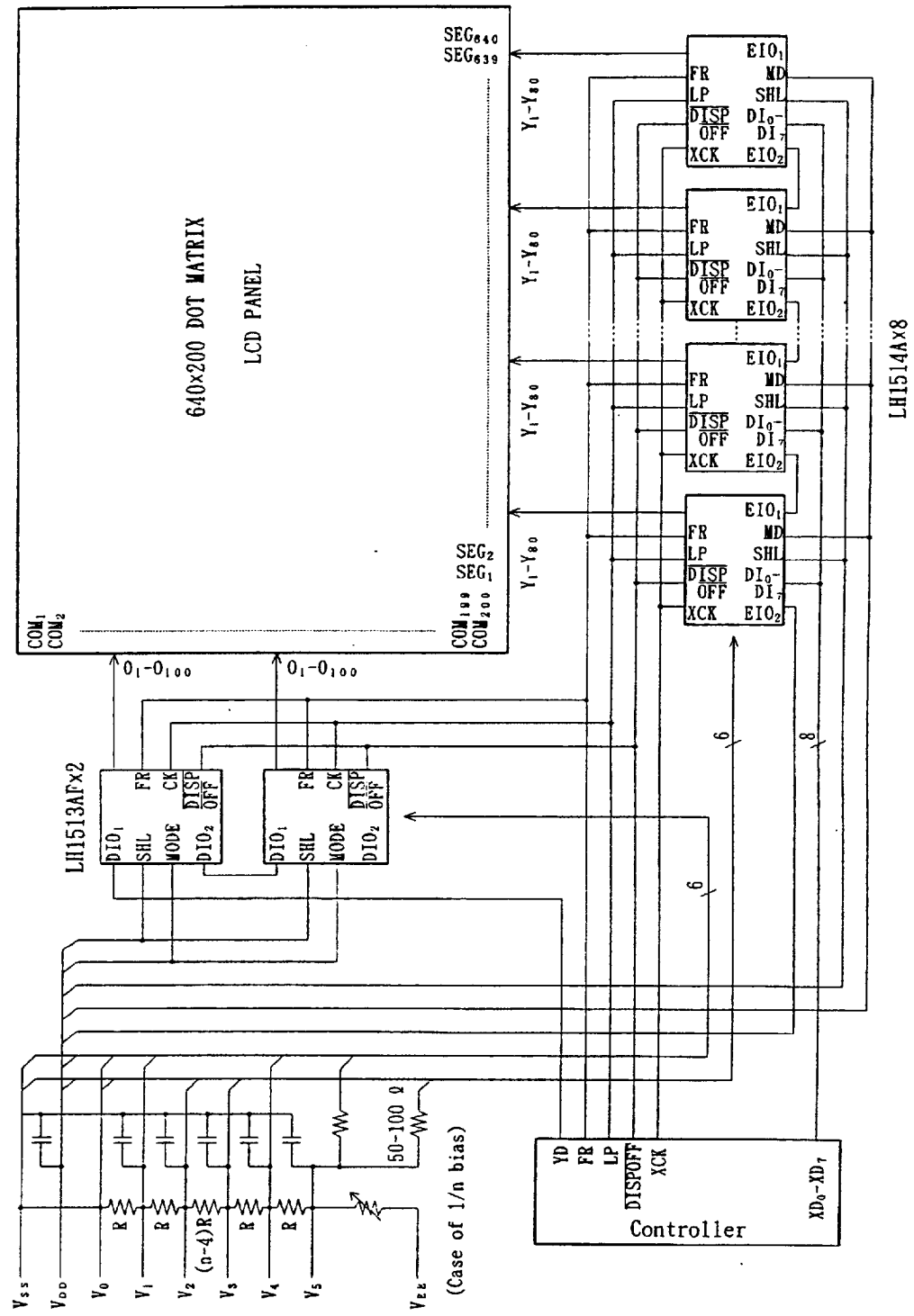
11-3. Timing Diagram



[SHL="L"]

Timing chart

12. Example of System Configuration



13. Example of Typical Characteristic

Parameter	Conditions	Mim.	Typ.	Max.	Unit
Typical Fundamental Rating Propagation Delay Time	Ta=+25 ℃, V_{SS}=0 V, V_{DD}=-5.0 V		50		ns

14. PACKAGE AND PACKING SPECIFICATION

1. Package Outline Specification
   Refer to drawing No. SPN2161-00

2. Markings
   The meanings of the device code printed on each tape carrier package are as follows.

   (1) Date code (example) : $\underset{a)}{4}\ \underset{b)}{37}\ \underset{c)}{0}$

   a) denotes the last figure of Anno Domini (of production)
   b) denotes the week (of production)
   c) denotes the number of times of alteration

3. Packing Specifications

   (1) Packing Materials

Item	Material	Purpose
Reel	Anti-static treated plastic (405mm dia.)	Packing of tape carrier package.
Separator	Anti-static treated PET (188 μm)	Protects device and prevents ESD (Electro Static Discharge)
Laminated aluminium bag	(520 × 600mm)	Keeping dry.
Adhesive tape paper		Fixing of tape carrier package and sparator.
Carton	Cardboard(420x420x50mm)	Contains a reel.
Label	Paper	Indicates production name, lot.No., and quantity.
Desiccant	Silica gel	Drying of device

   (2) Packing Form

   a) Tape carrier package(TCP)is wound on a reel with separators 1 and 2 and the ends of them are fixed with adhesive tape.
   b) A label indicating production name, lot no. and quantity is stuck on one side of the reel.
   c) The reel and silica gel is put in a laminated aluminium bag. Nitrogen gas is enclosed in the bag and the bag is sealed. The same label(b) is affixed to the bag. The bag is put in a carton and the same label(b) is affixed to one side of the carton.

* Specification of label

TYPE	PRODUCTION NAME LOT NO.
QUANTITY	QUANTITY
LOT(DATE)	SHIPPING DATE

4. Miscellaneous

   (1) The length of the tape carrier is 34 ~ 46 meters maximum per reel, and depends on shipping quantity.

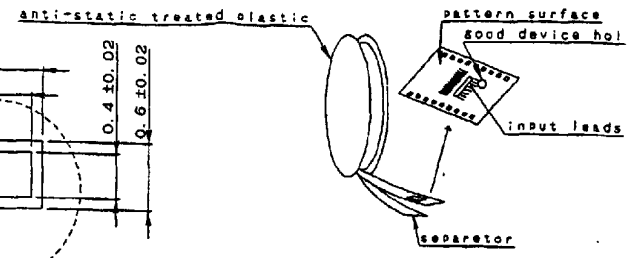
   (2) Before unpacking, prepare a work bench equipped with anti-static devices. Also, the operater shoud ware anti-static wrist bands.

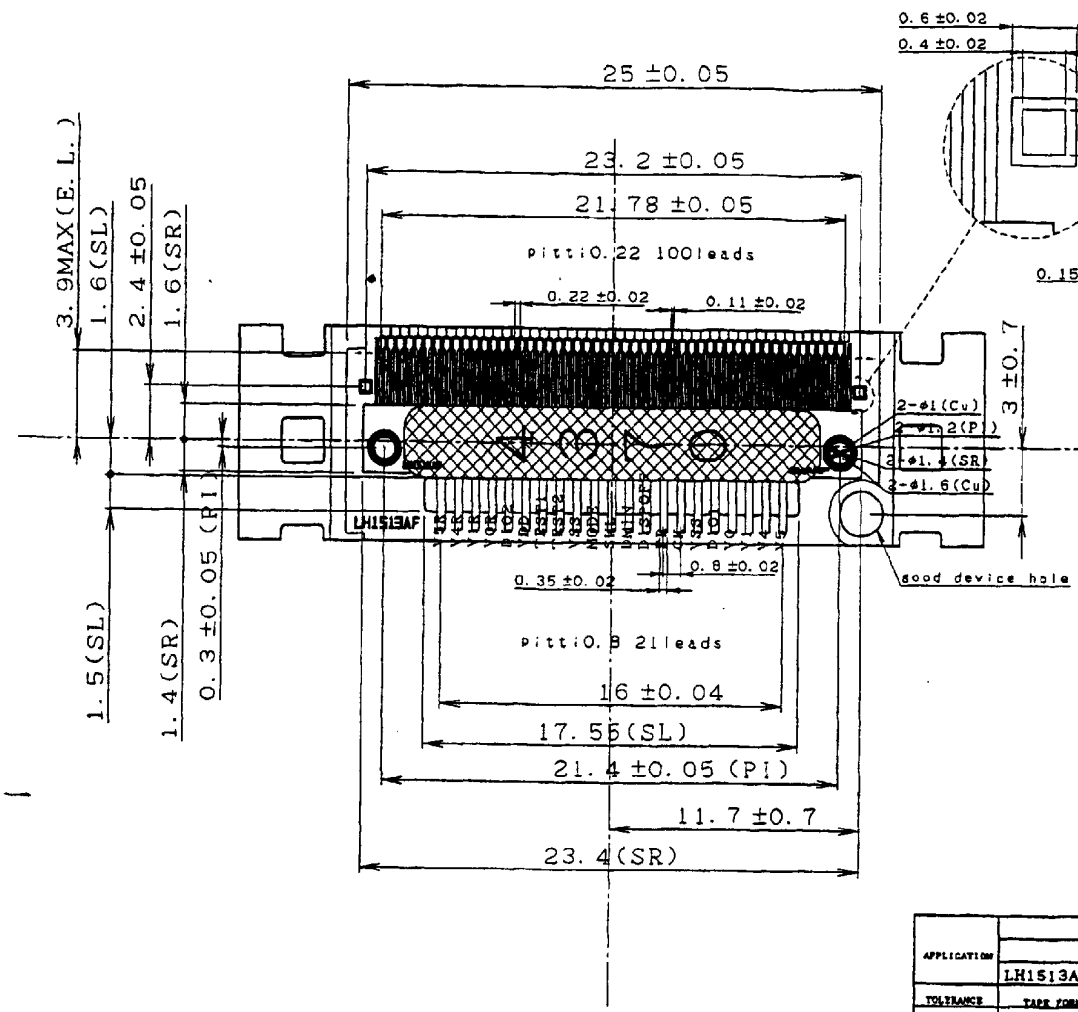
   (3) The device, once unpacked, should be stored in a nitrogen gas, room temperature atomosphere and used within 1 week.

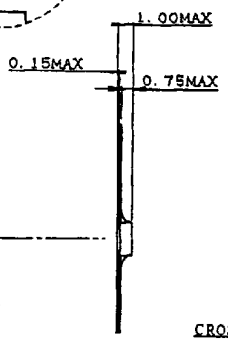
ISSUE DATE	AUG.24.1994	APROVE	CHECK	DESIGN	(NOTE)
ISSUE NUMBER	H6804	A. Suzuki	Y. Hondo	T. Hidoguchi	
S/C NUMBER					

SHARP

NOTES: 1. REEL WINDING

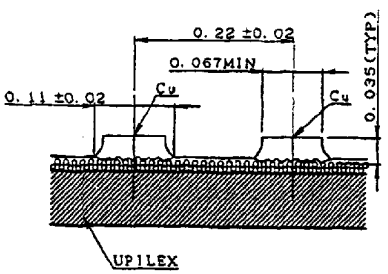






2. RESIN AREA OF FRONT AND BACK SURFACE IS 20.0X3.5mm(MAX).
3. E.L. MEANS ASSUMED EXCISING LINE.
4. SL MEANS DIMENSION OF PUNCHING HOLE AND ITS TOLERANCE IS ±0.05mm.
5. SR MEANS DIMENSION OF SOLDER RESIST AND ITS TOLERANCE IS ±0.3mm.

CROSS SECTION OF OUTPUT LEADS



APPLICATION		SCALE	UNIT
	LH1513AF	5/1	mm
TOLERANCE	TAPE FORMAT	TAPE MATERIALS	FINISH
±0.1	35mmWIDE TYPE 2 PERFO-PITCH	UPILEX S75 ADHESIVE #6700 ED Cu(SLP) SOLDER RESIST	TIN PLATING
DATE	AUG. 24. 1994		
DESIGN	T. KIDOGUCHI	ASSEMBLY ENGINEERING DEPT.	
DRAWING	T. KIDOGUCHI	IC GROUP	
CHECK	A. Suzuki	SHARP CORPORATION	

DATE	REVISE	CHARGE
TITLE	OUT LINE DRAWING OF LH1513AF	
CODE		
DRAWING NO.	SPN2161-00	