T-41-39

LM020L
LM020LN (EL Backlit Version)

- 16 character x 1 line
- Controller LSI HD44780 is built-in (See page 115).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	80W x 36H x 12T (max.) mm
Effective display area	64.5W x 13.8H mm
Character size (5 x 7 dots)	3.07W x 5.73H mm
Characrer pitch	3.77 mm
Dot size	0.55W x 0.75H mm
Weight	about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

EL Power Supply (when fitted)
Voltage (VEL) . . . . . AC 150 Vms
Frequency (fEL) (at 100 Vms) 1kHz

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	1.0 mA typ. 2.0 mA max.

Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/16

Range of $V_{DD}-V_O$	1.5~5.25 V
Ta = 0°C	4.6 V typ.
Ta = 25°C	4.4 V typ.
Ta = 50°C	4.2 V typ.

Power Supply for EL (when fitted)

VEL (typ. at 400Mz)	100 Vms
fEL (max at VEL 100V, fEL 400Hz)	9.5mA

OPTICAL DATA . . . . . See page 5.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	V_{SS}	—	0V (Power supply)
2	V_{DD}	—	+5V (Power supply)
3	V_O	—	— (Power supply)
4	RS	H/L	L: Instruction code input H: Data input
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)
6	E	H, H→L	Enable signal
7	DB0	H/L	Data bus line Note (1), (2)
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	

Luminescent output of EL (where fitted) at Ø = 25°C, Ø = 0°C - 6cd / m^2 typ.

Notes:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.
(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).
(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

DRIVING INFORMATION

To reduce component count, this module is configured as a 2 line of 8 character display but with these organised to visually appear as 1 line of 16 characters.

The consequences are :

1) on power up this must be configured as 2 line display
2) character address not continuous 0 - 7 address is 00HEX - 07HEX, 8 - 15 address is 40HEX - 47HEX

Unit: mm

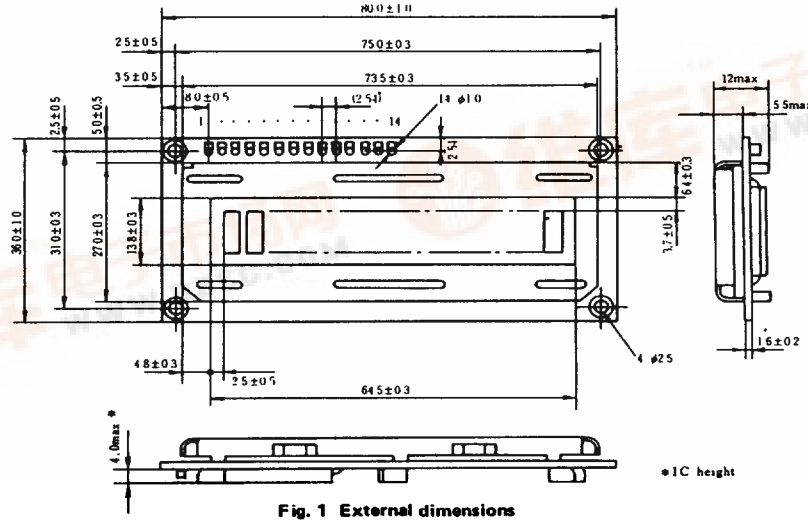


Fig. 1 External dimensions

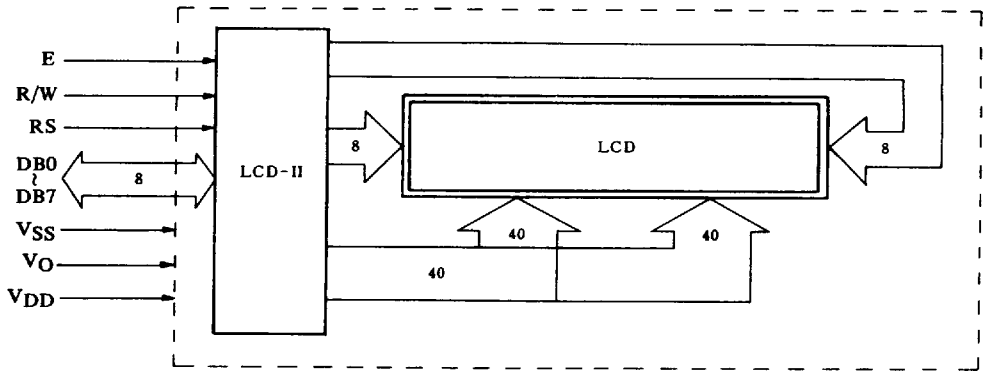
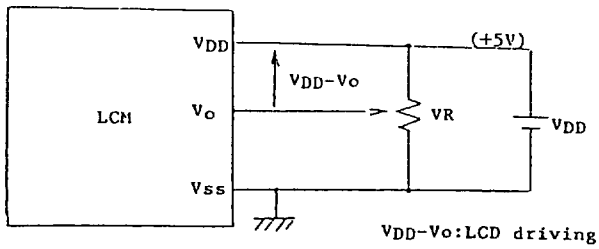


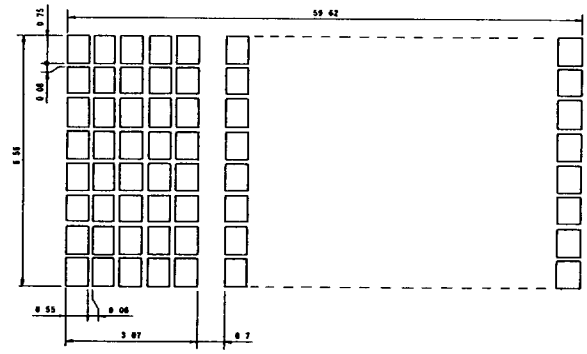
Fig. 2 Block diagram

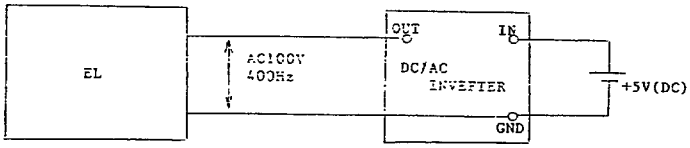


VDD-Vo:LCD driving voltage

VR:10k 20k

POWER SUPPLY for LCM

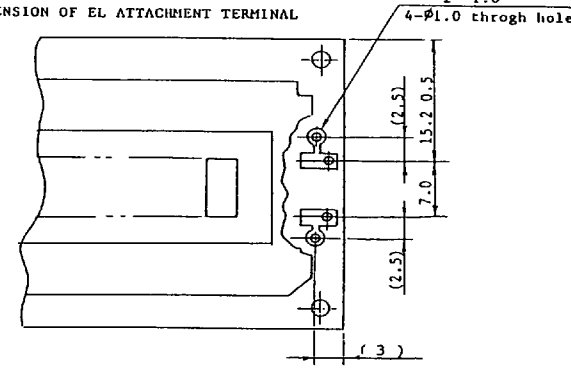




Recommended DC/AC INVERTER : NEL-D32-45
(Made by NEC)

POWER SUPPLY for EL

DIMENSION OF EL ATTACHMENT TERMINAL



TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	PW_{EH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

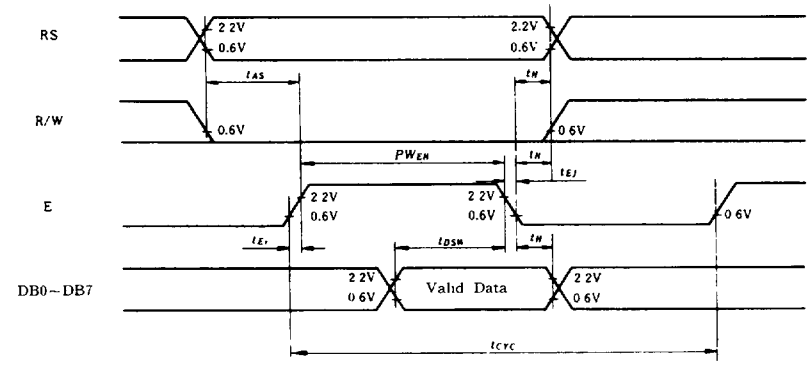


Fig. 5 Interface timing (data write)

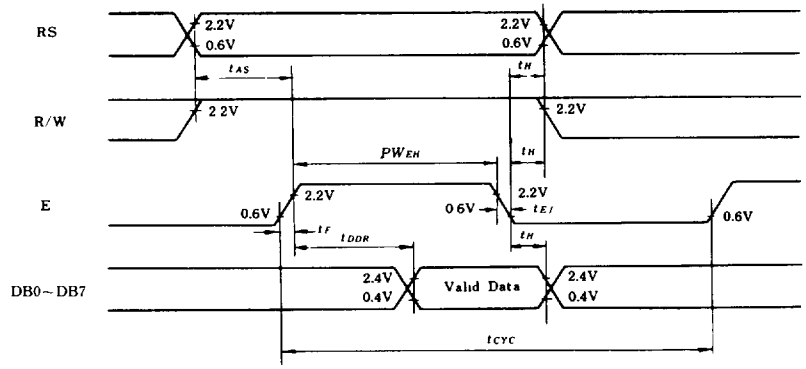


Fig. 6 Interface timing (data read)