Z02201

V.22BIS MODEM DATA PUMP WITH INTEGRATED AFE

FEATURES

Device	Data Pump	AFE	Speed (MHz)
Z02201	16-Bit	Integrated	12.5

- Combined Data Pump and Analog Front-End (AFE)
- Data Modem Throughput to 2400 bps
  - ITU V.22bis, V.23, V.22, V.21
  - Bell 212A and Bell 103
- FSK (V.23 1200/75 bps, V.21/Bell103 300 bps), DPSK (V.22/Bell 212A 1200 bps), or QAM Encoding (V.22bis 2400 bps)
- Programmable Bi-Quad Tone Detectors for Call Progress Tone Detection
- Scrambler/descrambler Functions plus Selectable Control Over Internal data pump Functions
- Adaptive Equalization to Compensate for a Wide Variety of Line Conditions
- Programmable Transmit Attenuation and Selectable Receive Threshold
- Fully Programmable Call Progress Detectors, Signal Quality Detectors, Tone Detectors, Tone Generators, and Transmit Signal Levels Aid in Rapid Country Qualifications
- Host Port Allows Direct Parallel Interface to Standard 8Bit Microprocessors
- HDLC Framing at All Speeds
- On-Chip Peripherals
  - Full-Duplex Voice Band AFE with 12-Bit Resolution
  - V.24 Compatible Serial Interface Port
  - Eye Pattern Interface
- Low Power Consumption: 50 mA Typical
- 44-Pin PLCC Package
- Single +5 VDC Power Supply
- 0°C to +70°C Commercial Temperature Range and –40°C to +85°C Extended Temperature Range

Note: (1) International Telecommunications Union (ITU), formerly CCITT.

GENERAL DESCRIPTION

The Z02201 is a synchronous single-chip modem which provides a means to construct a V.22bis modem capable of 2400 bps full duplex over dial-up lines. This device is specifically designed for use in embedded modem applications where space, performance, and low-power consumption are key requirements.

Operating over the Public Switched Telephone Network (PSTN), the Z02201 meets the modem standards for V.22bis, V.22, V.23, V.21, Bell 212A, and Bell 103.

A typical modem can be made by simply adding a control microprocessor (host), phone line interface, and DTE interface.

The Z02201 performs HDLC framing at all speeds. This capability eliminates the need for an external Serial Input/Output (SIO) device in Data Terminal Equipment (DTE) for products incorporating error correction.

All modulation, demodulation, filtering, A/D and D/A conversion functions for transmit and receive are provided on-chip.

GENERAL DESCRIPTION (Continued)

Automatic and selectable compromise equalizers are included to optimize performance over a wide range of line types.

The Z02201 device compensates for a wide variety of adverse line conditions by using a combination of fixed link, fixed cable, and adaptive equalizers.

The Z02201 provides comprehensive selectable and programmable tone generation and detection.

All digital I/O signals are TTL compatible. The parallel interface is compatible with standard 8-bit microprocessors, allowing direct access to eight I/O registers and indirect access to the modem RAM.

The RAM access capability allows the host to retrieve diagnostic data, modem/line status and control data and set programmable coefficients. The serial interface is used for data transfer and is compatible with V.24 specifications. All control and status information is transferred by means of the parallel interface.

The Z02201 transmit drivers and receive amplifiers can be connected directly to a Data Access Arrangement (DAA) by means of a transformer, thereby reducing the external circuits to a minimum.

In addition, the Z02201 provides for further system level savings by providing built-in filters for both the Transmitter Analog Output and the Receiver Analog Input, thus eliminating the need for external filtering components.

The Z02201 device operates on a single +5 VDC power supply. During periods of no traffic, the host can place the modem into Sleep mode, reducing power consumption to less than 1 percent of full load power.

Notes: All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$ (WORD is active Low); $\overline{B}$/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

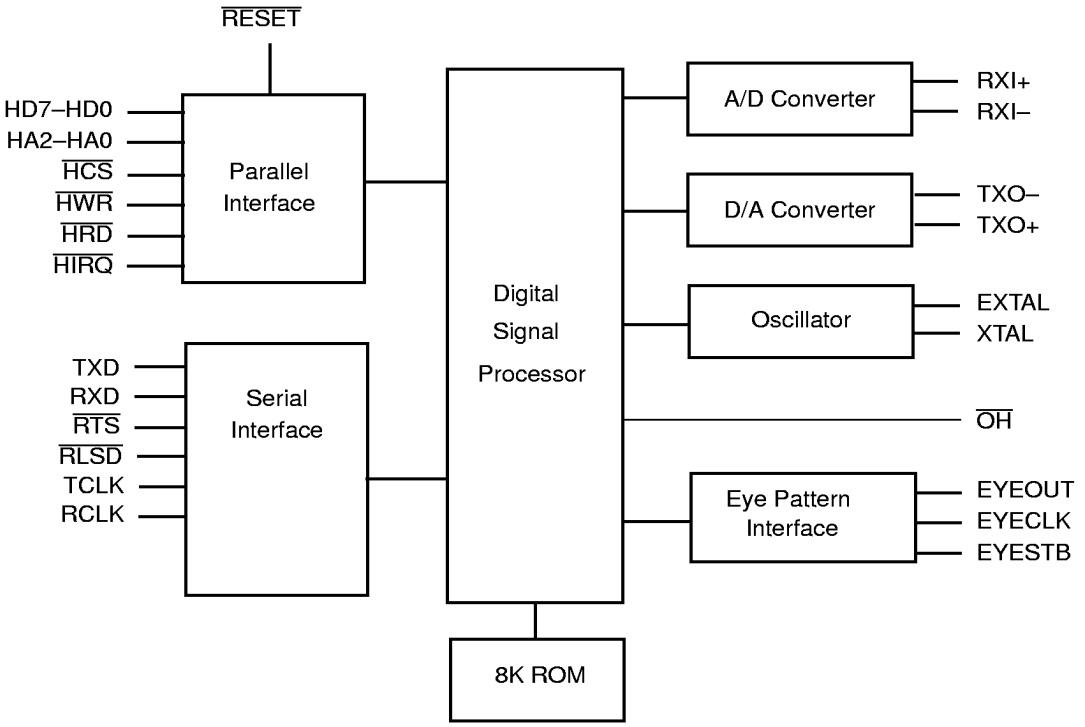


Figure 1. Z02201 Block Diagram

USER INFORMATION

The Zilog Z02201 data pump chip can be selected for either parallel or serial synchronous data transfer under software control. Figure 1 shows a block diagram of the general modem interface. The hardware and software Configurations can be customized for a particular modem application. The parallel interface allows direct access to 8 I/O registers, indirect access to the modem RAM, and is compatible with most 8-bit microprocessors, including the Z8, Z80 and Z18X family devices. The serial interface is used for data transfer and is compatible with V.24. All controls and status information are transferred via the parallel interface. The RAM access capability allows indirect access to diagnostic data, additional status control, and programmable coefficients. The hardware and software interfaces are presented in the subsequent sections.

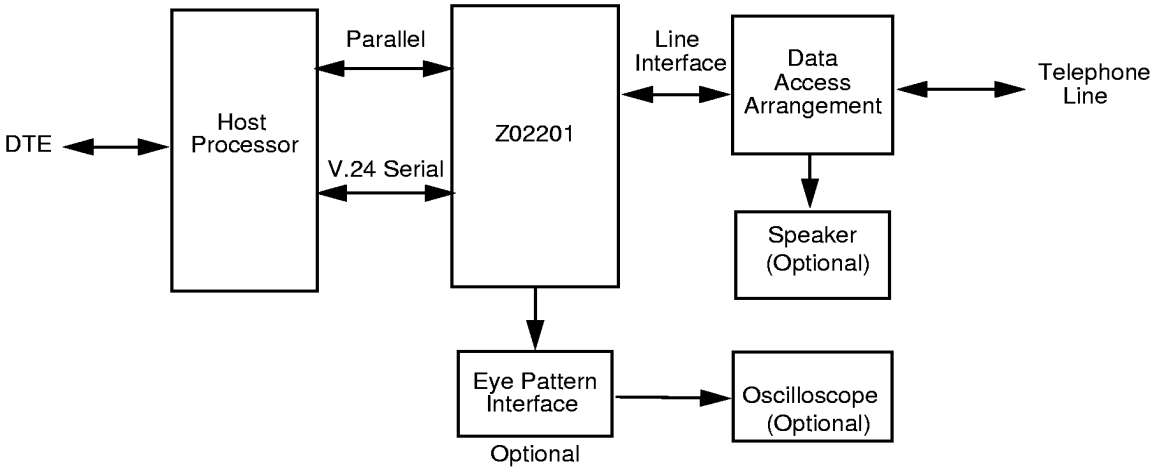


Figure 2. Z02201 System Block Diagram

PIN DESCRIPTION

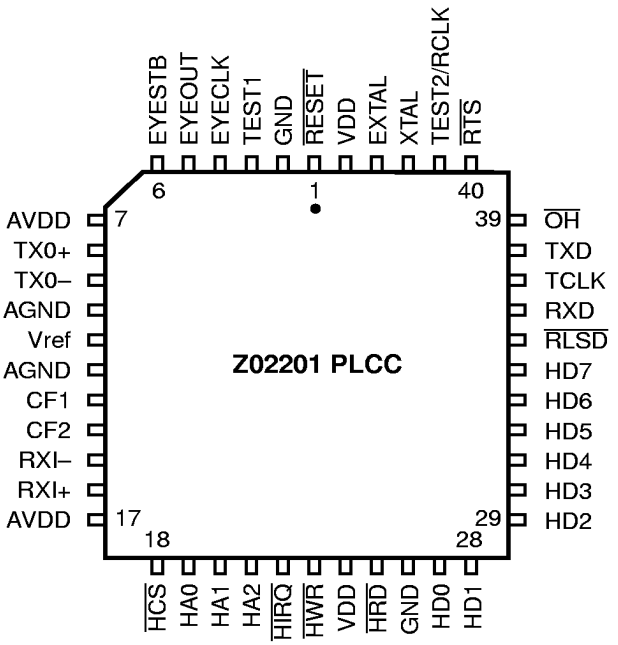


Figure 3. Z02201 44-Lead PLCC Pin Identification

Table 1. Z02201 Modem Pin Assignments

Pin No.	Symbol	Direction
1	$\overline{\text{RESET}}$	Input
2	GND	
3	TEST1	Input
4	EYECLK	Output
5	EYEOUT	Output
6	EYESTB	Output
7	AV_{DD}	
8	TXO+	Analog Output
9	TXO–	Analog Output
10	A_{GND}	
11	Vref	Analog Output
12	A_{GND}	
13	CF1	Analog Input
14	CF2	Analog Input
15	RXI–	Analog Input
16	RXI+	Analog Input
17	AV_{DD}	
18	$\overline{\text{HCS}}$	Input
19	HA0	Input
20	HA1	Input
21	HA2	Input
22	$\overline{\text{HIRQ}}$	Output

Table 1. Z02201 Modem Pin Assignments

Pin No.	Symbol	Direction
23	$\overline{\text{HWR}}$	Input
24	V_{DD}	
25	$\overline{\text{HRD}}$	Input
26	GND	
27	HD0	Input/Output
28	HD1	Input/Output
29	HD2	Input/Output
30	HD3	Input/Output
31	HD4	Input/Output
32	HD5	Input/Output
33	HD6	Input/Output
34	HD7	Input/Output
35	$\overline{\text{RLSD}}$	Output
36	RXD	Output
37	TCLK	Output
38	TXD	Input
39	$\overline{\text{OH}}$	Output
40	$\overline{\text{RTS}}$	Input
41	TEST2/RCLK	Input/Output
42	XTAL	Output
43	EXTAL	Input
44	V_{DD}	

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage	–0.3	+7.0	V
T_{OPR} (com)	Operating Temperature	0	+70	∞C
T_{OPR} (ext)	Operating Temperature	–40	+85	°C
T_{STG}	Storage Temperature	–65	+150	°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Parameters will be tested as per the table referencing the DC Characteristics. The Z02201 tester has active loads which are used to test the loading for I_{OH} and I_{OR}.

Available operating temperature range is:

S=0°C to +70°C

E=–40°C to +85°C

Voltage Supply Range:

+4.5 V ≤ V_{CC} ≤ + 5.5 V

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for address and control lines.

POWER REQUIREMENTS

The modem power and environmental requirements are shown in tables 2 and 3 below.

Voltage	Current Typical @ 25°C	Current Maximum @ 0°C
+5 V_{DC}, Operating	50 mA	≤ 100 mA
+5 V_{DC}, Sleep	25 µA	≤ 125 µA

Notes:

1. All voltages are ±5% DC and must have ripple less than 0.1V. peak to peak. If switching supply is used, the frequency may be between 20 kHz and 150 kHz. No component of the switching frequency should be present outside of the supply greater than 500 µV peak.

ENVIRONMENTAL REQUIREMENTS

Table 2. Environmental Requirements

Parameter	Value
Ambient Temperature Under Bias (Commercial Temp Range)	0°C to +70°C
Ambient Temperature Under Bias (Extended Temp Range)	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Voltage on any pin to V_{SS}	–0.3V to +7V
Power Dissipation	250mW
Soldering Temperature 10 sec	+230°C

Table 3. Crystal Specification

Parameter	Value∞
Temperature Range (Commercial) Temperature Range (Extended)	0°C to +70°C –40°C to +85°C
Nominal Frequency @ 25 °C	24.576 MHz
Frequency Tolerance @ 25 °C	± 20 PPM
Temperature Stability @ 0 °C to 70 °C	± 25 PPM
Calibration Mode	Parallel Resonant
Shunt Capacitance	7 pF Max.
Load Capacitance	32 ±0.3 pF
Drive Level	1.0 mW max.
Aging, per Year Max.	±5 PPM
Oscillation Mode	Fundamental
Series Resistance	60Ω max.
Max. Frequency Variation with 28.8 or 35.2 pF load	±30 PPM

DC CHARACTERISTICS

Table 4. TDC Pin Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Units
Pin Types I & I/O: Input & Input-Output						
V_{IH}	Input High Voltage		2	–	V_{CC} +0.3	V
V_{IL}	Input Low Voltage		0	–	0.8	V
I_L	Input Leakage Current	GND <V0<V_{DD}	–10	–	10	µA
Pin Types O & IO: Output & Input-Output						
V_{OH}	Output High Voltage	$I_{OH=}$ –200 µA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OI} –2.2 mA	0	–	0.4	V
I_{OZ}	Tri-state Leakage Current	GND<V0<V_{DD}	–10	–	10	µA
Pin Types I-PU & I-PD: Input with Internal pull-up/pull-down resistor						
V_{IH}	Input High Voltage		2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage		0		0.8	V
I_{IL}	Input Current	GND <V0<V_{DD}	–10		10	µA
Pin Type XI: Crystal Input						
V_{IH}	Input High Voltage		V_{DD} x0.8		V_{DD}	V
V_{IL}	Input Low Voltage		0			
Pin Type O–OD: Output with Open-Drain						
V_{OL}	Output Low Voltage	I_{OI}=2.2 mA	0	–	0.4	
I_{OZ}	Tri-state Leakage Current	GND<V0<V_{DD}	–10	–	10	µA
Pin Type XO: Crystal output						
V_{OH}	Output High Voltage	I_{OH}=1.0 mA	V_{DD} –1		V_{DD}	V
V_{OL}	Output Low Voltage	I_{OI}=–1.0 mA	0		1	V
Pin Type AI: Analog Input						
V_{DC}	Input Bias Offset		V_{REF} –15	V_{REF}	V_{REF} +15	mV
V_{OFFI}	Input Offset (Differential)		–20	0	+20	mV
I_L	Input Current		–100	–	100	µA
C_{IN}	Input Capacitance		–	10	–	pF
R_{IN}	Input Resistance		–	20	–	KΩ
Pin Type AO: Analog Output						
V_O	Analog Output Voltage		V_{REF} –1.163	V_{REF}	V_{REF} +1.163	mV
V_{OFF}	Output DC Offset		V_{REF} –40	V_{REF}	V_{REF} +40	mV
V_{OFFO}	Output DC Offset (differential)		–40	0	+40	mV
R_O	Output Resistance		–	0.8	–	Ω
C_O	Output Capacitance		–	10	–	pF

DC CHARACTERISTICS (Continued)

Table 4. TDC Pin Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Units
Z_I	Load Impedance		400	600	Infinite	Ω
Pin Type PWR: Power and Ground						
V_{DD}	Digital Supply Voltage	Voltage	4.75	5	5.25	V
GND	Digital Ground		–	–	0	–
AV_{DD}	Analog Supply Voltage		V_{DD}	V_{DD}	V_{DD}	V
AGND	Analog Ground		GND	GND	GND	V
I_{DD1}	Digital Supply Current	Operating	–	45	90	mA
I_{ADD1}	Analog Supply Current	Operating	–	5	10	mA
I_{DD2}	Digital Supply Current	Sleep Mode	–	20	100	µA
I_{ADD2}	Analog Supply Current	Sleep Mode	–	5	25	µA

AC CHARACTERISTICS

Timing Diagrams

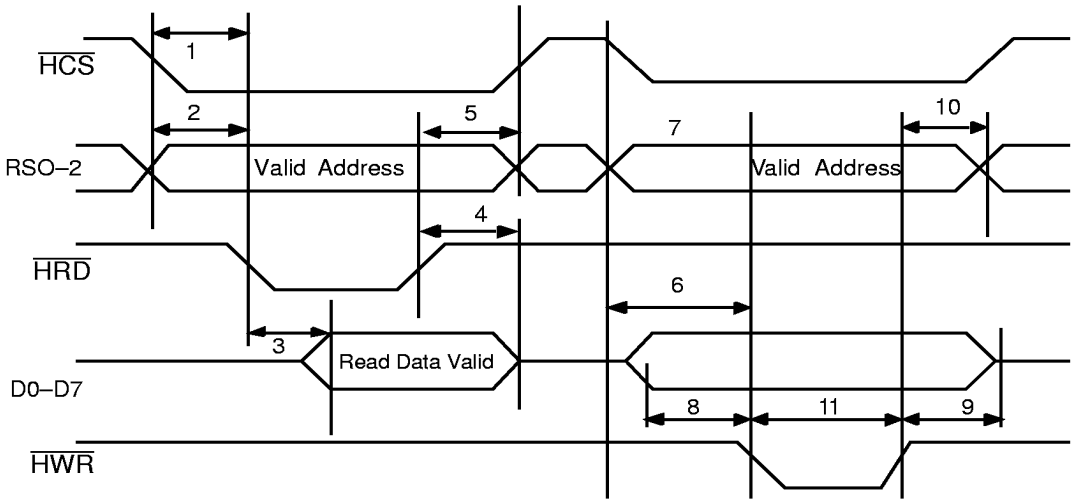


Figure 4. Microprocessor Interface Read/Write Diagram

Table 5. Microprocessor Interface Timing

Description					
Read Timing	**Parameter**	**Min**	**Typ**	**Max**	**Units**
HA0–2 & $\overline{HCS}$ to $\overline{HRD}$ Setup Time	1	0	–	–	ns
HA0–2 to $\overline{HRD}$ Setup Time	2	0	–	–	ns
$\overline{HRD}$ to Data Access Time	3	–	25	85	ns
$\overline{HRD}$ Data Hold	4	0	10	–	ns
HA0–2 and $\overline{HCS}$ Hold From $\overline{HRD}$	5	0	–	–	ns
Write Timing					
HA0–2 & $\overline{HCS}$ to $\overline{HWR}$ Setup Time	6	70	–	–	ns
$\overline{HCS}$ to $\overline{HWR}$ Setup Time	7	70	–	–	ns
Data to $\overline{HWR}$ Setup Time	8	50	–	–	ns
$\overline{HWR}$ Data Hold	9	10	–	–	ns
HA0–2 and $\overline{HCS}$ Hold from $\overline{HWR}$	10	10	–	–	ns
$\overline{HWR}$ Pulse Width	11	25	–	–	ns
Reset Timing					
Reset Pulse Width		1.0	–	–	us
Reset Rise Time			–	100	ns

DC CHARACTERISTICS (Continued)

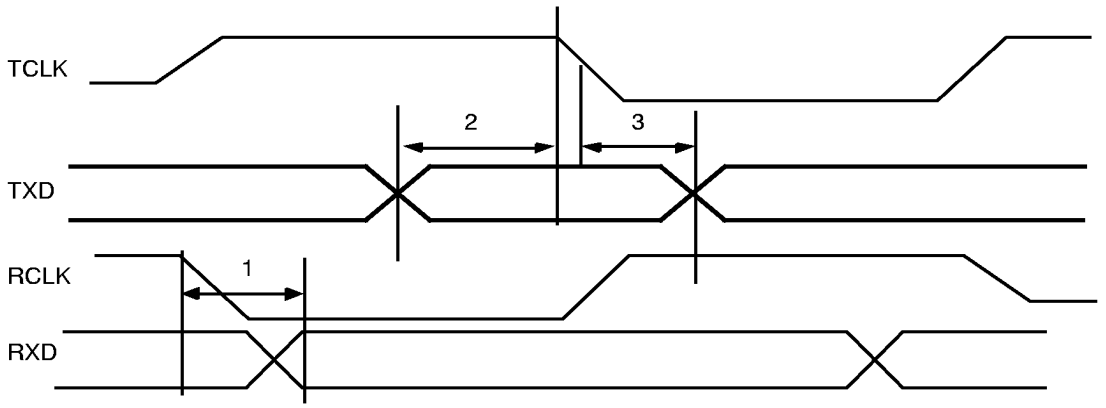


Figure 5. Serial Port Timing Diagram

Table 6. Serial Interface Timing

Description	Parameter	Min	Typ	Max	Units
RXD Data Valid Delay Time	1	–	12	–	ns
TXD Data Setup Time	2	100	–	–	ns
TXD Data Hold Time	3	100	–	–	ns

Timing Diagrams

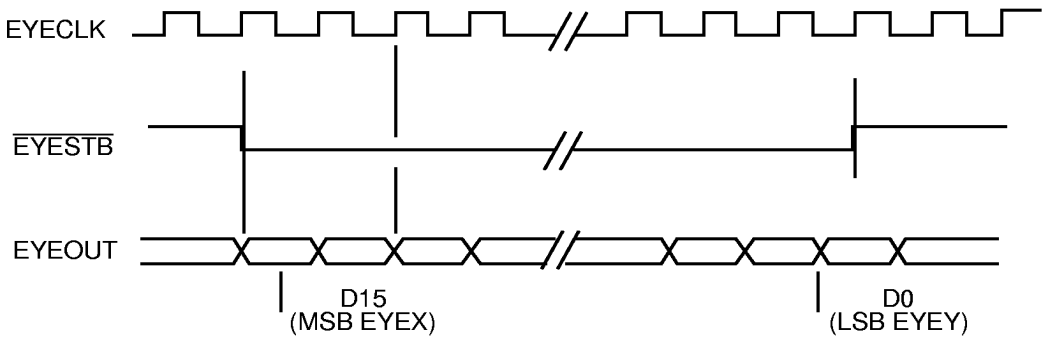


Figure 6. Eye Pattern Port Timing Diagram

Table 7. Analog Characteristics Table

Description	Parameter	Min	Typ	Max	Units
Input impedance of transformer interface	1	400	1200	–	Ω
3 dB point of transformer interface	2	21	26.5	32.5	kHz
External integration capacitance Type NPO (COG)	3	73	82	90	pF

ANALOG INPUTS: TYPE AI

AC Characteristics	Sym	Min	Type	Max	Units
Input Impedance (DC to V_{REF})	Z_{IN}	15K	25K	–	Ω
Power Supply Rejection	P_{SRRi}	40	–	–	dB
Input Current	I_i	–80	–	80	µA
Idle Channel Noise (3950 Hz Bandwidth)	I_{CNi}	–	–	–72	dBm
Signal to Distortion	S_{TDi}	30	–	–	dB

These characteristics below are provided for information only. They are not tested except in the functional test vectors.

Characteristics	Sym	Min	Typ	Max	Units
Input Capacitance	C_{IN}	–	10	–	pF
Input Bias	V_{DCOFF}	–	+2.5	–	V
Analog Input Voltage (peak differential), (23)	V_{PKI}	–2.362	–	+2.362	V
Analog Input Voltage (per RXI+. RXI– pin)	V_{PKIP}	–1.181	–	+1.181	V

ANALOG OUTPUTS: TYPE A0

AC Characteristics	Sym	Min	Type	Max	Units
Power Supply Rejection	P_{SRRO}	40	–	–	dB
Signal to Distortion	S_{TD0}	35	–	–	dB
Idle Channel Noise (3950 Hz Bandwidth)	I_{CNO}	–	–	–72	dBm
Out of Band Noise	N_{qo}				dBm
4–8 kHz	–	–	–20		dBm
8–12 kHz	–	–	–40		dBm
12 kHz and above in 4 kHz bandwidths	–	–	–55		dBm

Characteristics	Sym	Min	Typ	Max	Units
Output Impedance	Zout	–	0.80	–	Ω
Output Capacitance	Cout	–	10	–	pF
Analog Output Voltage (peak differential), (24)	Vpko	–2.375	–	+2.375	V
Load Impedance (25)	Zl	400	600	–	–

PIN FUNCTIONS

HD7–HD0 *Host Data Bus* (Bidirectional, Active High). HD0–HD7 constitutes an 8-bit bidirectional data bus used for the transfer of control and status information.

$\overline{\text{HCS}}$ *Host Chip Select* (Input, Active Low). When **$\overline{\text{CS}}$** is low, data transfer between the data pump and the host is enabled. Data transfers to the data pump registers are 8 bits wide.

$\overline{\text{HWR}}$ *Host Write Enable Strobe* (Input, Active Low). The write enable strobe is an active low signal that is used to initiate a write operation to the data pump. During a write operation, data is sent to the data pump by the controller via the host data bus.

$\overline{\text{HRD}}$ *Host Read Enable Strobe* (Input, Active Low). The read enable strobe is an active low signal that is used to initiate a read operation from the data pump. During a read operation, data is transferred out of the data pump by the controller via the host data bus.

$\overline{\text{HIRQ}}$ *Host Interrupt Request* (Output, Active Low). The $\overline{\text{HIRQ}}$ is an open-drain output that can be tied through an external pull-up resistor to the digital power supply V_{DD}. The $\overline{\text{HIRQ}}$ active low data pump output can be activated when the controller selects this option or requests by setting the RXIE or TXIE bits in the data pump Host Register. This pin can be connected to the host interrupt request pin to initiate controller service.

$\overline{\text{RESET}}$ *Reset* (Input, Active Low). The $\overline{\text{RESET}}$ signal places the device into its reset state.

HA2–HA0 *Host Address* (Input, Active High). These three register select lines (pins) are used for addressing the "controller accessible" internal registers of the data pump. When $\overline{\text{HCS}}$ is active, the state of the HA2–HA0 is used as the internal data pump interface register address. HA2 is the most significant bit; HA0 is the least significant bit.

$\overline{\text{RLSD}}$ *Receive Line Signal Detect* (Output, Active Low). Indicates when an input signal has been detected.

RXD *Receive Data* (Output). The data pump serial receive data is presented by the data pump to the local DTE on the RXD output.

TCLK *Transmit Serial Data Clock* (Output). The serial data output clock is a synchronous data clock used to transfer serial data via V.24 compatible serial interface between the data pump and the controller. The clock frequencies are 2400, 1200 Hz, 300 Hz corresponding to all the supported data bit rates.

TXD *Transmit Data* (Input). The data pump accepts the serial transmit data from the local DTE on the TXD input when the data pump is Configured to the serial transmit data mode. Serial transmit data mode is selected when the TDPM bit (b4) of the RAM control/data pump Status register (reg 6) is reset to 0.

$\overline{\text{OH}}$ *Off Hook Relay Control* (Output, Active Low). This pin is activated to drive a relay which engages the modem with the phone line. (Modem equivalent of picking up the receiver).

$\overline{\text{RTS}}$ *Request To Send* (Input, Active Low). The logical or of this pin and the RTSP bit (Reg 4.3) determines the data pump mode of operation. When the result of the logical or of these two bits is logic 1 then the data pump is in transmit mode at the selected speed else the data pump is in receive mode. In standby mode the state of this pin is a don't care.

EYECLK *Eye Pattern Clock* (Output, Active High). Data is valid at the rising edge of clock. The EYECLK can be used to clock an external D/A converter shift register for eye pattern display.

EYEOUT *Eye Pattern Data* (Output, Active High). Serial 16-bit eye pattern output data. First 8-bits is the EYEX data and the next 8-bit data is the EYEY data. This data can be used for display on an oscilloscope X and Y-axis following D/A conversion.

EYESTB *Serial Eye Pattern Strobe* (Output, Active High). This signal can be used for loading an external D/A converter.

TXO+ *Transmit Differential Analog Output Positive* (Analog Output). The TXO+, TXO– is capable of driving a 600Ω resistive load over a leased line or public switched telephone network via a Data Access Arrangement (DAA).

TXO– *Transmit Differential Analog Output Negative* (Analog Output). The TXO–, TXO+ is capable of driving a 600Ω resistive load over a leased line or public switched telephone network via a Data Access Arrangement (DAA).

RXI– *Receive Differential Analog Input Negative* (Analog Input).

RXI+ *Receive Differential Analog Input Positive* (Analog Input).

PIN FUNCTIONS (Continued)

TEST1 *Test Pin 1* (Input, Active High). This is a test pin and must be tied to digital ground.

TEST2/RCLK *Test Pin 2, Receive Data Clock* (Output, Active High). This is a test pin and must be tied to digital ground through a pull-down resistor. The resistor should be low enough to ensure this pin floats below 0.8V when the part is in the reset state. After reset, this pin becomes the Receive Data Clock Output. The resistor should be high enough such that the output can be driven to logic "1". This is a synchronous data clock used to transfer serial data via V.24 compatible serial interface between the data pump and the controller. The clock frequencies are 2400, 1200 Hz, 300 Hz corresponding to the supported data bit rates.

Vref *Reference Voltage* (Output, Active High). An internally generated reference voltage.

XTAL *Crystal Oscillator Output* (Output, Active High). The data pump chip can be connected to an external crystal circuit consisting of 24.576 MHz parallel resonant crystal with a resistor and two capacitors.

EXTAL *Crystal Oscillator Input* (Input, Active High). The data pump chip can be connected to an external circuit consisting of a 24.576 MHz parallel resonant crystal with a resistor and two capacitors.

CF1 and CF2 *Integration Capacitor PINS 1 and 2* (Analog Input). Connect an 82pF capacitor between CF2 and CF1 to complete the internal feedback integration filter for improved analog A/D performance.

GND *Digital ground*–0 volts.

V_{DD} *Digital Power*–5 volts.

AV_{DD} *Analog Power*–5 volts

AGND *Analog Ground*–0 volts.

HARDWARE INTERFACE SIGNALS

The Z02201 interface consists of the V.24 compatible Serial Interface Port, 8-bit Host Microprocessor Interface, Eye Pattern Interface, Voice Band AFE, System Signals, and Overhead Signals. The Z02201 functional hardware signals diagram is shown in Figure 7. Any signal that is active low is represented by a slash before the signal name.

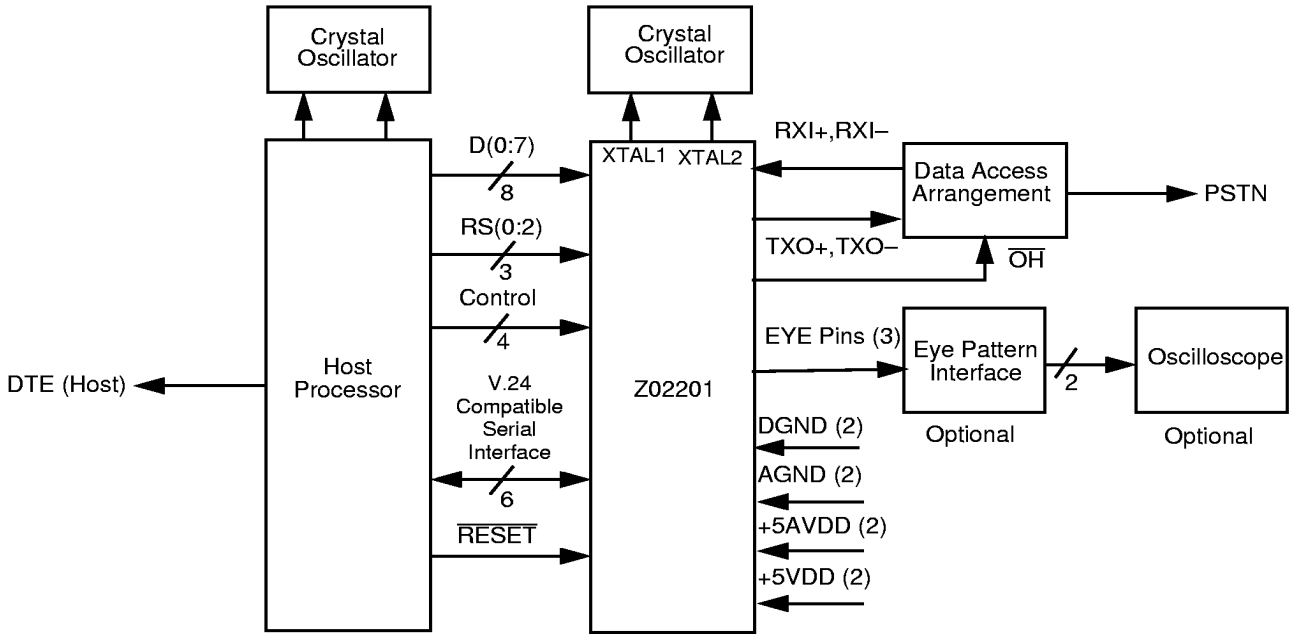


Figure 7. Modem Functional Interconnect Diagram

V.24 Compatible Serial Interface Port

The V.24 compatible Serial Interface Port provides no parallel-to-serial/serial-to-parallel conversion hardware. The V.24 compatible serial interface port consists of 7 signal pins:

Pin	Signal Name
TxD	Transmit Data
RxD	Receive Data
$\overline{RTS}$	Request To Send
$\overline{RLSD}$	Receive Line Signal Detect
TCLK	Transmit Data Clock
RCLK	Receive Data Clock

Host Port Interface

The host parallel port interface consists of 15 signal pins: 8-bit bidirectional data bus pins (HD7–HD0), 3-bit Address bus (HA2–HA0), 4 control lines, which include the Host Read ($\overline{HRD}$), Host Write ($\overline{HWR}$), Host Chip Select ($\overline{HCS}$) and Host Interrupt Request ($\overline{HIRQ}$). Multiple interrupt sources are provided in the Z02201, each of which can be masked under host control.

The host parallel interface allows the host access to data pump RAM address and data bits, transmit and receive data, RAM control and status bits, and read data pump status bits. The host can access eye pattern functions, generate transmit and receive tones and access adaptive equalizer coefficients in modem-type applications.

The host parallel interface is compatible with standard 8bit microprocessors, which include theZ8 and Z80 bus.

Eye Pattern Interface

The eye pattern interface consists of 3 pins; Eye Pattern Data (EYEOUT), Eye Pattern Clock (EYECLK), and Eye Pattern Strobe (EYESTB). Sixteen bits of data are serially transmitted via EYEOUT, under control of EYESTB and EYECLK. The first byte is the X-coordinate and the second byte is Y-coordinate of the sample. The least significant bit is presented first for both X and Y coordinate. A schematic of an eye pattern circuit is found in Figure 13 at the end of this specification.

HARDWARE INTERFACE SIGNALS (Continued)

The Eye Pattern Data, EYEOUT outputs a serial bit stream containing data for display of the eye pattern on an oscilloscope after D/A conversion. Eight bits of the X-axis data and eight bits of the Y-axis are output as a single sixteen bit data stream with the X-axis data first. EYEOUT is synchronous with the rising edge of EYECLK. EYEOUT is valid only while the EYESTB is low. Data is shifted out MSB first.

Data on eyeout is shifted out on each rising edge of the 1.536 MHz EYECLK. EYEOUT data is valid on the following edge of the Eye Pattern Clock, EYECLK.

The EYEOUT data is valid when the Eye Pattern Strobe, EYESTB is low. EYESTB changes state on the rising edge of EYECLK.

TECHNICAL SPECIFICATIONS

Configurations and Data Rates

The Z02201 can be Configured to any of the V.22bis operation modes. Table 7 provides the selectable options, the supported data rate as well as baud rate and the frequency to be modulated for the Z02201.

Tone Generation and Tone Detection

The Z02201 provides comprehensive and flexible tone generation and detection. This includes all tones needed to establish a circuit connection and to setup and control a communication session. The tone generation furnishes the DTMF tones for PSTN auto dialing, and the supervisory tones for call establishment. The tone detection provides support for call progress monitoring. The detector can also be user-programmed to recognize up to 16 tones.

Data Encoding

The data encoding for the Z02201 meets ITU–T recommendations as well as Bell standards.

Table 8. Selectable Configurations

Configuration	Modulation	Carrier Freq.	Data Rate (bps)	Symbol Rate (baud)	Bits Per Symbol	Constellation Points
V.22 bis 2400	QAM	1200/2400	2400	600	4	16
V.22 bis 1200	DPSK	1200/2400	1200	600	2	4
V.22 1200	DPSK	1200/2400	1200	600	2	4
V.23 1200/75	FSK	1700/420	1200/75	1200/75	1	–
V.21	FSK	1080/1750	300	300	1	–
Bell 212A	DPSK	1200/2400	1200	600	2	4
Bell 103	FSK	1170/2125	300	300	1	–

Notes:
1. Configuration is selected through the RAM location Config.
2. QAM=Quadrature Amplitude Modulation FSK=Frequency Shift Key
3. Tone=Single or Dual Tone (DTMF), TM=Trellis Modulation, DPSK=Dual Phase Shift Keying

TRANSMITTED DATA SPECTRUM

The transmitted data spectrum with compromised equalization disabled is shaped in the baseband by the finite impulse response (FIR) filter. Table 9 reflects the spectrum characteristics.

Table 9. Spectral Shaping

Mode	Carrier Freq	Spectral Power Shaping Function
V.22	1200	sqrt 75% Raised Cosine at 600 baud
V.22bis	2400	sqrt 75% Raised Cosine at 600 baud

Note: The carrier and the spectral shaping are selected automatically according to the Configuration.

TRANSMIT LEVELS

The transmit output level of the Z02201 is programmable in 1dBm decrements from –6dBm to –43dBm with a default value of –10dBm when measured differentially across pins TX0+ and TX0– with a sinusoidal waveform.

Note: To avoid saturation in high speed data mode, the transmit level should be set to –6dBm or lower by the host. If a higher transmit level is required, it can be accomplished using external op amps.

RECEIVER LEVELS

The timing recovery circuit can track a ±0.01% (100 ppm) frequency error in the associated transmit timing source with less than 1.0 dB degradation in performance.

Clamping
Received Data (RXD) is clamped to a constant mark whenever $\overline{\text{RLSD}}$ is off.

Carrier Recovery
The recovery circuit can track a ±7 Hz frequency offset in the receiver carrier with less than 1.0 dB degradation in performance.

SOFTWARE INTERFACE

The host microprocessor communicates with the Z02201 via the parallel microprocessor bus interface. Access is provided to a set of eight 8-bit Interface Registers, and through these registers, to Z02201 RAM memory locations. This interface allows the host to request modem status information and receive data, control the Configuration, and load data for transmit. Table 10 is the Parallel Interface Register map.

Table 10. Interface Register Map

Function	Register Number	RS2–0 b2b1b0	MSB* Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB** Bit 0	Access Method
RAM Access low	0	000	RAMDL								R/W
RAM Access high	1	001	RAMDH								R/W
RAM Access Address	2	010	RAMAL								W
Parallel Data	3	011	DATAP								R/W
RAM Control & Status	4	100	TXIE	RXIE	RAMIE	TPDM	RTSP	RAMRW	RAMRQ	RAMAH	R/W
Modem Status	5	101	TXI	RXI	RAMI	DPBUSY	Reserved	RTRND	CDET	RES	R
HDLC	7	111	0	0	0	0	0	TEND	RXERR	EOF	R/W

Microprocessor Interface Register and Bit Definitions:

Reg0, Reg1 RAMDL, RAMDH: DATA PUMP RAM DATA REGISTERS. RAMDL is the least significant byte, RAMDH is the most significant byte. After a data pump RAM read operation has completed, these registers contain the requested data. When a data pump RAM write operation is started, these registers contain the data written to data pump RAM.

Reg2 RAMAL: DATA PUMP RAM DATA ADDRESS. When a data pump RAM read or write operation is started, this byte contains the lower 8 bits of the RAM address. Register Reg4.RAMAH is the high bit of the RAM address.

Reg3 DATAP: DATA PUMP PARALLEL DATA. This register contains data transferred to or from the remote modem during parallel modem (see register Reg4.TPDM). Upon any reset, and when Config.MODE=0 (standby), the data pump places its firmware version number in register DATAP.

SOFTWARE INTERFACE (Continued)

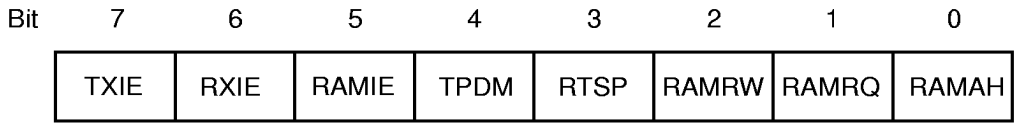


Table 11. REG4: RAM Control Register

SYMBOL	POSITION	NAME AND DESCRIPTION
RAMAH	REG 4.0	**RAM Address High Bit**. This is the most significant bit of the data pump RAM address. This bit should be set to 1 when accessing a data pump RAM address that is greater than 255 else this bit should be set to 0.
RAMRQ	REG 4.1	**Data Pump RAM Access Request Bit**. Set this bit to 1 to request a read or write of the data pump RAM. The data pump will set this bit to 0 when the request has been fulfilled.
RAMRW	REG 4.2	**Data Pump RAM Read/Write Bit**. Set this bit to 0 to request a read of data pump RAM; 1 to request a write of data pump RAM.
RTSP	REG 4.3	**Register Request to Send Bit**. This bit is OR'd with the hardware RTS signal received by the data pump on its $\overline{RTS}$ pin. The host uses either $\overline{RTS}$ or RTSP=1 to inform the data pump the host is transmitting data. To control the data pump using the $\overline{RTS}$ signal, set RTSP to 0. To control the data pump using RTSP, hold $\overline{RTS}$ high.
TPDM	REG 4.4	**Select Parallel Data Mode**. Setting this bit selects the parallel data mode. Resetting it selects the serial data mode.
RAMIE	REG 4.5	**RAM Interrupt Enable Bit**. Setting this bit will allow the data pump to interrupt the host when a RAM read/write request has been completed.
RXIE	REG 4.6	**Receive Data Interrupt Enable Bit, Parallel Data Mode Only**. This bit, when set, will cause the data pump to generate an interrupt whenever the RXI bit is set.
TXIE	REG 4.7	**Transmit Data Interrupt Enable Bit, Parallel Data Mode Only**. This bit, when set, will cause the data pump to generate an interrupt whenever the TXI bit is set.

Note: All the bits in this register (REG 4) default to logic 0 upon power-up or after reset sequences are completed.

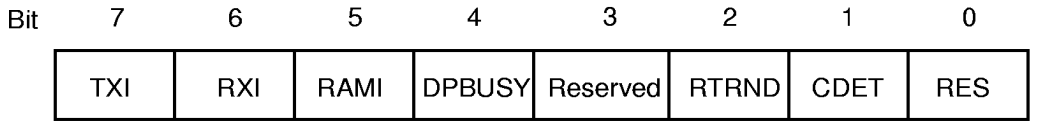


Table 12. REG5: Data Pump Status Register

SYMBOL	POSITION	NAME AND DESCRIPTION
RES	REG 5.0	**Data Pump in RESET Mode**. This bit is set whenever the data pump is in RESET mode due to a hardware reset or power-on, and sets RES=0 when it completes reset.
CDET	REG 5.1	**Carrier Detect**. The data pump sets CDET=1 when it enters any data mode and is ready to transmit data. The data pump sets CDET=0 during retrains (see Reg5.RTRND) and when no signal is detected from the remote modem. See locations RLSDOnThresh and RLSDOffThresh for more information. CDET is inverted and reflected on the data pump's $\overline{\text{RLSD}}$ pin, so if CDET=1, $\overline{\text{RLSD}}$ is low (asserted). Upon any reset, or when the host sets Config.MODE=0 (standby) the data pump sets CDET=0.
RTRND	REG 5.2	**Retrain Detect, 2400 bps (V.22bis data modem only)**. Retrain sequence detected when this bit is set. The data pump has detected a retrain request sequence from the remote modem.
DPBUSY	REG 5.4	**Data Pump Busy**. This bit is set whenever the data pump starts transmitting data. When the link is to be terminated, setting RTSP to 0 will cause this bit to be reset after the data pump has finished transmitting the last of the data in its internal buffers. When this bit has been reset, it is safe to set Config. MODE to standby mode (0) and hang up the telephone, thus terminating the connection. It also indicates when digits are being dialed during timed dialing operation. Upon any reset, or when the host sets Config.MODE=0 (standby) the data pump sets DPBUSY=0. This bit is not valid during HDLC operation.
RAMI	REG 5.5	**Data Pump RAM Interrupt Status**. This bit is set when the data pump has processed a RAM read/write request.
RXI	REG 5.6	**Receive Interrupt Status**. This bit is set when the data pump is in parallel data transfer mode (TPDM=1) and the data pump has written a new octet to the DATAP register. A read from the DATAP register will clear this bit.
TXI	REG 5.7	**Transmit Interrupt Status**. This bit is set when the data pump is in parallel data transfer mode (TPDM=1) and the data pump has read the DATAP register. A write to the DATAP register will clear this bit.

Note: The RXI bit is set to logic 1 after the reset sequences. All other bits in this register (REG 5) default to logic 0 upon power up or after reset sequences are completed.

SOFTWARE INTERFACE (Continued)

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	TEND	RXERR	EOF

Table 13. REG7: HDLC Register.

SYMBOL	POSITION	NAME AND DESCRIPTION
EOF	REG 7.0	**Receive End of Frame**. The data pump sets EOF=1 when an HDLC frame has been completely received, i.e., when frame data has been received and a closing HDLC flag or HDLC Abort condition is received. If the frame was correctly received, the data pump also sets Reg5.RXERROR=0, Reg5.RXI=1, and DATAP=7EH. See Reg7.RXERROR for a description of CRC errors and HDLC Aborts. EOF reflects whether the current register DATAP value indicates the end of receipt of an HDLC frame. When the first data byte of the next HDLC frame is received, or if an HDLC Abort condition is received when no HDLC frame data was being received, the data pump sets EOF=0. This may occur only 8 bit times after the data pump sets EOF=1.
RXERR	REG 7.1	**Receive Error**. If an HDLC frame contains a CRC error, or an HDLC Abort condition is received, the data pump sets RXERROR=1, Reg5.RXI=1, and DATAP=7EH or FFH. If the frame had a CRC error, DATAP=7EH. If an HDLC Abort condition was received, DATAP=FFH.
TEND	REG 7.2	**Transmit End of Frame**. The data pump sets TEND=1 when it closes an HDLC frame being transmitted. The data pump sets TEND=0 after transmitting the CRC bytes, when it starts transmitting the closing flag of the HDLC frame. The data pump closes an HDLC frame when the host does not provide data to transmit (see DATAP) in time to be included in the HDLC frame.

Note: All the bits in this register (REG 7) default to logic 0 upon power up or after reset.
All undefined bits of this register are reserved. The controller should write logical 0 to all reserved bit positions when writing this register. The controller should ignore the reserved bits when reading this register.

Reg7 Data Pump Register 7 These bits represent the state of HDLC frames when the data pump is in the HDLC framing mode. These bits are valid only if Bufctrl.HDLC=1. The host should refrain from writing Reg7 to avoid changing the values of bit fields set by the data pump. Bits not defined below are reserved or not available for use.

The host reads register Reg7 immediately after DATAP has been read.

The two CRC checksum bytes in received HDLC frames are returned as bytes of the frame.

Upon any reset, or when the host sets Config.MODE=0 (standby) the data pump sets TEND=0, RXERROR=0 and EOF=0.

RAMI, RXI, AND TXI INTERRUPTS

The 3 MS bits in the RAM Control and data pump Status Registers define the interrupt masks for RAMI, RXI and TXI. The RAMIE, RXIE, and TXIE enable bits in the RAM Control Register are logically ANDed with its corresponding interrupt bits in the data pump Status Register. The outputs are then logically ORed and drive the $\overline{HIRQ}$ pin which provides an interrupt to the host interrupt (See Figure 8).

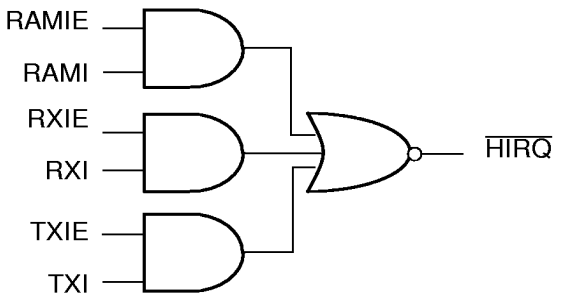


Figure 8. Host Interrupt Circuit Diagram

INTERFACE RAM

We shall use the short form **<variable name>.<bit field>** to name bits, since the actual location of some bits may not be intuitively obvious. For example, Config.MCUCTRL refers to the MCUCTRL bit in the variable Config.

The interface RAM is also used by the data pump for normal operations. Therefore all writes to the interface RAM should be of the form Read-Modify-Write where only the bits that need to be changed are changed. All undocumented bits are reserved and should be preserved.

Important Notes

1. Do not read or write data pump RAM more frequently than once every 2 msec.
2. Data pump RAM reads of writes requires approximately 0.1 msec to complete.
3. Data pump RAM writes take effect at different times depending upon the location being written to. In general, during data modes, writes take effect at the end of the next baud period. In general, during other modes of operation, writes take effect 0.1 msec.
4. Writing Reg4, for example to set Reg4.TXIE=0 in an interrupt handler, while waiting for the data pump to set Reg4.RAMRQ=0 in the background may cause unwanted side effects. Setting Reg4.RAMRQ=1 may cause the data pump to repeat the read/write request if the data pump had just set Reg4.RAMRQ=0, whereas setting Reg4.RAMRQ=0 may abort the RAM read/write request.

DATA PUMP INTERFACE RAM ACCESS METHOD

To write to data pump RAM:

1. Write data to RAMDL & RAMDH.
2. Write the address to RAMAL & RAMAH.
3. Set RAMRW to 1 and RAMRQ to 1 (can be set with RAMAH as long as RAMAL is written first).
4. Wait until RAMRQ is reset to 0 by the data pump or until RAMI=1.

To read from data pump RAM:

1. Write the address to RAMAH & RAMAL.
2. Set RAMRW to 0 and RAMRQ to 1 (can be set with RAMAH as long as RAMAL is written first).
3. Wait until RAMRQ is reset to 0 by the data pump or until RAMI=1.
4. Read data from RAMDL & RAMDH.

Reads and writes to the data pump RAM may take as much as 105us to complete.

MODEM DATA PUMP RAM MAP

Table 14. Modem Data Pump RAM Map

Mnemonic	Address (Hex)	Access Mode	Description
Config	01FF	R/W	Data pump Configuration
Trnctrl	01FE	R/W	Training Control
Bufctrl	01FD	R/W	Buffer Control
ToneStatus	01FC	R/W	DTMF and Tone Control Status
Dpctrl	01FA	R/W	Data pump Miscellaneous Controls
MStatus	01F7	R/W	Modem Control and Status
EQMMaxThresh	01F6	R/W	MSE Maximum Threshold
RLSDOffThresh	01F5	R/W	RLSD Off Threshold
RLSDOnThresh	01F4	R/W	RLSD On Threshold
CONN_Mode	01F0	R/W	Connection Speed After Handshake is Complete
DTMFh_lev	01A1	R/W	DTMF High Band Transmit Level
DTMFl_lev	01A0	R/W	DTMF Low Band Transmit Level
ToneGenA	0191	R/W	Tone Generator A
ToneGenB	0196	R/W	Tone Generator B
TxLevel	0185	R/W	Modem Transmit Level
Seq3Count	18E	R/W	Dial Timer Inter-Pulse Count
Seq2Count	18D	R/W	Dial Timer Off Count
Seq1Count	18C	R/W	Dial Timer On Count
BiquadA	0155–015E	R/W	Biquad A Coefficient
BiquadB	015F–0168	R/W	Biquad B Coefficient
DTD0–DTD15	0145–0154	R/W	Tone Detector Coefficients
EQMlev	092	R/W	Eye Quality Monitor Level
BiQuadOffThresh	052	R/W	Biquad Detectors Off Point
BiQuadOnThresh	051	R/W	Biquad Detectors On Point
DTD0Lev–DTD15Lev	026–035	R/W	Tone Detector Levels
DTDThresh	03	R/W	Tone Detector Threshold
DTDStatus	00	R/W	Discrete Tone Detector Status

INTERFACE RAM DEFINITIONS

Table 15. Modem data pump Word Definitions

Register & Address (hex)	Default Value		Function and Explanation
Config	01FF	0H	**Data pump Configuration register**
		b15	Unused. Set this bit=0.
		b14	**ORG** (Set Originate Mode: all modes) If ORG=1, then the modem is in originate mode. Otherwise, it is in answer mode. Be sure to set ORG before or at the same time as Config.MODE, not afterwards.
		b13	**ERROR** (Data Pump Error: all modes) This bit is set to 1 when the data pump detects an internal error condition such as an invalid Config code. The host should reset the data pump.
		b12	**RESERVED**
		b11	**RESERVED**
		b10	**MCUCTRL** (Manual Handshake; all data modes). Set MCUCTRL=1 to control the handshake process manually.
		b9	**RESERVED**
		b8	**SRESET** (Soft Reset: all modes) Set this bit to soft reset the data pump. The data pump sets SRESET to 0 when the software reset completes.
		b7	Unused. Set this bit=0.
		b0.6	**MODE** (Data Mode Configuration: selects a mode) Selects data pump operation mode, as follows. All modes unlisted below should be considered reserved. The host should read MODE once after writing it to allow the data pump enough time to begin operation in the new mode. Setting MODE=0 (standby) starts the idle mode of operation, not the power-saving sleep mode. The mode table follows:

Value (hex)	Data Mode specified
00	Standby
01	Transmit tones using both generators simultaneously
02	Detect tones/BiQuads using all discrete tone detectors and biquad tone detectors simultaneously
03	Dial
07	Sleep Mode
08	V.22bis 2400 bps/1200 bps mode
09	V.22 1200 bps mode
0B	Bell 212A 1200 bps mode
10	V.21 300 bps mode
11	Bell 103 300 bps mode
13	V.23 1200 bps Tx/75 bps Rx mode
14	V.23 75 bps Tx/1200 bps Rx mode

INTERFACE RAM DEFINITIONS (Continued)

Table 15. Modem data pump Word Definitions

Register & Address (hex)		Default Value	Function and Explanation
Trnctrl	**01FE**	0H	**Training Control Register**
			The data pump sets this location to its default value upon any reset and when the host sets Config.MODE=0. This RAM location controls the handshake process during a manual training process (see *Manual Handshake Procedure* for an example on the use of this interface). This RAM location has no effect once data mode is entered (Trnctrl=5 or 6).
			b7 **SB1DET**–Scrambled Binary 1 Detected (1200 bps or 2400 bps). Debounced through 30 msec.
			b6 **S1DET**–S1 Detected: debounced through 27 msec
			b5 **USB1DET**–Unscrambled Marks Detected (1200 bps) The data pump sets USB1DET=1 when it detects unscrambled marks (1200 bps, FSK modes). USB1DET is not debounced. It reflects the state of the currently received symbol.
			b4 **SB0DET**–Scrambled Binary 0 Detected (1200 bps or 2400 bps) SB0DET is not debounced. It reflects the state of the currently received symbol.
			b3 **V22BIS** Force 16 Way Decisions. Set V22BIS=1 to cause the data pump to make 16-way (V.22 Bis) instead of 4-way (V.22, BELL 212A) decisions.
			b0–2 **TXCTRL** Transmitter Control. Set TXCTRL to control the output of the data pump, using the following table as a guide. The default frequency for the transmitted tone (TXCTRL=7) is 2225 Hz, and may be changed after setting TXCTRL by changing ToneGenA appropriately. The tone level is controlled by TxLevel.

Value	V.22/Bell 212A/V.22bis Sequence Transmitted
0	Silence: squelch transmitter
1	Transmit unscrambled binary 1 at 1200 bps
2	Transmit S1 signal
3	Transmit scrambled binary 1 at 1200 bps
4	Transmit scrambled binary 1 at 2400 bps
5	Begin V.22 1200 bps
6	Begin 2400 bps data mode
7	Transmit tone

Value	FSK Sequence Transmitted
0	Silence: squelch transmitter
1	Transmit marks (binary 1)
2	Transmit spaces (binary 0)
5	Begin FSK Data Mode
7	Transmit tone

Table 15. Modem data pump Word Definitions

Register & Address (hex)		Default Value		Function and Explanation
Bufctrl	01FD	0H		**Buffer Control register** The data pump sets this location to its default value upon any reset.
			b15..b8	Set these bits=0 when setting Bufctrl.HDLC=1.
			b7	**HDLC** (Set HDLC Mode: all modes) Set HDLC mode. When parallel data transfer mode is selected (TPDM=1) and HDLC is set, the data pump will transfer data using the synchronous HDLC mode. In serial mode (TPDM=0), this bit has no effect. The host should set bits 8–15 to 0 when it sets this bit to 1.
			b3	**SCRDIS** (Scrambler Disable: V.22, V.22bis, Bell 212A) Set this bit to disable the transmitter scrambler. Takes precedence over TmCtrl.TXCTRL.
			b2	**TXMHLD** (Hold Data Pump Output to the Remote Modem to Marks: all data modes) Set this bit to force the data pump to transmit only marks to the remote modem, disregarding data received from the host.
			b1	**DSCRDIS** (Descrambler Disable: V.22, V.22bis, Bell 212A) Set this bit to disable the receiver descrambler.
			b0	**RXMHLD** (Hold Rx Output to Marks: all modes) Set RXMHLD=1 to cause the data pump to transmit only marks to the host, disregarding data received from the remote modem.

INTERFACE RAM DEFINITIONS (Continued)

Table 15. Modem data pump Word Definitions

Register & Address (hex)	Default Value		Function and Explanation
ToneStatus 01FC	080H		**Biquad Tone Detector Control and Status, Dial Control** The data pump sets this location to its default value upon any reset.
		b15	**TONEA** (Tone A detected) The tone frequency programmed in biquad detector A has been detected if this bit is set. TONEA is reset when the host sets Config.MODE=2.
		b14	**TONEB** (Tone B detected) The tone frequency programmed in biquad detector B has been detected if this bit is set. TONEB is reset when the host sets Config.MODE=2.
		b13	**Cascade biquad tone detectors A & B** The two 4th order biquad filters can be cascaded to form a single 8th order filter if this bit is set by the host. The result of the cascaded biquad tone detector is available in ToneStatus.TONEA.
		b7	**TONEDIAL** (Use DTMF to dial) This bit tells the data pump to use DTMF tone dialing when in dialing mode (Config.MODE=3).
		b5	**SQRDIS** (Squarer disable) Set SQRDIS=1 to cause the data pump to provide the output of biquad detector A directly to the input of biquad detector B, without first squaring it. SQRDIS is valid only when the biquad tone detectors are cascaded (see ToneStatus.CASCADE).
		b4	**TIMEDIAL** (Timed Dialing) Set TIMEDIAL=1 to cause the data pump to generate timed DTMF tones or pulse dialing. If TIMEDIAL=0, continuous dialing is used.
		b0–b3	**DIAL DIGIT** The DTMF digit to be dialed is set here before Config is set for DTMF transmit. See the following table to determine how to set this parameter. For pulse dialing, only digits 0 through 9 are valid:

Table 15. Modem data pump Word Definitions

Register & Address (hex)	Default Value	Function and Explanation
ToneStatus 01FC	080H	**Biquad Tone Detector Control and Status, Dial Control** The data pump sets this location to its default value upon any reset.

Digit	Value
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
*	10
#	11
A	12
B	13
C	14
D	15

INTERFACE RAM DEFINITIONS (Continued)

Table 15. Modem data pump Word Definitions

Register & Address (hex)		Default Value		Function and Explanation
Dpctrl	01FA	0H		**Data Pump Miscellaneous Controls** Do not modify this location during automatic handshake or retrain. The data pump sets this location to its default value upon any reset.
			b15	**TXSQLCH** (Squelch Transmitter: all modes)
			b14	**AGCFRZ** (Freeze Autogain Control: V.22/V.22bis/Bell 212A) Set to 1 to freeze AGC adaptation.
			b13	**Reserved** for internal use. Set to 0 when Dpctrl is written by the host.
			b12	**Reserved** for internal use. Set to 0 when Dpctrl is written by the host.
			b10–11	**LEQTYPE** (Link Equalizer Type) Set LEQTYPE to 0 for a flat line equalizer, or LEQTYPE to 1 for a 3002 line equalizer.
			b9	**GTEN** (Guard Tone Enable: V.22/V.22bis/Bell 212A) This bit controls whether a V.22/V.22bis/Bell 212A link is made with a guard tone or not. If it is set, a guard tone is transmitted along with the carrier. Must not be enabled in modes other than V.22, V.22bis, and Bell 212A! This bit must be set prior to selecting the mode in Config. The frequency of the guard tone is selected by Dpctrl.GTSEL.
			b8	**GTSEL** (Guard Tone Select: V.22/V.22bis/Bell 212A) This bit selects the guard tone frequency. 0=550 Hz, 1=1800 Hz. This bit must be set prior to selecting the mode in Config.
			b4	**EQE** (Equalizer EQM > threshold in data pump RAM: V.22/V.22bis/B212A: all modes) Set to 1 when EQM exceeds the threshold set in data pump RAM.
			b3	**EQFRZ** (Freeze Equalizer: all modes) Set to 1 to freeze adaptive equalizer (AEQ) adaptation. AEQ coefficients are lost when a mode change (in Config) occurs.
			b2	**TSPACE** (Select T-spaced vs. T/2-spaced Equalizer: V.29) This bit, when set, selects a T-spaced AEQ. When reset, it selects a T/2 spaced AEQ. V.22/V.22bis/Bell 212A modes always use a T/2-spaced equalizer.

Table 15. Modem data pump Word Definitions

Register & Address (hex)		Default Value		Function and Explanation
MStatus	01F7	0H		**Modem Control and Status** The data pump sets this location to its default value upon any reset.
			b11	**RETRAIN** (Force a Retrain: V.22bis) This bit, when set will force a retrain if the data pump has a V.22bis connection. The CDET (Register 5 bit 1) bit will be set to 0 when the retrain has begun. The CDET bit will be set to 1 when the retrain has been completed. The data pump sets RETRAIN=0 when retrain begins and when the host sets Config.MODE to any data mode.
			b2	**OFFHOOK** (Enable Off-hook Relay) The data pump sets the $\overline{OH}$ signal to the inverted value of this bit. For example, when OFFHOOK=1, the data pump sets $\overline{OH}$ low. When $\overline{OH}$ is low, the off-hook relay should be closed so the signal from the telephone line is presented to the data pump. The data pump sets OFFHOOK to 1 when the host sets Config.MODE to 3 (dial), or to any data mode. The data pump sets OFFHOOK to 0 upon any reset. Modify OFFHOOK only when Config.MODE=0 (standby) to avoid interference with the data pump's use of this bit.
EQMMaxThresh	01F6	400H		**EQM Maximum Threshold** This is the upper acceptable limit for the Eye Quality Monitor (EQM). During V.22, V.22bis or Bell 212A data mode, when EQMlev exceeds EQMMaxThresh, the data pump sets Dpctrl.EQE to 1. The data pump sets this location to its default value upon any reset. Changes in value take effect at the end of the next baud period.
RLSDOffThresh	01F5	–48 dBm		**Received Line Signal Detect "off" Threshold**
RLSDOnThresh	01F4	–43 dBm		**Received Line Signal Detect "on" Threshold** The upper and lower thresholds of the received telephone line energy. If Reg5.CDET=1 and the telephone line energy falls below RLSDOffThresh then the data pump sets Reg5.CDET=0. If Reg5.CDET=1 and the telephone line energy rises above RLSDOnThresh then the data pump sets Reg5.CDET=1. These thresholds stabilize Reg5.CDET by hysteresis when RLSDOffThresh is set to a lower value than RLSDOnThresh. Use the formula $$RLSDval = 10^{(thresh)/20} \cdot 32767$$ where thresh is specified in dBm and less or equal to 0. The data pump sets this location to its default value upon any reset. Changes in value take effect after the next baud period.

INTERFACE RAM DEFINITIONS (Continued)

Table 15. Modem data pump Word Definitions

Register & Address (hex)		Default Value	Function and Explanation
CONN_Mode	01F0	—	**Connection Mode Register** The data pump sets this location to its default value upon any reset. This RAM location reports the connection type and speed established after handshake is completed. The values for this location are the same as those for Config.MODE:

Value (hex)	Data mode specified
08	V.22bis 2400 bps mode
09	V.22 1200 bps mode
0B	Bell 212A 1200 bps mode
10	V.21 300 bps mode
11	Bell 103 300 bps mode
13	V.23 1200 bps Tx/75 bps Rx mode
14	V.23 75 bps Tx/1200 bps Rx mode

DTMFh_lev	01A1	–6 dBm	**DTMF Transmit Level—High Band**
DTMFl_lev	01A0	–9 dBm	**DTMF Transmit Level—Low Band**

These are the transmit levels for the DTMF low band (DTMFl_lev) and DTMF high band (DTMFh_lev) frequencies. The levels are set by the formula

$$\mathrm{DTMFlev} = 10^{(\mathrm{lev})/20} \cdot 32767$$

where lev is specified in dBm and less or equal to 0. Change in value takes effect in 0.1 msec. The data pump sets these locations to their default values upon any reset.

Table 15. Modem data pump Word Definitions

Register & Address (hex)		Default Value	Function and Explanation
ToneGenA	0191	—	**Tone Generator A**
ToneGenB	0196	—	**Tone Generator B**
			The data pump has two independent tone generators, each simultaneously generating a pure tone with its own transmit level when Config.MODE=1 (transmit tones). The outputs of the tone generators are mixed together. The generated frequencies are set by writing a coefficient to location ToneGenA or ToneGenB. The coefficient is defined as: $$\text{coeff}_x = \frac{2\pi \cdot f}{9600} \cdot 4096$$ where f is the frequency of the tone to be generated. The transmit levels for tone generators A and B are set in locations DTMFl_lev and DTMFh_lev, respectively. See "Transmitting Tones" for more information including a description of setting the tone transmission levels.
TxLevel	185	–10 dBm	**Transmit Power Level**
			Sets the transmit power level. Use the formula $$\text{TxLevel} = 10^{(\text{power})/20} \cdot 2048$$ where power is specified in dBm and less than or equal to –6. Change in value takes effect at the end of each baud period.

INTERFACE RAM DEFINITIONS (Continued)

Table 15. Modem data pump Word Definitions

Register & Address (hex)		Default Value	Function and Explanation	
Seq3Count	18E	None	**Dial Timer Inter-Pulse Count**	See Seq1Count.
Seq2Count	18D	95 msec	**Dial Timer Off Count**	See Seq1Count.
Seq1Count	18C	95 msec	**Dial Timer On Count**	
			Seq1Count, Seq2Count and Seq3Count are timer counts in units of 1/9600 of a second, for DTMF and pulse dialing. For DTMF dialing, Seq1Count is the length of the digit on-time, and Seq2Count is the length of the digit off-time. For pulse dialing, Seq1Count is the length of the break period, Seq2Count is the length of the make period, and Seq3Count is the length of the pause after dialing a digit. The data pump sets these locations to their default values when the host sets Config.MODE=3 (dial).	
Biquad A Coefficients	0155–015E	—	**Biquad A and B Coefficients**	
Biquad B Coefficients	015F–0168	—		
			These locations program the frequency range for the biquad filters. The coefficients are in the following order: b2, b1, a3, a2, a1, B2, B1, A3, A2, A1. See the section on Call Progress Monitoring Using BiQuad Tone Detectors for more information.	
DTD0–DTD15	0145–0154	—	**Tone Detector Coefficients**	
			These locations set the tone detector coefficients for the 16 detectors in the system. The coefficients are set by using the following formula: $$\text{coeff}_{\text{tone}} = \cos\left(\frac{2\pi \cdot f_{\text{tone}}}{9600}\right) \cdot 32767$$ See the section on Tone Detectors for more information.	
EQMlev	092	—	**Eye Quality Monitor (EQM)**	
			Provides a measure of line quality during V.22, V.22bis, or Bell 212A, and is computed as a running average of the mean square error (MSE) of the received point and the decision point. When EQM exceeds EQMlev, Dpctrl.EQE is set to 1; otherwise, it is set to 0.	

Table 15. Modem data pump Word Definitions

Register & Address (hex)	Default Value	Function and Explanation
BiQuadOffThresh 052	–42 dBm	**Biquad Tone Detectors "off" Point** The data pump sets this location to its default value when Config.MODE is set to 2 by the host.
		This location can be used to set the off point for the Biquad filter detection routines. If the power level is below this value, the detector will turn off the detection status bit. Use the following formula to set the threshold: $$\text{Threshold} = 10^{(\text{level})/20} \cdot 32767$$ where level is in dBm. The data pump sets this location to its default value when the host sets Config.MODE=2 (detect tones).
BiQuadOnThresh 051	–35 dBm	**Biquad Tone Detectors "on" Point** The data pump sets this location to its default value when Config.MODE is set to 2 by the host.
		This location can be used to set the on point for the Biquad filter detection routines. If the power level is above this value, the detector will turn on the detection status bit. Use the following formula to set the threshold: $$\text{Threshold} = 10^{(\text{level})/20} \cdot 32767$$ where level is in dBm. The data pump sets this location to its default value when the host sets Config.MODE=2 (detect tones).
DTD0Lev–DTD15Lev 26–35	—	**Discrete Tone Detector Levels**
		These locations represent the tone detector levels when in Tone Detect mode (Config.MODE=002H). They may be used by the host to determine which tone is dominant if multiple tones are detected. These locations have no default.
DTDThresh 03	–24 dBm	**Discrete Tone Detector Threshold**
		This location programs the threshold for all the tone detectors. Any signal whose signal strength is above this threshold will turn on the detection bit for that tone. Any signal below this threshold will turn off the detection bit for that tone. This location can be programmed using the following formula: $$\text{Threshold} = 10^{(\text{level})/20} \cdot 32767$$ This location must be programmed after Config.MODE is set to detect tone (02H). This is because the data pump will reset this location to its default when Config.MODE is set to tone detect mode. See the section on Tone Detectors for more information.

INTERFACE RAM DEFINITIONS (Continued)

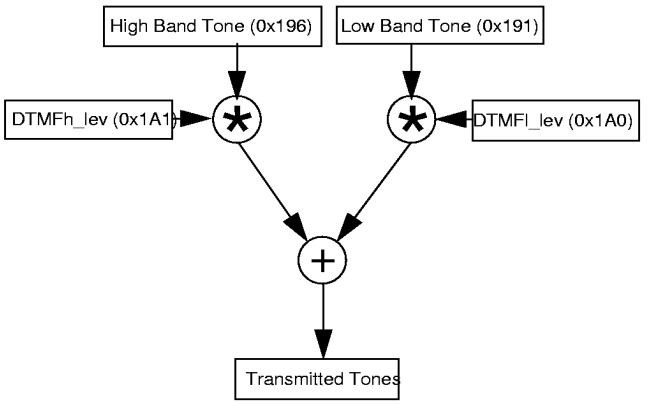
Table 15. Modem data pump Word Definitions

Register & Address (hex)		Default Value	Function and Explanation
DTDStatus	00	—	**Discrete Tone Detector Status**
			This location contains the status of the tone detectors when in tone detect mode (Config.MODE=002H). Bit 0 contains the status of detector 0, bit 1 the status of detector 1, and so on. This location is only valid when in tone detection mode. The response time of the tone detectors is dependent upon the frequency of the tone being detected and sampling rate of the data pump. When the host sets Config.MODE=0 (standby) or resets the data pump, the data pump writes its part number into this location.

OPERATING NOTES

TRANSMITTING TONES

The data pump has two tone generators, each with their own transmit level. The outputs are mixed together. The frequency of the tones are programmed by writing coefficients to locations ToneGenA and ToneGenB. The transmit levels are programmed by writing values to locations DTMF_lev and DTMFh_lev. If only one tone is to be transmitted, set the other tone generator's transmit level to 0 to disable it.



For example, to generate a 2100 Hz Answer Tone for 3.3 seconds at –10dBm:

1. Set location ToneGenA to 015FEH.
2. Set location DTMFl_lev to 0287H.
3. Set location DTMFh_lev to 0, disabling ToneGenB.
4. Set Config.MODE=1 (transmit tone).
5. Wait 3.3 seconds, then set Config.MODE=0 (standby).

TONE DETECTORS

There are 16 tone detectors in the data pump. They are programmed by setting up one word for each tone detectors. There is one global threshold setting for all 16 tone detectors. The address for the tone detectors are as follows:

- Tone Detector Coefficients—0145–0154H (Tone0–Tone15)
- Tone Detector Receive Levels—026H–035H (DTD0lev–DTD15lev)
- Tone Detector Threshold—03H
- Tone Detector Status—00H
- The tone coefficients are calculated as follows:

$$\mathrm{coeff}_{\mathrm{tone}} = \cos\left(\frac{2\pi \cdot \mathrm{f}_{\mathrm{tone}}}{9600}\right) \cdot 32767$$

TONE DETECTORS (Continued)

■ The default values on reset are:

Tone Detector	Frequency Detected (Hz)
0	697
1	770
2	852
3	941
4	1209
5	1336
6	1477
7	1633
8	1750
9	1800
10	1650
11	2225
12	2250
13	1300
14	2100
15	600

■ The threshold is calculated as follows:

$$\text{Threshold} = 10^{(\text{level})/20} \cdot 32767$$

where level is in dBm. The default value for the threshold is –24dBm. This value is set every time Config.MODE is set up to detect tones. If the user wishes a different value, it should be reloaded *after* Config.MODE is set to detect tones.

To use the tone detectors, perform the following steps:

1) Set up the tone detector coefficients (0145–0154H).

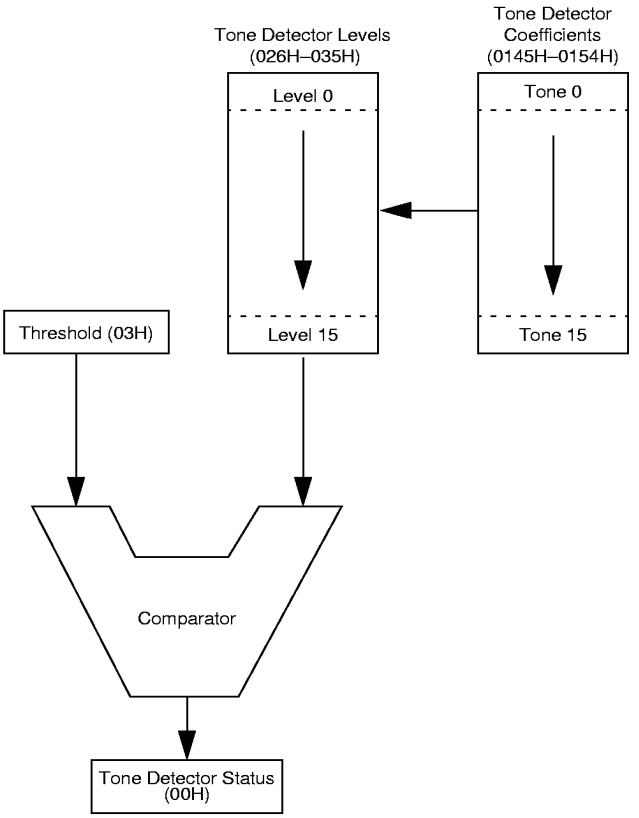
2) Set Config.MODE to tone detect mode (02H). Note that this is the same mode for using the Biquad tone detectors. This is because both the Biquad tone detectors and the tone detectors run at the same time. This allows the controller to look for individual answer tones as well as call progress tones.

3) Set up the tone detector threshold (03H)

4) Inspect the tone detector status (00H) for detected tones.

5) When the detection phase is complete, set Config.MODE to standby (00H).

The Detectors are set up as follows:



CALL PROGRESS MONITORING USING BIQUAD TONE DETECTORS

The data pump contains two biquad tone detectors that are capable of detecting energy in a frequency band. These detectors are useful for call progress monitoring where the exact frequency of the incoming signal is not known. Each biquad tone detector is composed of two cascaded, independently programmable biquad sections. The order of biquad coefficients in RAM is:

b2, b1, a3, a2, a1, B2, B1, A3, A2, A1

The addresses for the coefficients for the two filters start at 0155H (TONEA) and 015FH (TONEB). The sample rate is 9600 Hz.

The transfer equation for each half of the biquad tone detector is of the form:

$$H_n = \frac{2(a_1 + a_2Z^{-1} + a_3Z^{-2})}{(1 - 2b_1Z^{-1} - 2b_2Z^{-2})}$$

There are two threshold settings affecting both biquad tone detectors. The locations BiQuadOffThresh and BiQuadOnThresh define the on and off hysteresis points:

- BiQuadOffThresh–052H–Off point.
- BiQuadOnThresh–051H–On point.

Use the following formula to set the thresholds:

$$\text{Threshold} = 10^{(\text{level})/20} \cdot 32767$$

where level is in dBm. The default values are –35 dBm (BiQuadOnThresh) and –42dBm (BiQuadOffThresh).

The biquad tone detector status is contained in ToneStatus.TONEA and ToneStatus.TONEB. The response time of the biquad tone detectors depends on the coefficients and the input signal frequency.

The biquad tone detectors can be cascaded to form one tone detector with 4 biquad sections (an 8th order IIR filter) by setting ToneStatus.CASCADE. In this case ToneStatus.TONEA contains the status of the cascaded tone detector, and ToneStatus.SQRDIS controls whether the output of biquad tone detector B is squared before being input to biquad tone detector A.

The default settings for the biquad tone detector coefficients are shown in the tables below, where the first row is TONEA and the second row is TONEB. The data pump sets the biquad tone detector coefficients to their default settings upon any reset.

Biquad1 Coefficients (Hex)

Band (Hz)	b2	b1	a3	a2	a1
245–650	C63E	6FE1	F8EA	0000	0716
360–440	C7CD	7438	01AA	FEBC	01AA

Biquad2 Coefficients (Hex)

Band (Hz)	B2	B1	A3	A2	A1
245–650	C774	7601	0716	F5FB	0716
360–440	C148	7A66	FF5C	0000	00A4

To use the Biquad tone detectors to do Call Progress Monitoring, do the following:

1. Set the coefficients. Coefficients which are changed remain valid until the next reset.
2. Set Config.MODE=2 (detect tones). The biquad tone detectors and the discrete tone detectors operate simultaneously to allow the host to look for call progress tones and individual answer tones at the same time.
3. Set the BiquadOnThresh and BiquadOffThresh values.
4. If the two biquad tone detectors are to be cascaded, set ToneStatus.CASCADE=1. Then if desired, set ToneStatus.SQRDIS=1 to disable the squarer when the tone detectors are cascaded.
5. Inspect ToneStatus.TONEA and ToneStatus.TONEB for the detection status. If ToneStatus.CASCADE is set, only inspect ToneStatus.TONEA.
6. Time the on time and the off time of the tone(s). This gives you the cadence, which is used to identify the type of call progress tone detected. For example, 0.5 second on, 0.5 second off is usually a BUSY tone.
7. After call progress monitoring is complete, set Config.MODE=0 (standby).

DIALING

The data pump may be programmed to dial using either DTMF tones, or make/break pulses. By default, the data pump is Configured for tone (DTMF) dialing.

Tone Dialing

Tone dialing may be either continuous or timed. Continuous dialing generates the desired tone until the host specifically shuts it off. Timed dialing allows the host to specify the on/off timing of the digit dialed.

This example assumes the host controls the data pump's RTS through Reg4.RTSP. To perform tone dialing:

1. Set Reg4.RTSP=0, ToneStatus.TIMEDIAL=1 for timed dialing or=0 for continuous dialing. Then set Config.MODE=3 (dial). Then, if timed dialing is required, set the timer locations Seq1Count and Seq2Count.

2. Control the twist by setting locations DTMFh_lev and DTMFl_lev to specify the transmit levels of the high tone and the low tone respectively.

3. Set up the digit to be dialed in ToneStatus (01FCH) bits 0–3 according to the following table:

Digit	Value
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
*	10
#	11
A	12
B	13
C	14
D	15

4. For continuous operation, set Reg4.RTSP=1 to start transmitting the DTMF tone and=0 to stop.

5. For timed operation, set Reg4.RTSP=1 to dial the digit. The data pump sets Reg5.DPBUSY=1 while it dials the digit. Set Reg4.RTSP=0 after the digit has been dialed. The data pump sets Reg5.DPBUSY=0 when the dial sequence is completed.

6. To dial additional digits, repeat the procedure starting at step 3.

7. When dialing is complete, set Config.MODE=0 (standby).

Pulse Dialing

Pulse dialing is very similar to timed dialing, with the exception that the "tone" generated is a cadence of pulses output on the $\overline{OH}$ pin and mirrored in RAM location MStatus.OFFHOOK. To implement pulse dialing, follow the instructions for timed tone dialing, except:

1. Select pulse instead of tone dial mode by setting locationToneStatus.TONEDIAL=0.
   ToneStatus.TIMEDIAL has no effect. Pulse dialing is always timed.

2. After setting Config.MODE=3 (dial), set Seq1Count and Seq2Count and Seq3Count to the desired break and make times, and the pause after each digit is dialed. For North American applications requiring a 100 msec cadence, a 39%/61% make/break ratio, and a 0.75 second pause, set locations Seq1Count=024AH, Seq2Count=0176H, and Seq3Count=01C20H.

MANUAL HANDSHAKE PROCEDURES

The V.22bis data pump software allows the host to control every aspect of the handshake procedure. The host instructs the data pump which signal to send at which time. The data pump sets status bits when it receives signals from the remote modem.

The host begins a manual handshake by setting Config.MCUCTRL=1 to prevent the data pump from transmitting its own handshake signals.

The host monitors the receive signal status bits in location Trnctrl and transmits its own responding signals by setting Trnctrl.TXCTRL to the following values:

Trnctrl Value	Signal Transmitted
0	Silence
1	1200 bps Unscrambled Binary 1
2	S1
3	1200 bps Scrambled Binary 1
4	2400 bps Scrambled Binary 1
5	1200 bps data mode or FSK
6	2400 bps data mode
7	2225 Hz tone

In the following section certain acronyms shall be used to denote the various V.22bis handshake signals. These are:

Name	Meaning
USB1	Unscrambled Binary 1
SB1	Scrambled Binary 1
S1	S1 Signal

Originating modem

1. Take the telephone line off-hook and dial.
2. Program the discrete tone detectors and the biquad tone detectors for answer tones (2100 Hz) and call progress tones (200–600 Hz). Look for the answer tone and also call progress tones (such as busy tones, ring back and so on).
3. Upon receiving the 2100 Hz answer tone, set Config=4409H (V.22, V.22bis originate, manual handshake).
4. Wait for Trnctrl.USB1DET=1 (USB1 detected) continuously for 155 msec.
5. Wait for 456 msec.
6. Set Trnctrl.TXCTRL=2 (transmit S1) for 100 msec.
7. Set Trnctrl.TXCTRL=3 (transmit SB1) and inspect Trnctrl.S1DET and Trnctrl.SB1DET repeatedly for either a received S1 signal or SB1. If SB1 is received for 270 msec, proceed to step 11. If S1 is received, wait for the S1 to end. Then wait for an additional 450 msec.
8. Set Trnctrl.V22BIS=1 (force a 16 way receive decision). Wait for 150 msec.
9. Set Trnctrl.TXCTRL=4 (transmit SB1 at 2400 bps). Wait for 200 msec.
10. Set Trnctrl.TXCTRL=6 (2400 bps data mode). Data is now being transmitted and received at 2400 bps.
11. In step 7, if SB1 is detected instead of the S1 signal, wait for 765 msec, then set Trnctrl.TXCTRL=5 (1200 bps data mode). Data is now being transmitted and received at 1200 bps.

Answering Modem

1. Upon a ring signal or a command from the host, take the phone off-hook and transmit silence for 1.8 to 2.5 seconds.
2. If desired, use the tone generators to transmit a 2100 Hz tone for 2.6 to 4 seconds. This is the V.25 answer tone.
3. Set Config.MODE=0 (standby) and transmit silence for 75 msec.
4. Set Config=409H (answer mode, manual handshake).
5. Set Trnctrl.TXCTRL=1 (transmit USB1).
6. Inspect Trnctrl.S1DET and Trnctrl.SB1DET repeatedly for either a received S1 signal or SB1. If SB1 is received continuously for 270 msec, proceed to step 12. If an S1 signal is received (Trnctrl.S1DET=1) wait for the S1 to end.
7. Set Trnctrl.TXCTRL=2 (transmit S1) for 100 msec.
8. Set Trnctrl.TXCTRL=3 (transmit SB1) for 350 msec.
9. Set Trnctrl.V22BIS=1 (force 16 way receive decisions). Wait for 150 msec.
10. Set Trnctrl.TXCTRL=4 (transmit SB1 at 2400 bps). Wait for 200 msec.
11. Set Trnctrl.TXCTRL=6 (2400 bps data mode). Data is now being transmitted and received at 2400 bps.

MANUAL HANDSHAKE PROCEDURES (Continued)

12. If in step 6., SB1 is received instead of an S1 signal, set Trnctrl.TXCTRL=3 (transmit SB1) for 765 msec, then set Trnctrl.TXCTRL=5 (1200 bps data mode). Data is now being transmitted and received at 1200 bps.

MAKING A V.22BIS CONNECTION

In the following example, all timing is performed by the host.

Originating Modem

1. Take the telephone line off-hook and dial.
2. Program the discrete tone detectors and the biquad tone detectors for answer tones (2100 Hz) and call progress tones (200–600 Hz). Look for the answer tone and call progress tones (busy tones, ring back, etc.)
3. Upon receiving the 2100 Hz answer tone, set Config=4008 (V.22bis originate). After setting Config, the host should be prepared to receive data from the remote modem. The data pump holds the received data to marks (i.e., receives nothing) until the modem is able to receive data from the remote modem.
4. When the data pump establishes a V.22bis connection and is ready to transmit data to the remote modem, it sets Reg5.CDET=1. Data may now be transmitted or received between the modems.

Answering Modem

1. Upon a ring signal or command from the terminal, take the phone off-hook and transmit silence for 1.8–2.5 seconds.
2. If desired, use the tone generators to transmit a 2100 Hz tone for 2.6–4 seconds. This is the V.25 answer tone.
3. Set Config.MODE=0 (standby) and transmit silence for 75 msec.
4. Set Config=8 (V.22bis answer). After setting Config, the host should be prepared to receive data from the remote modem. The data pump holds the received data to marks (i.e., receives nothing) until the modem is able to receive data from the remote modem.
5. When the data pump establishes a V.22bis connection and is ready to transmit data to the remote modem, it sets Reg5.CDET=1. Data may now be transmitted or received between the modems.

Important notes

a. The data pump sets Reg5.CDET=0 during carrier dropouts, retrains, and when the remote modem hangs up the telephone line. Depending on the data mode, the host may use Reg5.CDET, Reg5.RTRND, Dpctrl.EQE, EQMlev and EQMMaxThresh to determine when the remote modem has initiated a retrain, or has hung up the telephone line.

b. During 2400 bps V.22bis data mode, the host may use Dpctrl.EQE and EQMMaxThresh or EQMlev to determine when the initiate a retrain (see (MStatus.RETRAIN) to improve the quality of the connection.

USING HDLC

The data pump includes HDLC firmware operating in all data modes. The HDLC firmware performs all the necessary operations to frame host-supplied data into HDLC format, including automatic opening and closing flag generation, zero insertion and deletion, flag and abort detection, and CRC checksum computation and checking.

HDLC Operation

During HDLC operation the data pump frames host-supplied asynchronous data into a synchronous data stream in the transmitter, and extracts the same asynchronous data from the received synchronous data stream in the receiver. The inclusion of 16-bit cyclic redundancy check (CRC) information in the frames allows the receiving host to check whether the data has been correctly received.

HDLC data is sent in frames. A frame consists of a number of bytes, each composed of 8 data bits. A frame contains an opening flag, frame data bytes, two CRC checksum bytes and a closing flag, in this order. Opening flags and closing flags indicate the start and end of a frame, respectively.

A flag, byte value 07E, is one of two HDLC control symbols. The other is an abort, which is any sequence of consecutive binary 1s more than six bits long. If the frames do not use the bandwidth of the data mode (for example, when there is no host data to transmit), the modem fills the remaining bandwidth by sending flags between frames.

Frame data bytes for transmission are supplied by the host to the data pump's DATAP register. These bytes are modified by the data pump to ensure that no more than five consecutive binary 1 bits are sent. To do this, the transmitting modem inserts a single 0 bit after every five consecutive binary 1 bits in the host supplied data. This zero insertion process allows the receiving modem's data pump to distinguish between frame data, flags and aborts. The receiving modem's data pump uses a zero deletion process to remove each inserted 0 bit before returning the data to the receiving modem's host.

When a frame is to be closed, the frame's two CRC checksum bytes are sent immediately following the frame data. The CRC checksum is computed without the inserted zeroes. The frame's closing flag is transmitted following the CRC. This flag may also serve as the opening flag of the next frame, saving bandwidth.

Enabling HDLC Operation

The data pump's HDLC firmware is disabled upon power-up and any reset, and can be enabled only in parallel mode (Reg4.TPDM=1). To enable HDLC, set Bufctrl.HDLC to 1, and bits 8..15 of Bufctrl to 0 prior to beginning data mode operation. The host should also read register DATAP just before starting data mode to clear DATAP.

These examples demonstrate the use of the data pump in parallel mode to transmit and receive HDLC data frames. The examples assume that the data pump has just been put in data mode, and HDLC operation is enabled. The data to be sent or received is the sequence of N bytes {Byte1..ByteN}, where Byte1 is sent (or received) first.

Transmitting

1. When Reg5.TXI=1, write Byte1 to DATAP. Repeat this step for each byte to be transmitted. If Reg4.TXIE=1, the data pump generates an interrupt when it is ready to transmit the next byte, i.e. when it sets Reg5.TXI=1.

2. When the last byte, ByteN, has been sent, wait for the data pump to set Reg7.TEND=1. This indicates the data pump has closed the current frame. The data pump now computes and transmits the CRC checksum and closing flag for the frame. The data pump does not set Reg7.TEND=1 until at least 8 bit times after it has set Reg4.TXI=1 indicating the data pump is ready to transmit another data byte. To transmit another frame, repeat steps 1–2.

3. When the data pump begins sending the frame's closing flag, it sets Reg7.TEND=0. Transmission of the frame is complete 8 bit times after the data pump sets Reg7.TEND=0.

Receiving

1. Prepare to receive a new frame.

2. When Reg5.RXI=1 the data pump has received a byte. First read register Reg7, then DATAP. Register Reg7 is read first because the data pump may change it any time after DATAP is read. If Reg4.RXIE=1, the data pump generates an interrupt when it sets Reg5.RXI=1.

3. Act on the value of Reg7 read in step 2 as follows: If RXERROR=0 and EOF=0 the DATAP value read in step 2 is an HDLC frame byte. Repeat step 2 to receive all remaining frame bytes. If RXERROR=0 and EOF=1 an HDLC frame with a correct checksum has been received. If bytes Byte1..ByteN+3 have been read, with ByteN+3 being the DATAP value just read, then the two previous bytes, ByteN+1 and ByteN+2, are the frame checksum bytes, and the remaining bytes, Byte1..ByteN, are the frame data bytes. Continue from step 1 to receive the next frame. If RXERROR=1 discard any received frame bytes and continue from step 1 to receive the next frame. If DATAP was 0FF, an HDLC abort sequence was received. If DATAP was 07EH, an HDLC frame with an incorrect checksum was received.

GETTING THE DATA PUMP FIRMWARE VERSION NUMBER AND PART NUMBER

The data pump code version can be obtained any time RAM location Config.MODE is set to 0. The data pump will write the part number to data pump RAM location 0 and the code version number to the DATAP register. To obtain the version and part number from the data pump, the following steps must be performed:

1. Set Config.MODE to 0 (standby), then read location Config to give the data pump enough time to begin standby operation.
2. Read the DATAP register. This will return the code release version number (an 8 bit value, e.g., 030H indicates version 30).
3. Read RAM location 0. This will return the part number (e.g., 02201H for a Z02201 part).

SLEEP MODE

The data pump incorporates a low power sleep mode. In this mode the data pump clock is shut down, effectively stopping the part. To enter sleep mode, the controller can set Config to mode 7. To exit sleep mode, the controller can either reset the data pump (asserting the RESET signal) or write any value to the DATAP register. The host should then wait until the RESET (output) bit indicates that the DSP is fully reset, before accessing the data pump registers.

TYPICAL PERFORMANCE DATA

The Bit Error Rate (BER) and Block Error Rate (BLER) curves in Figure 10 and 11 represent typical V.22 and V.22bis performance over a variety of signal to noise conditions (SNR). Note that modems will usually exhibit lower bit error rates receiving in the low band as opposed to the high band. One analog link was made, after which the Adaptive Equalizer (AEQ) was frozen. The noise level was then increased without making new links. These tests were conducted using a Consultronics TCS500 Telephone Line Simulator and a Hewlett Packard 4951B protocol analyzer/BERT tester, under the following conditions:

Line Simulation	Flat
Transmit Level	–10 dBm
Receive Level	–16.0 dBm
Data Transmitted	511 pseudorandom pattern
Number of Bits Sent	1,000,000
Number of Blocks Sent	1,000
Bits per Block	1,000
AEQ	Frozen after link establishment
Noise Calibration	C-message

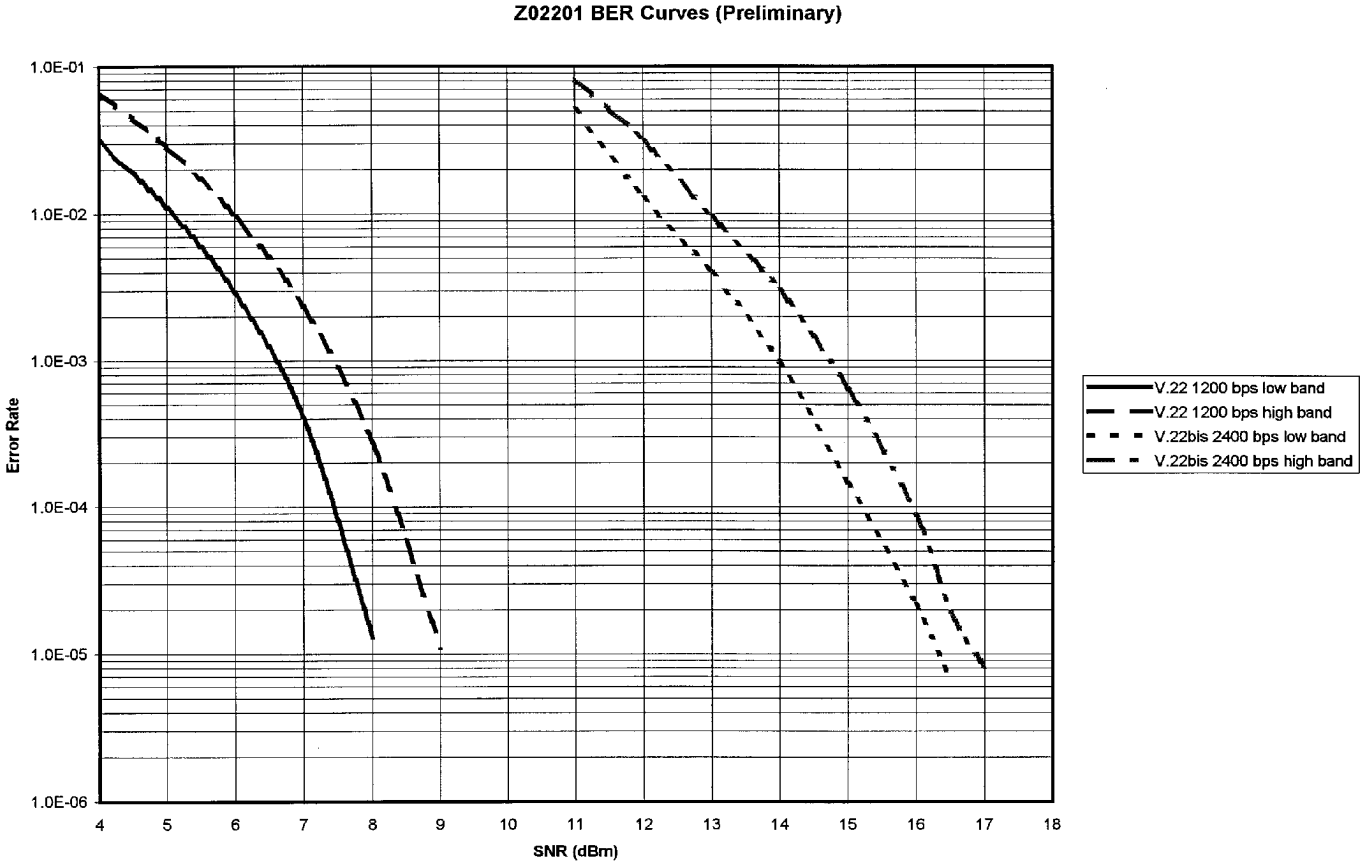


Figure 9. Typical Performance Data

TYPICAL PERFORMANCE DATA (Continued)

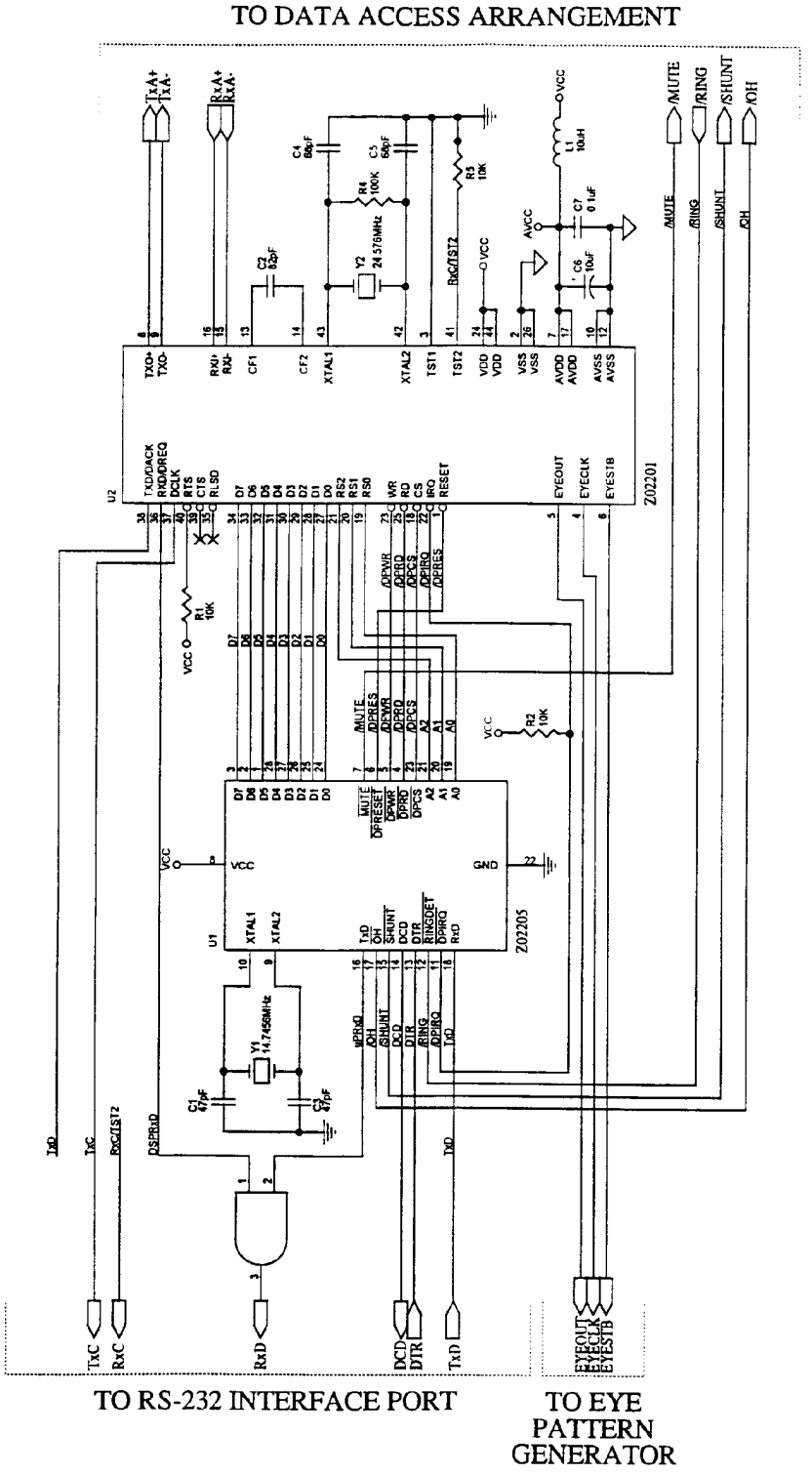


Figure 10. Typical Modem Using Z02201

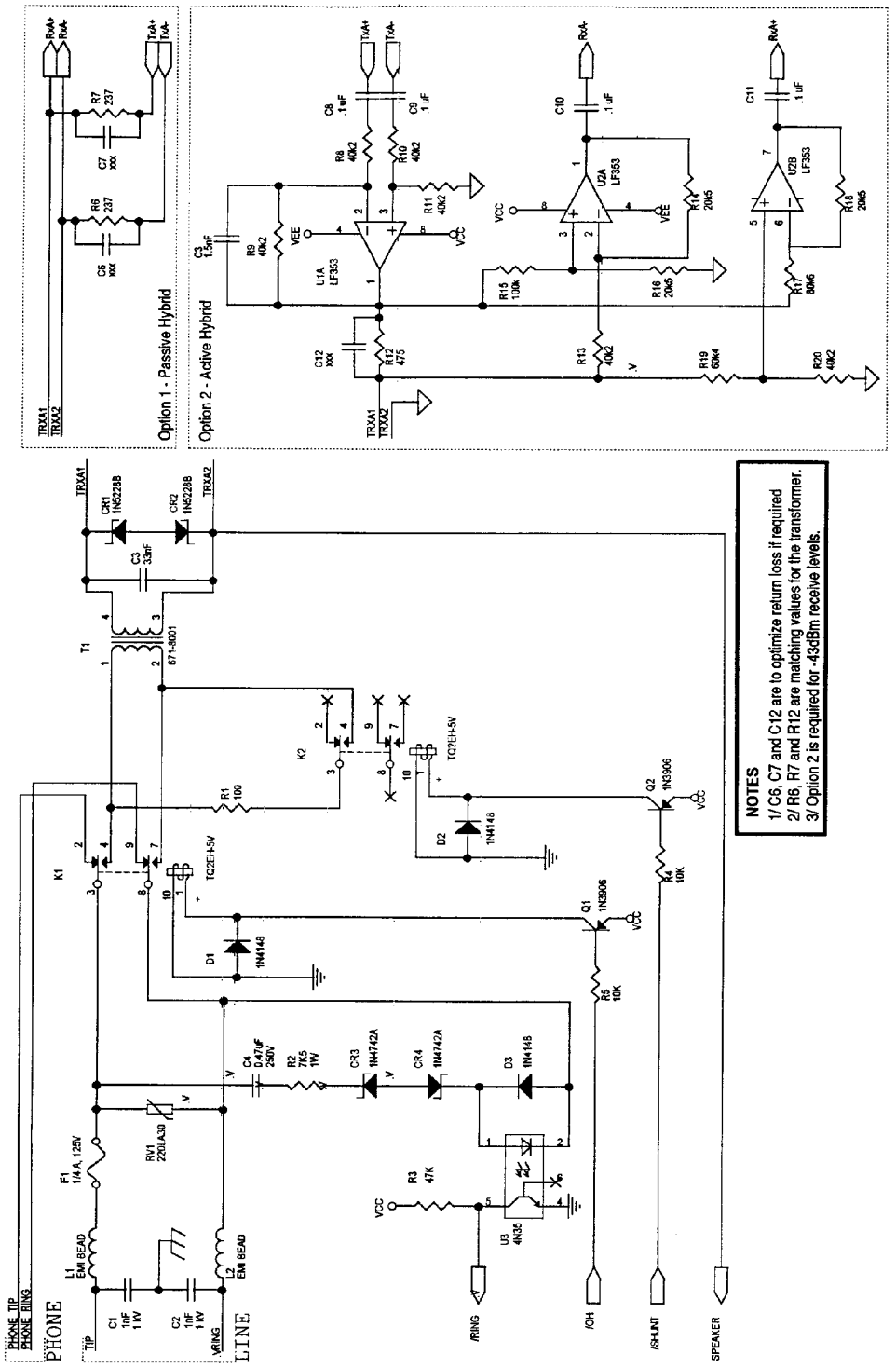


Figure 11. Example DAA (North America)

Figure 11 shows an example DAA configuration for North America. Isolation transformer T1 couples the primary (line) and secondary (modem) sides, while providing high voltage isolation. This "wet" transformer (allowing DC current) simplifies the circuit and reduces the cost of the DAA.

TYPICAL PERFORMANCE DATA (Continued)

On the Secondary side, the transmit (TxA+ and TxA–) and receive (RxA+ and RxA–) are combined in the 4-wire to 2-wire hybrid circuit. This hybrid can be either passive or active. The more complex active hybrid allows operation to lower signal levels, since it cancels out most of the transmit signal from the receive signal.

On the Primary side, the off-hook relay switches the phone line between a local handset (PHONE) or the modem. The ring detect circuit consists of DC blocking capacitor C4, current limiting resistor R2, zener diodes CR3 and CR4, optocoupler U3 and its reverse protection diode D3. Protection elements RV1, F1, C1, and C2 (and transformer T1's isolation) will provide higher voltage capability for approval in some foreign markets. C1 and C2, for example, may need to be replaced by Metal Oxide Varistors (MOVs) or Gas Discharge Tubes (GDTs). The shunt relay reduces the DAA impedance during pulse dialing. This is required for certain country approvals.

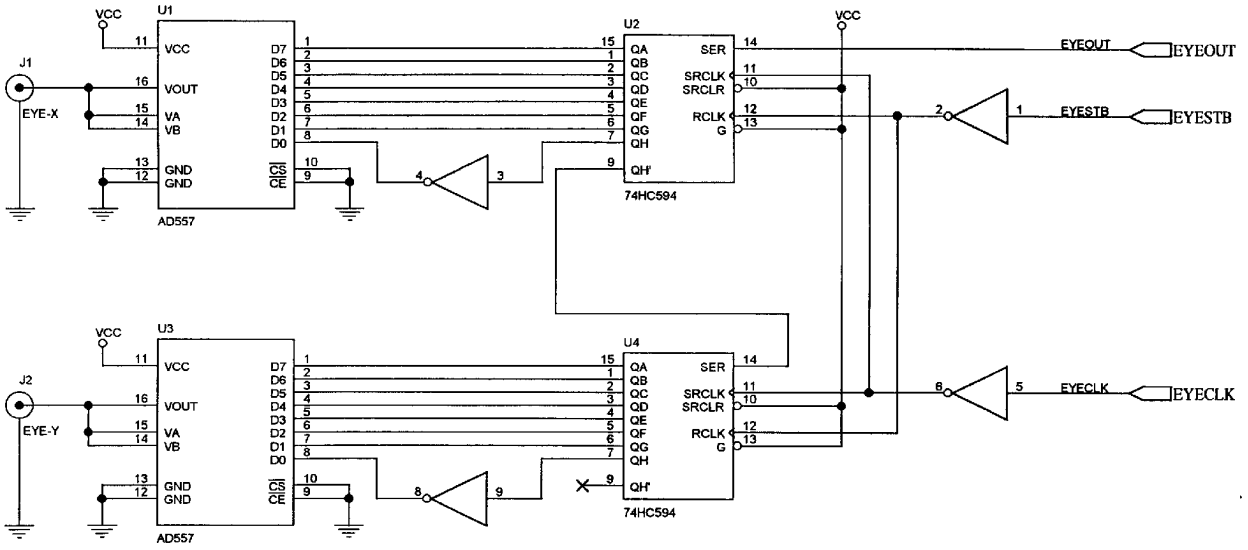


Figure 12. Eye Pattern Circuit

Figure 12 is the eye pattern circuitry used on the Z0220100ZCO modem evaluation board, and can be used with modem components such as the Zilog Z02201 and Z02922 that have an eye pattern interface. The Z02201 Eye Pattern port consists of 3 signals:

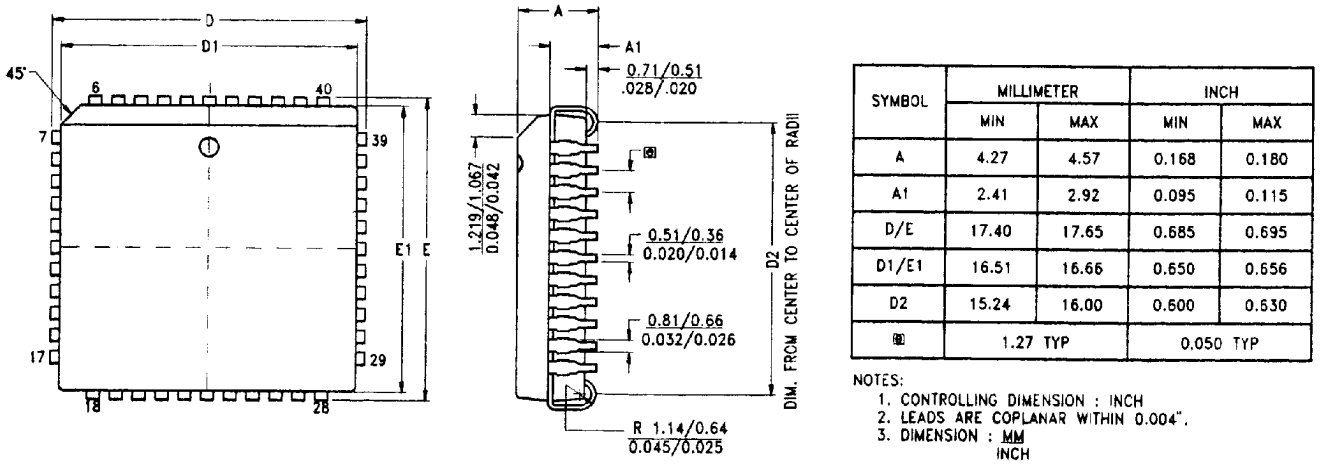
Data (EYEOUT): The most significant and least significant bytes of this 16 bit word are the X and Y coordinates respectively for the eye pattern display. Each byte is most significant bit first.

Clock (EYECLK): Data is set on the rising edge of the EYECLK, and should be read on the falling edge.

Strobe ($\overline{\text{EYESTB}}$): This signal is active low when the data is valid.

Data is shifted through a pair of 8 bit serial-in parallel-out shift registers (74HC594) in response to the falling edge of EYECLK, then latched into a pair of 8 bit DACs on the rising edge of EYESTB. The output of these DACs can be viewed on an oscilloscope in X–Y mode to see the received signal quality.

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 TYP		0.050 TYP	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM / INCH

Figure 13. 44-Lead PLCC Package Diagram

ORDERING INFORMATION

Z02201
12 MHz
44-Pin PLCC
Z0220112VSC
Z0220112VEC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Speed

12=12 MHz

Package

V=Plastic Leaded Chip Carrier

Temperature

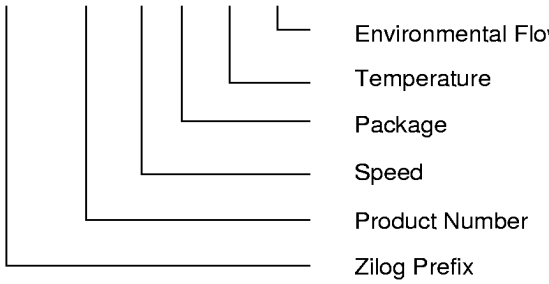
S=0°C to +70°C
E=–40°C to +85°C

Environmental

C=Plastic Standard

Example

Z 02201 12 V S C is a Z02201, 12 MHz, PLCC, 0°C to +70°C, Plastic Standard Flow



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