SED1180F/SED1181F

CMOS DOT MATRIX HIGH DUTY LCD DRIVER

■DESCRIPTION

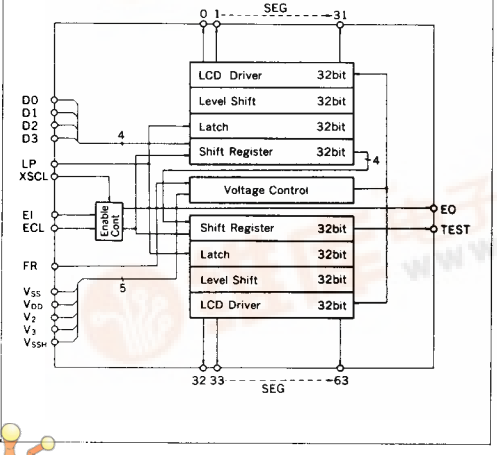
The SED1180F and SED1181F are LCD Segment drivers which are used in conjunction with the SED1190F and SED1191F (LCD common drivers).
They can drive a large dot-matrix LCD display with a duty ratio of 1/64 or higher.

■FEATURES

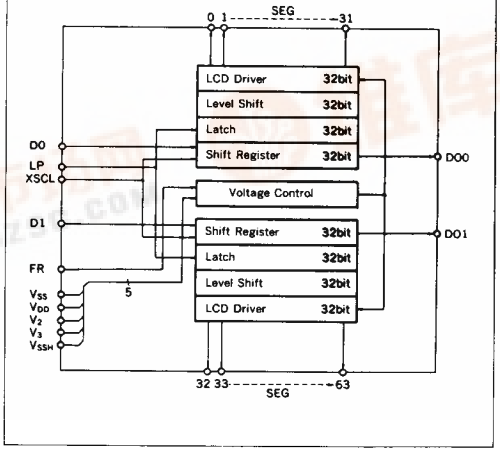
- ●Display duty ·····1/64 to 1/128
- ●64-bit high voltage resistant output, LCD driver (Segment driver)
- ●Rightward shift suitable for a 1/64-duty panel
- ●Allows cascade-connection. Dasy-chain connection of enable pins can be used to minimize power consumption. (SED1180F only)
- ●Power supply for the logic·····−5V±10%
- ●CMOS high-voltage-resistant process·····25V (Max)
- ●SED1180F ·····4-bit bus data transfer
- ●SED1181F ·····Independent serial data input for each 32 segment
- ●Package·····80-pin QFP (plastic)

■BLOCK DIAGRAM

SED1180F



SED1181F



■PIN DESCRIPTION

SED1180F

Pin Name	Functions
SEG0 to 63	Outputs to Segment pins of LCD Output level changes at each latch pulse LP falling-edge.
XSCL	Shift clock for displayed data Falling-edge trigger
LP	Latch pulse for displayed data Falling-edge trigger
FR	LCD display frame signal
EI	Enable input ; enabled on "H", disabled on "L"
ECL	A clock pulse for propagation of enable signals Falling-edge trigger
EO	Enable output In cascade connection, EO of nth driver is connected to EI of (n+1)-th driver.
D0 to D3	4-bit display data input
TEST	Outputs shifted data input from D3
V_{DD}, V_{SS}	Power supply for the logic, V_{DD} : 0V (GND), V_{SS} : −5.0V
V_2, V_3, V_{SSH}	Power supply for driving LCD, $V_{DD} > V_2 > V_3 > V_{SSH}$

SED1181F

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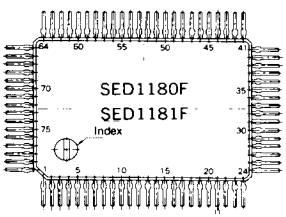
SEG0 to 63	Outputs to Segment pins of LCD Output level changes at each latch pulse LP falling-edge
XSCL	Shift clock for displayed data Falling-edge trigger
LP	Latch pulse for displayed data Falling-edge trigger
FR	LCD display frame signal
DO0	Outputs serial display data input from D0.
DO1	Outputs serial display data input from D1.
D0, D1	Input 2-bit serial display data (Data read at a XSCL falling-edge)
V_{DD}, V_{SS}	Power supply for the logic, V_{DD} : 0V (GND), V_{SS} : −5.0V
V_2, V_3, V_{SSH}	Power supply for driving LCD, $V_{DD} > V_2 > V_3 > V_{SSH}$

Note :
D0 : serial display data corresponds to SEG0 to SEG31.
D1 : serial display data corresponds to SEG32 to SEG63.

■PIN CONFIGURATION



SED1180F

No.	NAME	No.	NAME	No.	NAME	No.	NAME
1	SEG27	21	SEG 7	41	SEG36	61	SEG56
2	SEG26	22	SEG 6	42	SEG37	62	SEG57
3	SEG25	23	SEG 5	43	SEG38	63	SEG58
4	SEG24	24	SEG 4	44	SEG39	64	SEG59
5	SEG23	25	SEG 3	45	SEG40	65	SEG60
6	SEG22	26	SEG 2	46	SEG41	66	SEG61
7	SEG21	27	SEG 1	47	SEG42	67	SEG62
8	SEG20	28	SEG 0	48	SEG43	68	SEG63
9	SEG19	29	EO	49	SEG44	69	V_{SSH}
10	SEG18	30	D3	50	SEG45	70	V_2
11	SEG17	31	D2	51	SEG46	71	V_3
12	SEG16	32	D1	52	SEG47	72	V_{SS}
13	SEG15	33	D0	53	SEG48	73	V_{DD}
14	SEG14	34	XSCL	54	SEG49	74	TEST
15	SEG13	35	LP	55	SEG50	75	EI
16	SEG12	36	FR	56	SEG51	76	ECL
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG 9	39	SEG34	59	SEG54	79	SEG29
20	SEG 8	40	SEG35	60	SEG55	80	SEG28

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1	SEG27	21	SEG 7	41	SEG36	61	SEG56
2	SEG26	22	SEG 6	42	SEG37	62	SEG57
3	SEG25	23	SEG 5	43	SEG38	63	SEG58
4	SEG24	24	SEG 4	44	SEG39	64	SEG59
5	SEG23	25	SEG 3	45	SEG40	65	SEG60
6	SEG22	26	SEG 2	46	SEG41	66	SEG61
7	SEG21	27	SEG 1	47	SEG42	67	SEG62
8	SEG20	28	SEG 0	48	SEG43	68	SEG63
9	SEG19	29	DO0	49	SEG44	69	V_{SSH}
10	SEG18	30	NC	50	SEG45	70	V_2
11	SEG17	31	NC	51	SEG46	71	V_3
12	SEG16	32	D1	52	SEG47	72	V_{SS}
13	SEG15	33	D0	53	SEG48	73	V_{DD}
14	SEG14	34	XSCL	54	SEG49	74	DO1
15	SEG13	35	LP	55	SEG50	75	NC
16	SEG12	36	FR	56	SEG51	76	NC
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG 9	39	SEG34	59	SEG54	79	SEG29
20	SEG 8	40	SEG35	60	SEG55	80	SEG28

■ABSOLUTE MAXIMUM RATINGS

(V_{DD} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	−7.0 to 0.3	V
Supply voltage (2)	V_{SSH}	−28.0 to 0.3	V
	V_2, V_3		
Input voltage	V_I	V_{SS} − 0.3 to 0.3	V
Operating temperature	T_{opr}	−20 to 75	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C · 10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD} = 0V, V_{SS} = −5V ± 10%, Ta = −20 to 75°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Supply voltage (1)	V_{SS}			−5.5	−5.0	−4.5	V
Supply voltage (2)	V_2			V_{SSH}		V_{DD}	V
	V_3			V_{SSH}		V_{DD}	V
	V_{SSH}	Recommended V_{SSH}		−25.0		−14.0	V
		Operable V_{SSH}*		−25.0		−5.0	V
High level input voltage	V_{IH}			0.2V_{SS}		V_{DD} + 0.3	V
Low level input voltage	V_{IL}			V_{SS} − 0.3		0.8V_{SS}	V
High level output voltage	V_{OH}	I_{OH} = −0.6mA		−0.4			V
Low level output voltage	V_{OL}	I_{OL} = 0.6mA		—		V_{SS} + 0.4	V
Input leak current	I_{LI}	$0V \leqq V_I \leqq V_{SS}$		—	0.05	2.0	μA
Output leak current	I_{LO}	$0V \leqq V_O \leqq V_{SS}$		—	0.05	5.0	μA
Shift clock	XSCL			—		6.0	MHz
Frame signal	FR			—	1/60	—	s
Input capacitance	C_I	Ta = 25°C		—	5.0	8.0	pF
Segment output on resistance	R_{SEG}	$V_{OH} = V_{DD} - 0.5V$, $V_{OL} = V_{SSH} + 0.5V$, SEG /bit	V_{SSH} = −20.0V	—	1.9	2.9	kΩ
			V_{SSH} = −14.0V	—	2.4	3.9	
			V_{SSH} = − 9.0V	—	3.6	7.0	
			V_{SSH} = − 5.0V	—	11.5	500.0	
Quiescent current	I_Q	V_{SSH} = −25V, V_{SS} = −5.5V, $V_I = V_{DD}$		—	0.05	30	μA
Operating current for the logic	I_{SSO}	SED1180: FR cycle = 16.7ms, ECL cycle = 13μs	V_{SS} = −5.0V, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, LP cycle = 130μs, XSCL = 1.5MHz (duty50%), All data input reversed bit by bit. All output pins are opened.	—	90	200	μA
		SED1181: FR cycle = 130μs (duty50%)		—	850	1200	
Operating current for LCD	I_{SSHO}	SED1180: FR cycle = 16.7ms, ECL cycle = 13μs	V_{SS} = −4.5V, V_2 = −4.0V, V_3 = −16.0V, V_{SSH} = −20.0V, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, LP cycle = 130μs, XSCL = 1.5MHz (duty50%), All data input reversed bit by bit. All output pins are opened.	—	40	80	μA
		SED1181: FR cycle = 130μs (duty50%)		—	70	100	

*Operable V_{SSH} indicates its functionally operable range although the driver output ON resistance becomes higher than with recommended V_{SSH}.
To determine the voltage, we recommend to test the driver with a liquid crystal panel.

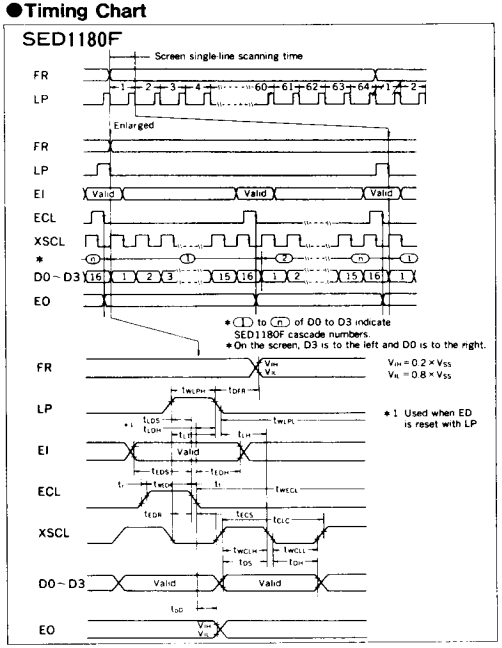
●AC Electrical Characteristics

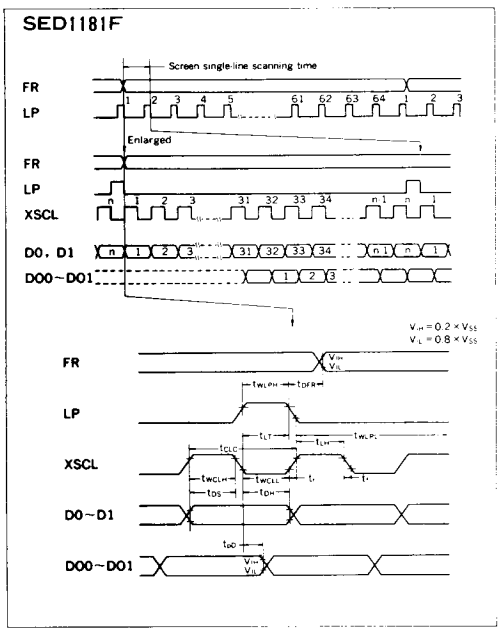
(V_{DD} = 0V, V_{SS} = −5.0V ± 10%, Ta = −20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Shift clock cycle	t_{CLC}		166	—	—	ns
Shift clock "H" width	t_{WCLH}		63	—	—	ns
Shift clock "L" width	t_{WCLL}		63	—	—	ns
Data setup time	t_{DS}		50	—	—	ns
Data hold time	t_{DH}		30	—	—	ns
Enable clock "H" width	t_{WECH}	*3	100	—	—	ns
Enable clock "L" width	t_{WECL}	*3	100	—	—	ns
Enable data setup time	t_{EDS}	*3	50	—	—	ns
Enable data hold time	t_{EDH}	*3	20	—	—	ns
Enable clock delay time	t_{EDR}	*3	−10	—	—	ns
Enable clock setup time	t_{ECS}	*3	70	—	—	ns
Latch pulse "H" width	t_{WLPH}	*1	110	—	—	ns
Latch pulse "L" width	t_{WLPL}		220	—	—	ns
Latch timing	t_{LT}		100	—	—	ns
Latch hold time	t_{LH}		0	—	—	ns
Latch pulse data setup time	t_{LDS}	*2, *3	140	—	—	ns
Latch pulse data hold time	t_{LDH}	*2, *3	50	—	—	ns
Permissible frame signal delay	t_{DFR}		−500	—	500	ns
Input signal rise time	t_r		—	—	*4	
Input signal fall time	t_f		—	—	*4	
Enable output delay	t_{PD}	*3	20	—	150	ns
Serial data output delay	t_{PO}		20	—	150	ns

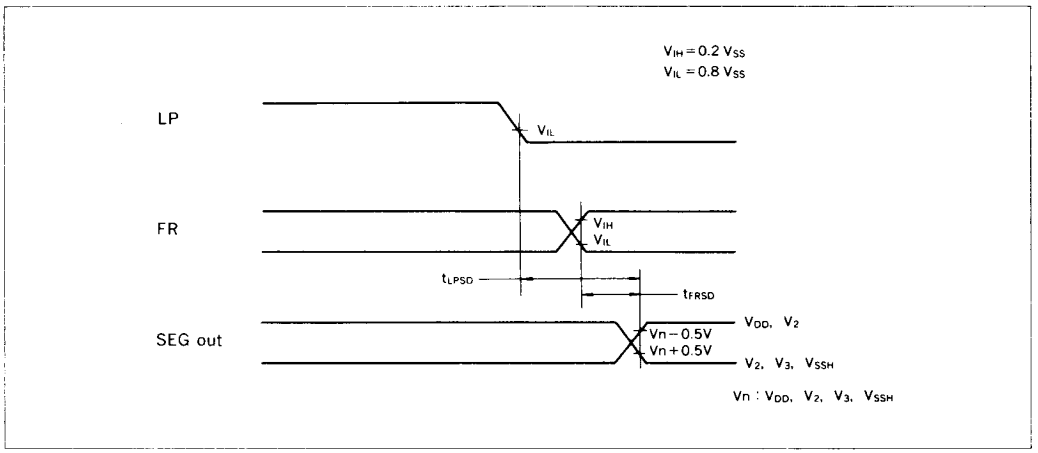
*1 t_{WLPH} = 160ns (Min) when LP is used as EI data.
*2 t_{WLPH} = 250ns (Min) when EO output is reset with LP. (tr = tf = 25ns)
*3 Applicable to SED1180F only.
*4 tr, tf < ($t_{CLC} - t_{WCLH} - t_{WCLL}$)/2, where tr, tf ≤ 50ns.

●Timing Chart





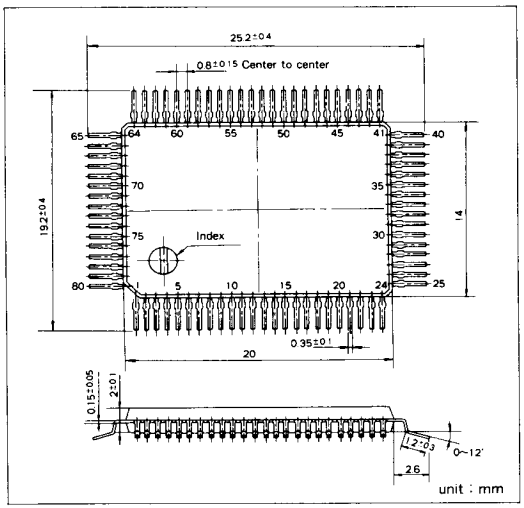
●SEG Output Signal Timing Characteristics



(VDD = 0V, VSS = −5V ± 10%, Ta = −20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LP-SEG output delay time	t_{LPSD}	V_{SSH} = −14.0 to −25.0V	—	—	4.5	μs
FR-SEG output delay time	t_{FRSD}	C_L = 100pF	—	—	4.5	μs

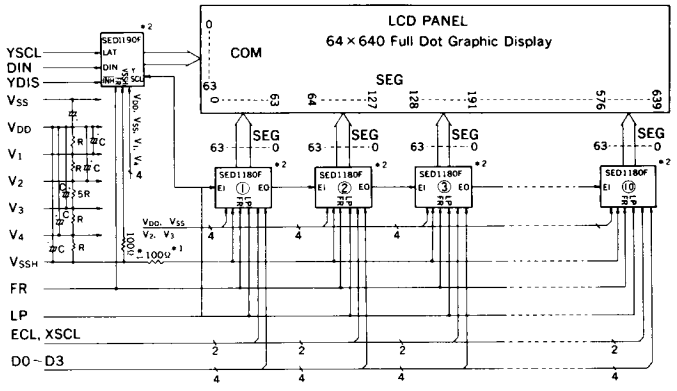
■PACKAGE DIMENSIONS



*Drawing is applicable to SED1180F0A/SED1181F0B.
*SED1180F5A/SED1181F5A are 2.7mm thick.

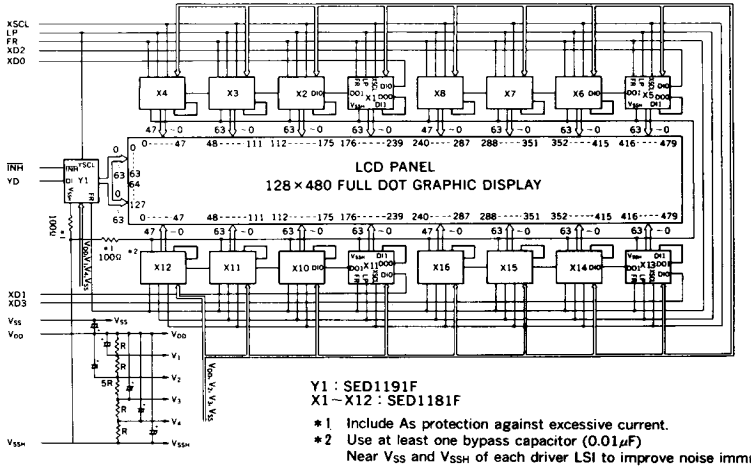
■EXAMPLE OF APPLICATION

SED1180F (64×640 dot, 1/64 duty, 1/9 bias)



*1 Use to protect against excessive current.
*2 Use at least one bypass capacitor (0.01μF)
Near V_{SS} and V_{SSH} of each driver LSI to improve noise immunity.

SED1181F (128×480 dot, 1/64 duty, 1/9 bias)



Y1 : SED1191F
X1~X12 : SED1181F

*1 Include As protection against excessive current.
*2 Use at least one bypass capacitor (0.01μF)
Near V_{SS} and V_{SSH} of each driver LSI to improve noise immunity.