XC2C512 CoolRunner-II CPLD

DS096 (v1.0) July 19, 2002

Advance Product Specification

Features

- Optimized for 1.8V systems
  - As fast as 6.0 ns pin-to-pin delays
  - As low as 30 µA quiescent current
- Industry's best 0.18 micron CMOS CPLD
  - Optimized architecture for effective logic synthesis
  - Multi-voltage I/O operation — 1.5V to 3.3V
- Available in multiple package options
  - 208-pin PQFP with 173 user I/O
  - 256-ball FT (1.0mm) BGA with 212 user I/O
  - 324-ball FG (1.2mm) BGA with 270 user I/O
- Advanced system features
  - Fastest in system programming
    - 1.8V ISP using IEEE 1532 (JTAG) interface
  - IEEE1149.1 JTAG Boundary Scan Test
  - Optional Schmitt-trigger input (per pin)
  - Unsurpassed low power management
  - Four seperate output banks
  - Fast Zero Power™ (FZP) 100% CMOS product term generation
  - DataGATE enable (DGE) signal control
  - Flexible clocking modes
    - Optional DualEDGE triggered registers
    - Clock divider (divide by 2,4,6,8,10,12,14,16)
    - CoolCLOCK
  - Global signal options with macrocell control
    - Multiple global clocks with phase selection per macrocell
    - Multiple global output enables
    - Global set/reset
  - Advanced design security
  - Open-drain output option for Wired-OR and LED drive
  - Optional bus-hold, 3-state or weak pullup on selected I/O pins
  - Optional configurable grounds on unused I/Os
  - Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels
    - SSTL2-1, SSTL3-1, and HSTL-1 I/O compatibility
  - Hot pluggable

Refer to the CoolRunner™-II family data sheet for architecture description.

Description

The CoolRunner-II 512-macrocell device is designed for both high performance and low power applications. This lends power savings to high-end communication equipment and high speed to battery operated devices. Due to the low power stand-by and dynamic operation, overall system reliability is improved

This device consists of thirty two Function Blocks inter-connected by a low power Advanced Interconnect Matrix (AIM). The AIM feeds 40 true and complement inputs to each Function Block. The Function Blocks consist of a 40 by 56 P-term PLA and 16 macrocells which contain numerous configuration bits that allow for combinational or registered modes of operation.

Additionally, these registers can be globally reset or preset and configured as a D or T flip-flop or as a D latch. There are also multiple clock signals, both global and local product term types, configured on a per macrocell basis. Output pin configurations include slew rate limit, bus hold, pull-up, open drain and programmable grounds. A Schmitt-trigger input is available on a per input pin basis. In addition to storing macrocell output states, the macrocell registers may be configured as "fast input" registers to store signals directly from input pins.

Clocking is available on a global or Function Block basis. Three global clocks are available for all Function Blocks as a synchronous clock source. Macrocell registers can be individually configured to power up to the zero or one state. A global set/reset control line is also available to asynchronously set or reset selected registers during operation. Additional local clock, synchronous clock-enable, asynchonous set/reset and output enable signals can be formed using product terms on a per-macrocell or per-Function Block basis.

A DualEDGE flip-flop feature is also available on a per macrocell basis. This feature allows high performance synchronous operation based on lower frequency clocking to help reduce the total power consumption of the device.

Circuitry has also been included to divide one externally supplied global clock (GCK2) by eight different selections. This yields divide by even and odd clock frequencies.

The use of the clock divide (division by 2) and DualEDGE flip-flop gives the resultant CoolCLOCK feature.

DataGATE is a method to selectively disable inputs of the CPLD that are not of interest during certain points in time.

By mapping a signal to the DataGATE function, lower power can be achieved due to reduction in signal switching.

Another feature that eases voltage translation is output banking. Four output banks are available on the CoolRunner-II 512 macrocell device that permits easy interfacing to 3.3V, 2.5V, 1.8V, and 1.5V devices.

The CoolRunner-II 512 macrocell CPLD is I/O compatible with various JEDEC I/O standards (see Table 1). This device is also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

Fast Zero Power Design Technology

Xilinx CoolRunner-II CPLDs are fabricated on a 0.18 micron process technology which is derived from leading edge FPGA product development. CoolRunner-II CPLDs employ Fast Zero Power™ (FZP), a design technique that makes use of CMOS technology in both the fabrication and design methodology. FZP design technology employs a cascade of CMOS gates to implement sum of products instead of traditional sense amplifier methodology. Due to this technology, Xilinx CoolRunner-II CPLDs achieve both high-performance and low power operation.

Supported I/O Standards

The CoolRunner-II 512 macrocell features LVCMOS, LVTTL, SSTL, and HSTL I/O implementations. See Table 1 for I/O standard voltages. The LVTTL I/O standard is a general purpose EIA/JEDEC standard for 3.3V applications that use an LVTTL input buffer and Push-Pull output buffer. The LVCMOS standard is used in 3.3V, 2.5V, 1.8V applications. Both HSTL and SSTL I/O standards make use of a V_{REF} pin for JEDEC compliance. CoolRunner-II CPLDs are also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

Table 1: **I/O Standards for XC2C512**

I/O Types	Output V_{CCIO}	Input V_{CCIO}	Input V_{REF}	Board Termination Voltage V_{TT}
LVTTL	3.3	3.3	N/A	N/A
LVCMOS33	3.3	3.3	N/A	N/A
LVCMOS25	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
1.5V I/O	1.5	1.5	N/A	N/A
HSTL-1	1.5	1.5	0.75	0.75
SSTL2-1	2.5	2.5	1.25	1.25
SSTL3-1	3.3	3.3	1.5	1.5

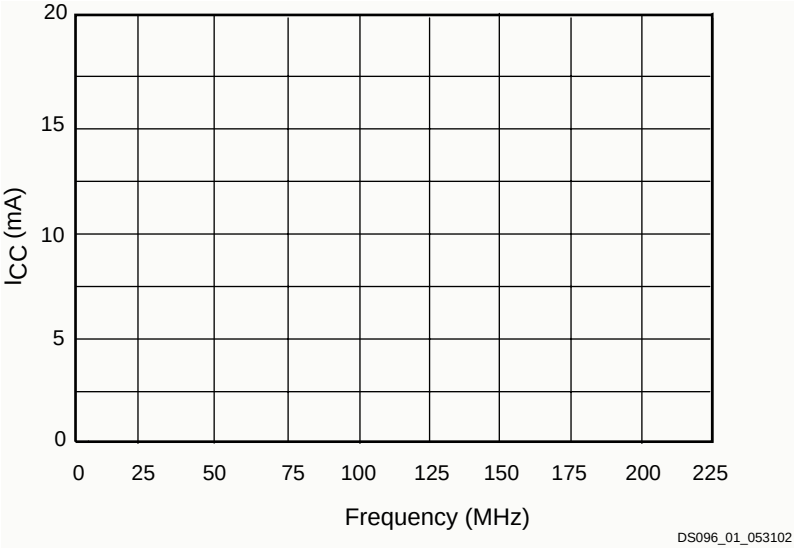


Figure 1: **I_{CC} vs Frequency**

Table 2: **I_{CC} vs Frequency (LVCMOS 1.8V T_A = 25°C)(1)**

	Frequency (MHz)								
	0	25	50	75	100	150	175	200	225
Typical -7.5, -10 I_{CC} (mA)									
Typical -6 I_{CC} (mA)									

Notes:
1. 16-bit up/down, resettable binary counter (one counter per function block).

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to ground	–0.5 to 2.0	V
V_{CCIO}	Supply voltage for output drivers	–0.5 to 4.0	V
V_{JTAG}	JTAG input voltage limits	-0.5 to 4.0	V
V_{AUX}	JTAG input supply voltage	-0.5 to 4.0	V
V_{IN}	Input voltage relative to ground(1)	–0.5 to 4.0	V
V_{TS}	Voltage applied to 3-state output(1)	–0.5 to 4.0	V
T_{STG}	Storage Temperature (ambient)	–65 to +150	°C
T_J	Junction Temperature	+150	°C

Notes:
1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easiest to achieve. During transitions, the device pins may undershoot to –2.0v or overshoot to +4.5V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
2. For soldering guidelines, see the Packaging Information on the Xilinx website.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply voltage for internal logic and input buffers	Commercial T_A = 0°C to +70°C	1.7	1.9	V
		Industrial T_A = –40°C to +85°C	1.7	1.9	V
V_{CCIO}	Supply voltage for output drivers @ 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers @ 2.5V operation		2.3	2.7	V
	Supply voltage for output drivers @ 1.8V operation		1.7	1.9	V
	Supply voltage for output drivers @ 1.5V operation		1.4	1.6	V
V_{AUX}	JTAG programming		1.7	3.6	V

DC Electrical Characteristics (Over Recommended Operating Conditions)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{CCSB}	Standby current (-7.5, -10)	V_{CC} = 1.9V, V_{CCIO} = 3.6V	-	100	µA
I_{CCSB}	Standby current (-6)	V_{CC} = 1.9V, V_{CCIO} = 3.6V			mA
I_{CC}	Dynamic current (-7.5, -10)	f = 1 MHz			mA
		f = 50 MHz			mA
I_{CC}	Dynamic current (-6)	f = 1 MHz			mA
		f = 50 MHz			mA
C_{JTAG}	JTAG input capacitance	f = 1 MHz	-	10	pF
C_{CLK}	Global clock input capacitance	f = 1 MHz	-	12	pF
C_{IO}	I/O capacitance	f = 1 MHz	-	10	pF

LVCMOS 3.3V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		3.0	3.6	V
V_{IH}	High level input voltage		2	V_{CCIO} + 0.3V	V
V_{IL}	Low level input voltage		–0.3	0.8	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 3V	V_{CCIO} – 0.4V	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 3V	V_{CCIO} – 0.2V	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 3V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 3V	-	0.2	V
I_{IL}	Input leakage current	V_{IN} = 0V or V_{CCIO} to 3.9V	–10	10	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0V or V_{CCIO} to 3.9V	–10	10	µA

LVCMOS 2.5V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		2.3	2.7	V
V_{IH}	High level input voltage		1.7	3.9	V
V_{IL}	Low level input voltage		–0.3	0.7	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 2.3V	V_{CCIO} – 0.4V	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 2.3V	V_{CCIO} – 0.2V	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 2.3V	-	0.4	V
		I_{OL} = 0.1mA, V_{CCIO} = 2.3V	-	0.2	V
I_{IL}	Input leakage current	V_{IN} = 0V or V_{CCIO} to 3.9V	–10	10	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0V or V_{CCIO} to 3.9V	–10	10	µA

LVCMOS 1.8V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		1.7	1.9	V
V_{IH}	High level input voltage		0.65 x V_{CCIO}	3.9	V
V_{IL}	Low level input voltage		–0.3	0.35 x V_{CCIO}	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 1.7V	V_{CCIO} – 0.45	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 1.7V	V_{CCIO} – 0.2	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 1.7V	-	0.45	V
		I_{OL} = 0.1 mA, V_{CCIO} = 1.7V	-	0.2	V
I_{IL}	Input leakage current	V_{IN} = 0 or V_{CCIO} to 3.9V	–10	10	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0 or V_{CCIO} to 3.9V	–10	10	µA

1.5V DC Voltage Specifications(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage		1.4	1.6	V
V_{IH}	High level input voltage		0.7 x V_{CCIO}	3.9	V
V_{IL}	Low level input voltage		–0.3	0.3	V
V_{OH}	High level output voltage	I_{OH} = –8 mA, V_{CCIO} = 1.4V	V_{CCIO} – 0.45	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 1.4V	V_{CCIO} – 0.2	-	V
V_{OL}	Low level output voltage	I_{OL} = 8 mA, V_{CCIO} = 1.4V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 1.4V	-	0.2	V
I_{IL}	Input leakage current	V_{IN} = 0 or V_{CCIO} to 3.9V	–10	10	µA
I_{IH}	I/O High-Z leakage	V_{IN} = 0 or V_{CCIO} to 3.9V	–10	10	µA

Notes:
1. Hysteresis used on 1.5V inputs.

AC Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	-6		-7.5		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
T_{PD1}	Propagation delay (single p-term)	-	5.7	-	7.1	-	9.2	ns
T_{PD2}	Propagation delay (OR array)	-	6.0	-	7.5	-	10.0	ns
T_{SUF}	Fast input register set-up time	2.2	-	2.4	-	2.7	-	ns
T_{SU1}	Setup time fast (single p-term)	2.3	-	2.6	-	3.1	-	ns
T_{SU2}	Setup time (OR array)	2.6	-	3.0	-	3.9	-	ns
T_{HF}	Fast input register hold time	0	-	0	-	0	-	ns
T_{H}	P-term hold time	0	-	0	-	0	-	ns
T_{CO}	Clock to output	-	4.4	-	5.8	-	7.8	ns
F_{TOGGLE}(1)	Internal toggle rate	-	416	-	250	-	166	MHz
$F_{SYSTEM1}$(2)	Maximum system frequency	-	217	-	179	-	128	MHz
$F_{SYSTEM2}$(2)	Maximum system frequency	-	204	-	167	-	116	MHz
F_{EXT1}(3)	Maximum external frequency	-	149	-	119	-	91	MHz
F_{EXT2}(3)	Maximum external frequency	-	143	-	114	-	85	MHz
T_{PSUF}	Fast input register p-term clock setup time	1.0	-	1.1	-	1.3	-	ns
T_{PSU1}	P-term clock setup time (single p-term)	1.1	-	1.3	-	1.7	-	ns
T_{PSU2}	P-term clock setup time (OR array)	1.4	-	1.7	-	2.5	-	ns
T_{PHF}	Fast input register p-term clock hold time	0.5	-	0.9	-	1.3	-	ns
T_{PH}	P-term clock hold	0.4	-	0.7	-	0.9	-	ns
T_{PCO}	P-term clock to output	-	5.6	-	7.1	-	9.3	ns
T_{OE}/T_{OD}	Global OE to output enable/disable	-	5.5	-	7.0	-	9.2	ns
T_{POE}/T_{POD}	P-term OE to output enable/disable	-	6.5	-	8.0	-	10.2	ns
T_{MOE}/T_{MOD}	Macrocell driven OE to output enable/disable	-	7.1	-	9.1	-	12.5	ns
T_{PAO}	P-term set/reset to output valid	-	7.4	-	8.9	-	11.6	ns
T_{AO}	Global set/reset to output valid	-	7.2	-	9.0	-	11.5	ns
T_{SUEC}	Register clock enable setup time	2.4	-	2.7	-	3.2	-	ns
T_{HEC}	Register clock enable hold time	0	-	0	-	0	-	ns
T_{CW}	Global clock pulse width High or Low	1.2	-	2.0	-	3.0	-	ns
T_{PCW}	P-term pulse width High or Low	6.0	-	7.5	-	10.0	-	ns
T_{DGSU}	Set-up before DataGATE latch assertion	7.0	-	9.0	-	10.0	-	ns
T_{DGHO}	Hold to DataGATE latch assertion	7.0	-	9.0	-	10.0	-	ns
T_{DGR}	DataGATE recovery to new data	-	7.0	-	9.0	-	11.0	ns
T_{DGW}	DataGATE high pulse width	2.5	-	3.0	-	5.0	-	ns
T_{CDRSU}	CDRST setup time before falling edge GCLK2	1.2	-	1.7	-	2.5	-	ns
T_{CDRHO}	Hold time CDRST after falling edge GCLK2	0	-	0	-	0	-	ns
T_{CONFIG}	Configuration time	-		-		-		us

Notes:

1. F_{TOOGLE} ($1/2*T_{CW}$) is the maximum frequency of a dual edge triggered T flip-flop with output enabled
2. $F_{SYSTEM1}$ ($1/T_{CYCLE}$) is the internal operating frequency for a device fully populated with 16-bit resettable binary counter through one p-term per macrocell while $F_{SYSTEM2}$ is through the OR array (one counter per function block).
3. F_{EXT1}($1/T_{SU2}+T_{CO}$) is the maximum external frequency using one p-term while F_{EXT2} is through the OR array

Internal Timing Parameters

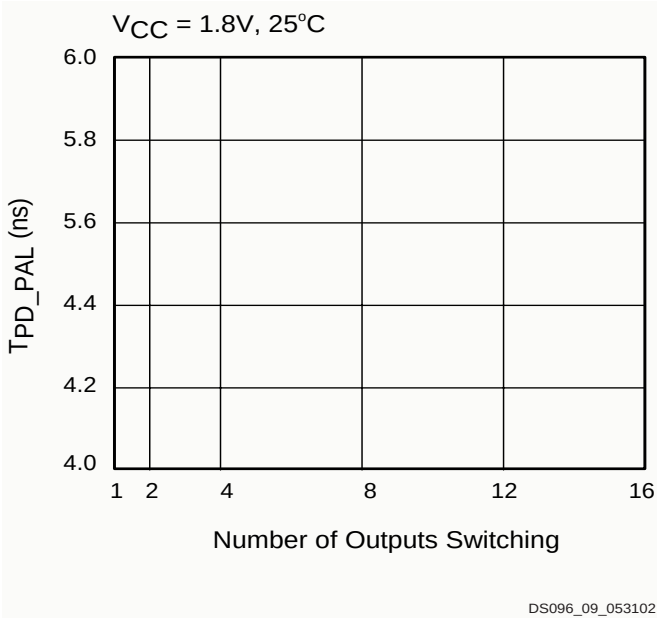
Symbol	Parameter[1]	-6		-7.5		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Buffer Delays								
T_{IN}	Input buffer delay	-	2.5	-	3.1	-	3.8	ns
T_{FIN}	Fast data register input delay	-	2.8	-	3.4	-	4.2	ns
T_{GCK}	Global Clock buffer delay	-	1.8	-	2.4	-	3.3	ns
T_{GSR}	Global set/reset buffer delay	-	2.8	-	3.8	-	4.6	ns
T_{GTS}	Global 3-state buffer delay	-	2.0	-	2.7	-	3.7	ns
T_{OUT}	Output buffer delay	-	2.4	-	3.0	-	3.9	ns
T_{EN}	Output buffer enable/disable delay	-	3.5	-	4.3	-	5.5	ns
P-term Delays								
T_{CT}	Control term delay	-	0.5	-	0.6	-	0.9	ns
T_{LOGI1}	Single P-term delay adder	-	0.4	-	0.5	-	0.8	ns
T_{LOGI2}	Multiple P-term delay adder	-	0.3	-	0.4	-	0.8	ns
Macrocell Delay								
T_{PDI}	Input to output valid	-	0.4	-	0.5	-	0.7	ns
T_{SUI}	Setup before clock	1.2	-	1.4	-	1.8	-	ns
T_{HI}	Hold after clock	0	-	0	-	0	-	ns
T_{ECSU}	Enable clock setup time	1.2	-	1.4	-	1.8	-	ns
T_{ECHO}	Enable clock hold time	0	-	0	-	0	-	ns
T_{COI}	Clock to output valid	-	0.2	-	0.4	-	0.7	ns
T_{AOI}	Set/reset to output valid	-	2.0	-	2.2	-	3.0	ns
T_{CDBL}	Clock doubler delay	-	0	-	0	-	0	ns
Feedback Delays								
T_{F}	Feedback delay	-	2.8	-	3.3	-	4.5	ns
T_{OEM}	Macrocell to global OE delay	-	1.6	-	2.0	-	3.0	ns
I/O Standard Time Adder Delays 1.5V CMOS								
T_{IN15}	Standard input adder	-	0.5	-	0.8	-	1.0	ns
T_{HYS15}	Hysteresis input adder	-	2.0	-	3.0	-	4.0	ns
T_{OUT15}	Output adder	-	0.5	-	0.8	-	1.0	ns
T_{SLEW15}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns
I/O Standard Time Adder Delays 1.8V CMOS								
T_{IN18}	Standard input adder	-	0	-	0	-	0	ns
T_{HYS18}	Hysteresis input adder	-	2.0	-	3.0	-	4.0	ns
T_{OUT18}	Output adder	-	0	-	0	-	0	ns
T_{SLEW}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns

Internal Timing Parameters *(Continued)*

Symbol	Parameter[1]	-6		-7.5		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
I/O Standard Time Adder Delays 2.5V CMOS								
T_{IN25}	Standard input adder	-	0.5	-	0.8	-	1.0	ns
T_{HYS25}	Hysteresis input adder	-	1.5	-	2.5	-	3.0	ns
T_{OUT25}	Output adder	-	1.5	-	2.5	-	3.0	ns
T_{SLEW25}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns
I/O Standard Time Adder Delays 3.3V CMOS/TTL								
T_{IN33}	Standard input adder	-	0.7	-	1.0	-	2.0	ns
T_{HYS33}	Hysteresis input adder	-	1.0	-	2.0	-	3.0	ns
T_{OUT33}	Output adder	-	1.0	-	2.0	-	3.0	ns
T_{SLEW33}	Output slew rate adder	-	2.0	-	3.0	-	4.0	ns
I/O Standard Time Adder Delays HSTL, SSTL								
SSTL2-1	Input adder to TIN, TFIN, TGCK, TGSR,TGTS	-	1.5	-	1.8	-	2.5	ns
	Output adder to TOUT	-	0	-	0	-	0	ns
SSTL3-1	Input adder to TIN, TFIN, TGCK, TGSR,TGTS	-	1.5	-	1.8	-	2.5	ns
	Output adder to TOUT	-	0	-	0	-	0	ns
HSTL-1	Input adder to TIN, TFIN, TGCK, TGSR,TGTS	-	1.5	-	1.8	-	2.5	ns
	Output adder to TOUT	-	0	-	0	-	0	ns

Notes:
1. 1.5 ns input pin signal rise/fall.

Switching Characteristics



Pin Descriptions

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
1(GTS0)	1	7	D4	C1	2
1	2	6	B2	C2	2
1(GTS3)	3	5	E3	B1	2
1	4	4	C3	B2	2
1	5	-	-	-	-
1	6	-	-	-	-
1	7	-	-	-	-
1	8	-	-	-	-
1	9	-	-	-	-
1	10	-	-	-	-
1	11	-	-	-	-
1	12	-	-	-	-
1(GTS2)	13	3	D3	D3	2
1	14	2	B3	C3	2
1	15	208	B4	A1	2
1(GRS)	16	206	C4	A2	2
2	1	-	A1	D2	2
2	2	8	-	D1	2
2	3	-	D2	F4	2
2	4	-	-	F3	2
2	5	-	-	-	-
2	6	-	-	-	-
2	7	-	-	-	-
2	8	-	-	-	-
2	9	-	-	-	-
2	10	-	-	-	-
2	11	-	-	-	-
2	12	-	-	-	-
2	13	-	C2	E2	2
2(GTS1)	14	9	E5	E1	2
2	15	10	B1	F2	2
2	16	12	E4	G4	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
3	1	205	-	B3	2
3	2	-	A2	C4	2
3	3	203	-	B4	2
3	4	-	C5	C5	2
3	5	202	A3	B5	2
3	6	-	-	-	-
3	7	-	-	-	-
3	8	-	-	-	-
3	9	-	-	-	-
3	10	-	-	-	-
3	11	-	-	-	-
3	12	-	-	-	-
3	13	201	E7	A3	2
3	14	-	A4	A4	2
3	15	200	C6	D6	2
3	16	199	B5	A5	2
4	1	-	C1	G3	2
4	2	14	E2	G2	2
4	3	-	F2	G1	2
4	4	15	E6	H4	2
4	5	-	-	-	-
4	6	-	-	-	-
4	7	-	-	-	-
4	8	-	-	-	-
4	9	-	-	-	-
4	10	-	-	-	-
4	11	-	-	-	-
4	12	-	-	-	-
4	13	-	F3	H3	2
4	14	16	D1	H2	2
4	15	17	G4	H1	2
4	16	18	E1	J4	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
5	1	198	D6	C6	2
5	2	197	A5	B6	2
5	3	196	E8	A6	2
5	4	195	B6	D7	2
5	5	194	C7	C7	2
5	6	-	-	-	-
5	7	-	-	-	-
5	8	-	-	-	-
5	9	-	-	-	-
5	10	-	-	-	-
5	11	-	-	-	-
5	12	-	-	-	-
5	13	193	-	B7	2
5	14	-	A6	A7	2
5	15	192	D7	D8	2
5	16	-	B7	C8	2
6	1	19	G3	J3	2
6	2	20	G2	J2	2
6	3	21	-	J1	2
6	4	-	F5	K4	2
6	5	-	-	-	-
6	6	-	-	-	-
6	7	-	-	-	-
6	8	-	-	-	-
6	9	-	-	-	-
6	10	-	-	-	-
6	11	-	-	-	-
6	12	-	-	-	-
6	13	-	-	K3	2
6	14	-	F1	K2	2
6	15	-	-	K1	2
6	16	-	G5	L1	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
7	1	191	-	B8	2
7	2	-	E9	A8	2
7	3	189	A7	D9	2
7	4	188	D8	C9	2
7	5	187	B8	B9	2
7	6	-	-	-	-
7	7	-	-	-	-
7	8	-	-	-	-
7	9	-	-	-	-
7	10	-	-	-	-
7	11	-	-	-	-
7	12	-	-	-	-
7	13	186	C8	A9	2
7	14	185	A8	D10	2
7	15	184	E11	C10	2
7	16	183	E10	B10	2
8	1	-	H2	L4	2
8	2	22	-	L3	2
8	3	23	H4	L2	2
8	4	-	-	M1	2
8	5	-	-	-	-
8	6	-	-	-	-
8	7	-	-	-	-
8	8	-	-	-	-
8	9	-	-	-	-
8	10	-	-	-	-
8	11	-	-	-	-
8	12	-	-	-	-
8	13	-	G1	M2	2
8	14	25	H3	M3	2
8	15	-	H1	M4	2
8	16	-	H5	N1	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
9	1	-	-	AA2	1
9	2	50	N3	AB1	1
9	3	49	-	AA1	1
9	4	48	-	W4	1
9	5	-	-	-	-
9	6	-	-	-	-
9	7	-	-	-	-
9	8	-	-	-	-
9	9	-	-	-	-
9	10	-	-	-	-
9	11	-	-	-	-
9	12	-	-	-	-
9	13	-	R1	Y3	1
9	14	47	N4	Y2	1
9	15	-	N2	W3	1
9(GCK1)	16	46	M3	Y1	1
10(CDRST)	1	51	P2	AB2	1
10	2	54	P4	Y4	1
10(GCK2)	3	55	P5	AB3	1
10	4	56	R2	AA4	1
10	5	-	-	-	-
10	6	-	-	-	-
10	7	-	-	-	-
10	8	-	-	-	-
10	9	-	-	-	-
10	10	-	-	-	-
10	11	-	-	-	-
10	12	-	-	-	-
10	13	57	T1	Y5	1
10(DGE)	14	58	T2	AA5	1
10	15	-	-	AB4	1
10	16	-	N5	W6	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
11	1	45	P1	W2	1
11	2	-	M4	W1	1
11(GCK0)	3	44	M2	V3	1
11	4	43	L3	U4	1
11	5	-	-	-	-
11	6	-	-	-	-
11	7	-	-	-	-
11	8	-	-	-	-
11	9	-	-	-	-
11	10	-	-	-	-
11	11	-	-	-	-
11	12	-	-	-	-
11	13	41	N1	V2	1
11	14	40	L4	V1	1
11	15	39	M1	U3	1
11	16	38	L5	U2	1
12	1	60	R4	AB5	1
12	2	61	M5	Y6	1
12	3	62	R5	AA6	1
12	4	63	R6	AB6	1
12	5	64	-	W7	1
12	6	-	-	-	-
12	7	-	-	-	-
12	8	-	-	-	-
12	9	-	-	-	-
12	10	-	-	-	-
12	11	-	-	-	-
12	12	-	-	-	-
12	13	65	N6	Y7	1
12	14	66	-	AA7	1
12	15	67	R3	AB7	1
12	16	-	-	W8	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
13	1	37	-	U1	1
13	2	-	K4	T4	1
13	3	36	L2	T3	1
13	4	35	-	T2	1
13	5	-	-	-	-
13	6	-	-	-	-
13	7	-	-	-	-
13	8	-	-	-	-
13	9	-	-	-	-
13	10	-	-	-	-
13	11	-	-	-	-
13	12	-	-	-	-
13	13	-	K3	T1	1
13	14	34	L1	R4	1
13	15	32	K5	R3	1
13	16	-	K2	R2	1
14	1	-	M6	Y8	1
14	2	-	-	AA8	1
14	3	69	T3	AB8	1
14	4	70	P6	W9	1
14	5	71	T4	Y9	1
14	6	-	-	-	-
14	7	-	-	-	-
14	8	-	-	-	-
14	9	-	-	-	-
14	10	-	-	-	-
14	11	-	-	-	-
14	12	-	-	-	-
14	13	72	P7	AA9	1
14	14	-	-	AB9	1
14	15	73	T5	W10	1
14	16	-	-	Y1-	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
15	1	31	J4	R1	1
15	2	-	K1	P4	1
15	3	30	J3	P3	1
15	4	29	J2	P2	1
15	5	-	-	-	-
15	6	-	-	-	-
15	7	-	-	-	-
15	8	-	-	-	-
15	9	-	-	-	-
15	10	-	-	-	-
15	11	-	-	-	-
15	12	-	-	-	-
15	13	28	J5	P1	1
15	14	27	J1	N4	1
15	15	-	-	N3	1
15	16	-	-	N2	1
16	1	74	N7	AA10	1
16	2	-	-	AB10	1
16	3	75	R7	AB11	1
16	4	76	M7	W11	1
16	5	77	T6	AA11	1
16	6	-	-	-	-
16	7	-	-	-	-
16	8	-	-	-	-
16	9	-	-	-	-
16	10	-	-	-	-
16	11	-	-	-	-
16	12	-	-	-	-
16	13	-	-	Y11	1
16	14	78	-	AB12	1
16	15	-	-	AA12	1
16	16	-	-	Y12	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
17	1	161	A16	A21	4
17	2	162	B13	B20	4
17	3	163	-	C19	4
17	4	164	-	B19	4
17	5	165	B14	C18	4
17	6	-	-	-	-
17	7	-	-	-	-
17	8	-	-	-	-
17	9	-	-	-	-
17	10	-	-	-	-
17	11	-	-	-	-
17	12	-	-	-	-
17	13	166	C13	B18	4
17	14	167	A15	A19	4
17	15	168	C12	D17	4
17	16	169	B12	A18	4
18	1	160	B15	A22	4
18	2	-	C14	B21	4
18	3	-	G11	B22	4
18	4	159	B16	C20	4
18	5	-	-	-	-
18	6	-	-	-	-
18	7	-	-	-	-
18	8	-	-	-	-
18	9	-	-	-	-
18	10	-	-	-	-
18	11	-	-	-	-
18	12	-	-	-	-
18	13	-	-	C21	4
18	14	-	D14	D19	4
18	15	158	-	D20	4
18	16	-	C15	C22	4

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
19	1	170	D13	C17	4
19	2	171	A14	B17	4
19	3	173	E13	A17	4
19	4	-	A13	D16	4
19	5	-	C11	C16	4
19	6	-	-	-	-
19	7	-	-	-	-
19	8	-	-	-	-
19	9	-	-	-	-
19	10	-	-	-	-
19	11	-	-	-	-
19	12	-	-	-	-
19	13	-	A12	B16	4
19	14	-	B11	A16	4
19	15	-	D11	D15	4
19	16	-	A11	C15	4
20	1	-	G12	D21	4
20	2	-	D15	D22	4
20	3	155	E14	E20	4
20	4	154	C16	F19	4
20	5	-	-	-	-
20	6	-	-	-	-
20	7	-	-	-	-
20	8	-	-	-	-
20	9	-	-	-	-
20	10	-	-	-	-
20	11	-	-	-	-
20	12	-	-	-	-
20	13	153	F14	E21	4
20	14	152	D16	E22	4
20	15	151	F13	F20	4
20	16	150	E15	F21	4

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
21	1	-	D10	B15	4
21	2	174	B10	A15	4
21	3	175	E12	D14	4
21	4	-	F12	B14	4
21	5	178	-	A14	4
21	6	-	-	-	-
21	7	-	-	-	-
12	8	-	-	-	-
21	9	-	-	-	-
21	10	-	-	-	-
21	11	-	-	-	-
21	12	-	-	-	-
21	13	-	-	D13	4
21	14	-	-	C13	4
21	15	-	-	B13	4
21	16	-	-	A13	4
22	1	149	G13	F22	4
22	2	148	F15	G19	4
22	3	147	G14	G20	4
22	4	146	E16	G21	4
22	5	-	-	-	-
22	6	-	-	-	-
22	7	-	-	-	-
22	8	-	-	-	-
22	9	-	-	-	-
22	10	-	-	-	-
22	11	-	-	-	-
22	12	-	-	-	-
22	13	145	H12	G22	4
22	14	144	F16	H19	4
22	15	143	H16	H20	4
22	16	142	-	H21	4

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
23	1	179	B9	A12	4
23	2	180	-	D12	4
23	3	-	C9	B12	4
23	4	182	-	C12	4
23	5	-	C10	A11	4
23	6	-	-	-	-
23	7	-	-	-	-
23	8	-	-	-	-
23	9	-	-	-	-
23	10	-	-	-	-
23	11	-	-	-	-
23	12	-	-	-	-
23	13	-	-	B11	4
23	14	-	A9	C11	4
23	15	-	-	D11	4
23	16	-	D9	A10	4
24	1	140	G15	H22	4
24	2	139	H13	J19	4
24	3	138	G16	J20	4
24	4	137	H14	J21	4
24	5	-	-	-	-
24	6	-	-	-	-
24	7	-	-	-	-
24	8	-	-	-	-
24	9	-	-	-	-
24	10	-	-	-	-
24	11	-	-	-	-
24	12	-	-	-	-
24	13	136	H15	J22	4
24	14	135	J12	K19	4
24	15	134	K12	K20	4
24	16	-	J16	K21	4

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
25	1	110	R16	W22	3
25	2	111	N15	V20	3
25	3	112	M15	V21	3
25	4	113	M13	U19	3
25	5	-	-	-	-
25	6	-	-	-	-
25	7	-	-	-	-
25	8	-	-	-	-
25	9	-	-	-	-
25	10	-	-	-	-
25	11	-	-	-	-
25	12	-	-	-	-
25	13	114	P16	V22	3
25	14	115	N16	U20	3
25	15	116	L14	U21	3
25	16	117	M14	U22	3
26	1	109	N14	Y22	3
26	2	108	T16	W21	3
26	3	107	R15	W20	3
26	4	106	P15	Y21	3
26	5	-	P14	Y20	3
26	6	-	-	-	-
26	7	-	-	-	-
26	8	-	-	-	-
26	9	-	-	-	-
26	10	-	-	-	-
26	11	-	-	-	-
26	12	-	-	-	-
26	13	103	P13	AA22	3
26	14	102	R13	AB22	3
26	15	101	N13	AA21	3
26	16	100	R14	AB21	3

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
27	1	118	L15	T19	3
27	2	-	L13	T20	3
27	3	119	M12	T21	3
27	4	120	M16	T22	3
27	5	-	-	-	-
27	6	-	-	-	-
27	7	-	-	-	-
27	8	-	-	-	-
27	9	-	-	-	-
27	10	-	-	-	-
27	11	-	-	-	-
27	12	-	-	-	-
27	13	-	K14	R19	3
27	14	-	-	R20	3
27	15	121	-	R21	3
27	16	-	-	R22	3
28	1	99	T15	W19	3
28	2	97	R12	AA20	3
28	3	95	T14	Y18	3
28	4	-	N11	AA19	3
28	5	-	P11	W17	3
28	6	-	-	-	-
28	7	-	-	-	-
28	8	-	-	-	-
28	9	-	-	-	-
28	10	-	-	-	-
28	11	-	-	-	-
28	12	-	-	-	-
28	13	-	M11	Y17	3
28	14	-	T13	AA18	3
28	15	-	N10	AB18	3
28	16	-	-	AA17	3

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
29	1	-	L16	P19	3
29	2	-	-	P20	3
29	3	122	-	P21	3
29	4	123	-	P22	3
29	5	-	-	-	-
29	6	-	-	-	-
29	7	-	-	-	-
29	8	-	-	-	-
29	9	-	-	-	-
29	10	-	-	-	-
29	11	-	-	-	-
29	12	-	-	-	-
29	13	-	-	N19	3
29	14	125	K15	N21	3
29	15	-	L12	N22	3
29	16	-	-	M22	3
30	1	-	-	AB17	3
30	2	91	T12	W16	3
30	3	90	P10	Y16	3
30	4	89	T11	AA16	3
30	5	-	R10	AB16	3
30	6	-	-	-	-
30	7	-	-	-	-
30	8	-	-	-	-
30	9	-	-	-	-
30	10	-	-	-	-
30	11	-	-	-	-
30	12	-	-	-	-
30	13	88	M10	W15	3
30	14	87	T10	Y15	3
30	15	-	M9	AA15	3
30	16	86	R9	AB15	3

Pin Descriptions *(Continued)*

Function Block	Macro-cell	PQ208	FT256	FG324	I/O Bank
31	1	126	K16	M19	3
31	2	-	-	M20	3
31	3	127	-	M21	3
31	4	128	J14	L22	3
31	5	-	-	-	-
31	6	-	-	-	-
31	7	-	-	-	-
31	8	-	-	-	-
31	9	-	-	-	-
31	10	-	-	-	-
31	11	-	-	-	-
31	12	-	-	-	-
31	13	-	-	L21	3
31	14	-	J15	L20	3
31	15	-	-	L19	3
31	16	131	J13	K22	3
32	1	85	P9	W14	3
32	2	84	N9	Y14	3
32	3	-	T9	AA14	3
32	4	83	M8	AB14	3
32	5	-	T8	W13	3
32	6	-	-	-	-
32	7	-	-	-	-
32	8	-	-	-	-
32	9	-	-	-	-
32	10	-	-	-	-
32	11	-	-	-	-
32	12	-	-	-	-
32	13	82	P8	Y13	3
32	14	80	R8	AA13	3
32	15	-	T7	AB13	3
32	16	-	N8	W12	3

Notes:

1. GTS = global output enable, GSR = global reset/set, GCK = global clock, CDRST = clock divide reset, DGE = DataGATE enable.

XC2C512 JTAG, Power/Ground, No Connect Pins and Total User I/O

Pin Type	PQ208	FT256	FG324
TCK	98	P12	Y19
TDI	94	R11	AB19
TDO	176	A10	C14
TMS	96	N12	AB20
V_{AUX} (JTAG supply voltage)	11	F4	F1
Power internal (V_{CC})	1, 53, 124	P3, K13, D12, D5	E3, AA3, N20, A20, D4
Power Bank 1 I/O (V_{CCIO1})	33,59,79	J6, K6, L7, L8	M9, N9, P10, P11
Power Bank 2 I/O (V_{CCIO2})	26, 204	F7, F8, G6, H6	J10,J11, K9, L9
Power Bank 3 I/O (V_{CCIO3})	92, 105, 132	J11, K11, L9, L10	M14, N14, P12, P13
Power Bank 4 I/O (V_{CCIO4})	133, 157, 172, 181	F9, F10, H11	J12, J13, K14, L14
Ground	13, 24, 42, 52, 68, 81, 93, 104, 129, 130, 141, 156, 177, 190, 207	F6, F11, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, L6, L11	D5, D18, E4, E19, J9, J14, K10, K11, K12, K13, L10, L11, L12, L13, M10, M11, M12, M13, N10, N11, N12, N13, P9, P14, V4, V19, W5, W18
No connects	-	-	-
Total user I/O (includes dual function pins)	173	212	270

Ordering Information

Part Number	Pin/Ball Spacing	θ_{JA} (C/Watt)	θ_{JC} (C/Watt)	Package Type	Package Dimensions	I/O	Commercial (C) Industrial (I)
XC2C512-6PQ208	0.5mm	35.1	7.2	Plastic Quad Flat Pack	28mm x 28mm	173	C
XC2C512-7PQ208	0.5mm	35.1	7.2	Plastic Quad Flat Pack	28mm x 28mm	173	C
XC2C512-10PQ208	0.5mm	35.1	7.2	Plastic Quad Flat Pack	28mm x 28mm	173	C
XC2C512-6FT256	1.0mm	32.2	4.9	Fine Pitch Thin BGA	17mm x 17mm	212	C
XC2C512-7FT256	1.0mm	32.2	4.9	Fine Pitch Thin BGA	17mm x 17mm	212	C
XC2C512-10FT256	1.0mm	32.2	4.9	Fine Pitch Thin BGA	17mm x 17mm	212	C
XC2C512-6FG324	1.0mm	39.1	5.0	Fine Pitch BGA	23mm x 23mm	270	C
XC2C512-7FG324	1.0mm	39.1	5.0	Fine Pitch BGA	23mm x 23mm	270	C
XC2C512-10FG324	1.0mm	39.1	5.0	Fine Pitch BGA	23mm x 23mm	270	C
XC2C512-10PQ208	0.5mm	35.1	7.2	Plastic Quad Flat Pack	28mm x 28mm	173	I
XC2C512-10FT256	1.0mm	32.2	4.9	Fine Pitch Thin BGA	17mm x 17mm	212	I
XC2C512-10FG324	1.0mm	39.1	5.0	Fine Pitch BGA	23mm x 23mm	270	I

Notes:
1. C = Commercial (T_A = 0°C to +70° C); I = Industrial (T_A = –40°C to +85°C).

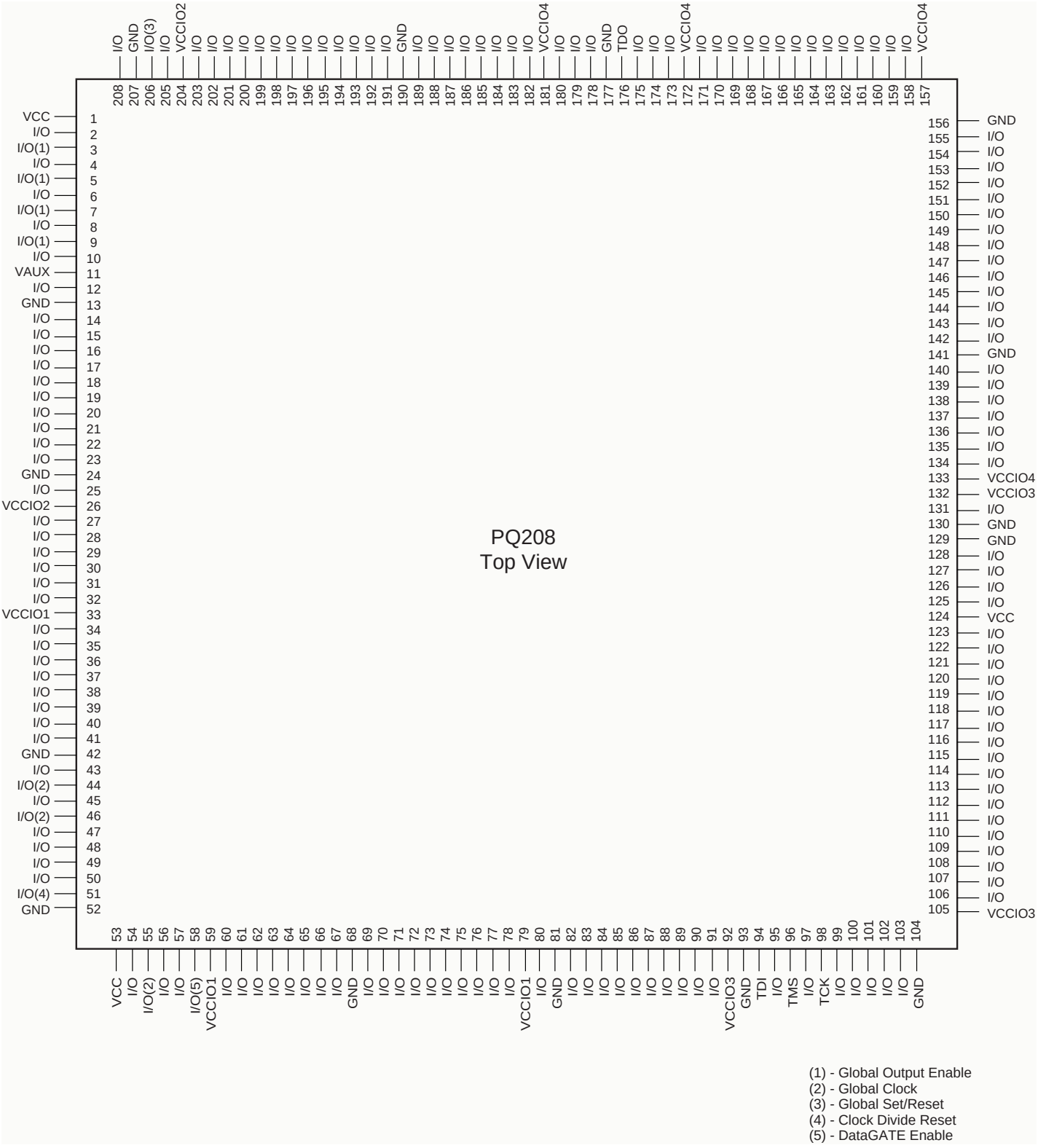
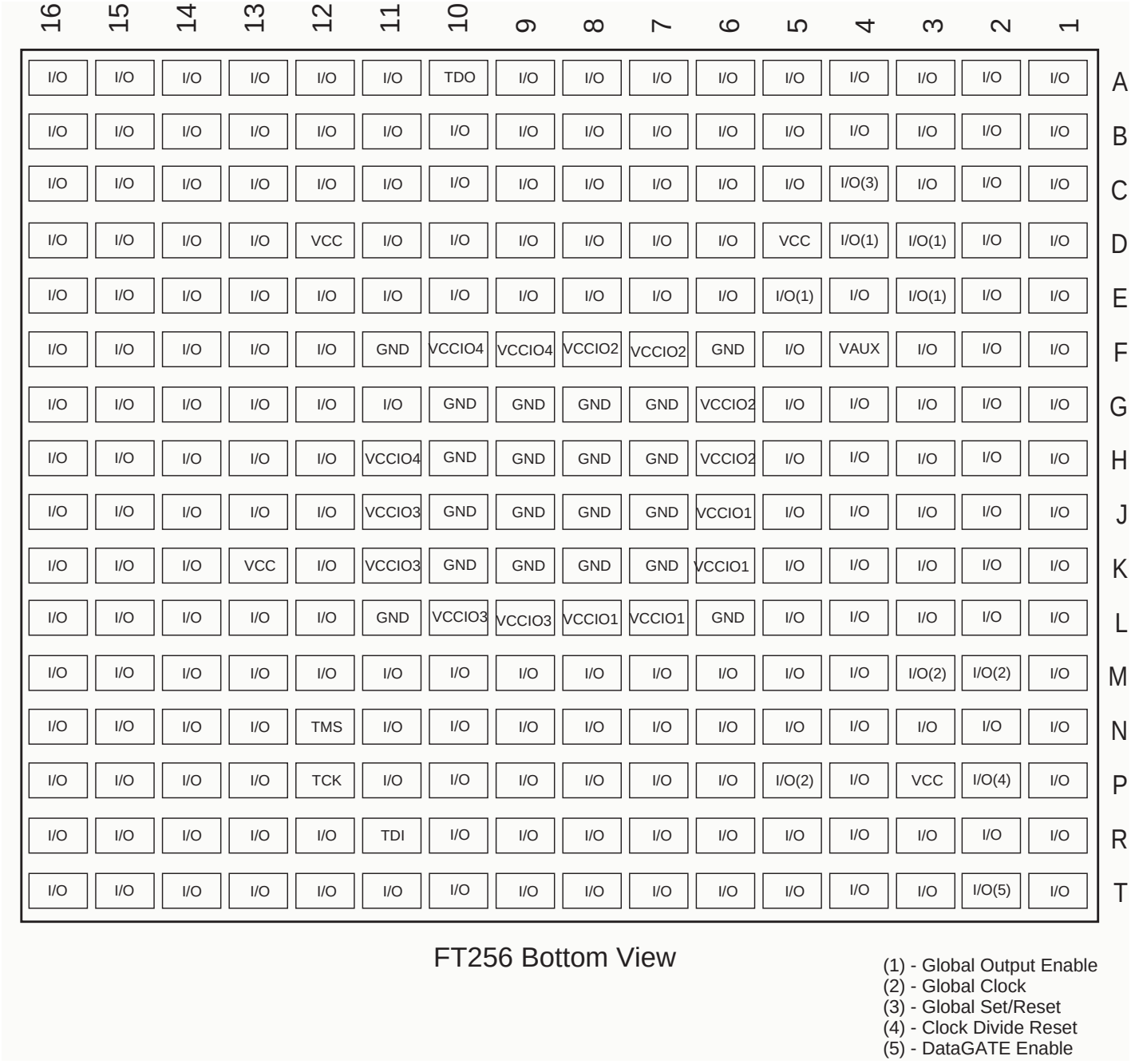


Figure 2: **PQ208 Plastic Quad Flat Pack**



FT256 Bottom View

(1) - Global Output Enable
(2) - Global Clock
(3) - Global Set/Reset
(4) - Clock Divide Reset
(5) - DataGATE Enable

Figure 3: **FT256 Fine Pitch Thin BGA**

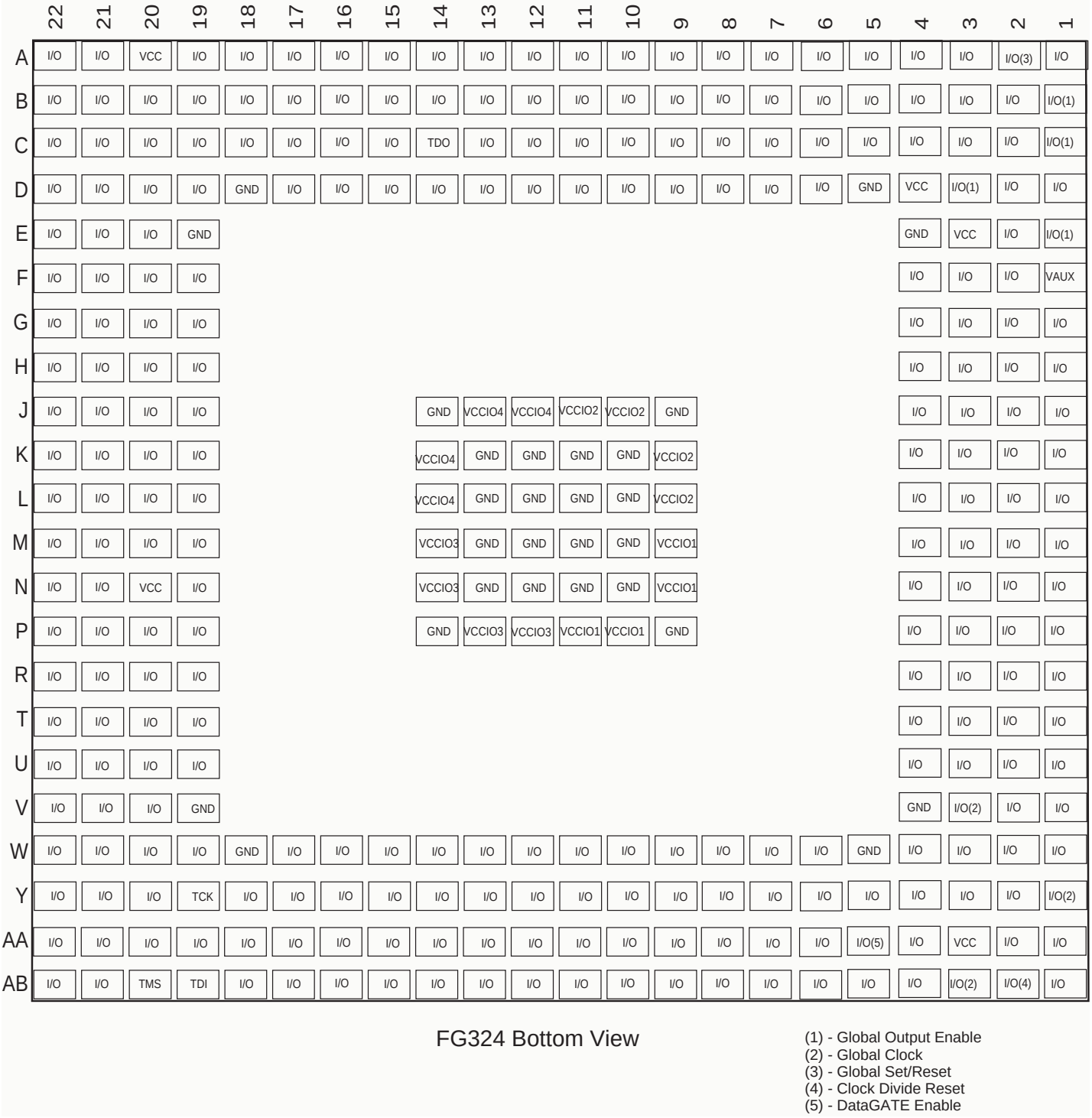


Figure 4: **FG3234 Fine Pitch BGA**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/19/02	1.0	Initial Xilinx release.