



UC1861-1868
UC2861-2868
UC3861-3868

Resonant-Mode Power Supply Controllers

FEATURES

- Controls Zero Current Switched (ZCS) or Zero Voltage Switched (ZVS) Quasi-Resonant Converters
- Zero-Crossing Terminated One-Shot Timer
- Precision 1%, Soft-Started 5V Reference
- Programmable Restart Delay Following Fault
- Voltage-Controlled Oscillator (VCO) with Programmable Minimum and Maximum Frequencies from 10kHz to 1MHz
- Low Start-Up Current (150μA typical)
- Dual 1 Amp Peak FET Drivers
- UVLO Option for Off-Line or DC/DC Applications

DESCRIPTION

The UC1861-1868 family of ICs is optimized for the control of Zero Current Switched and Zero Voltage Switched quasi-resonant converters. Differences between members of this device family result from the various combinations of UVLO thresholds and output options. Additionally, the one-shot pulse steering logic is configured to program either on-time for ZCS systems (UC1865-1868), or off-time for ZVS applications (UC1861-1864).

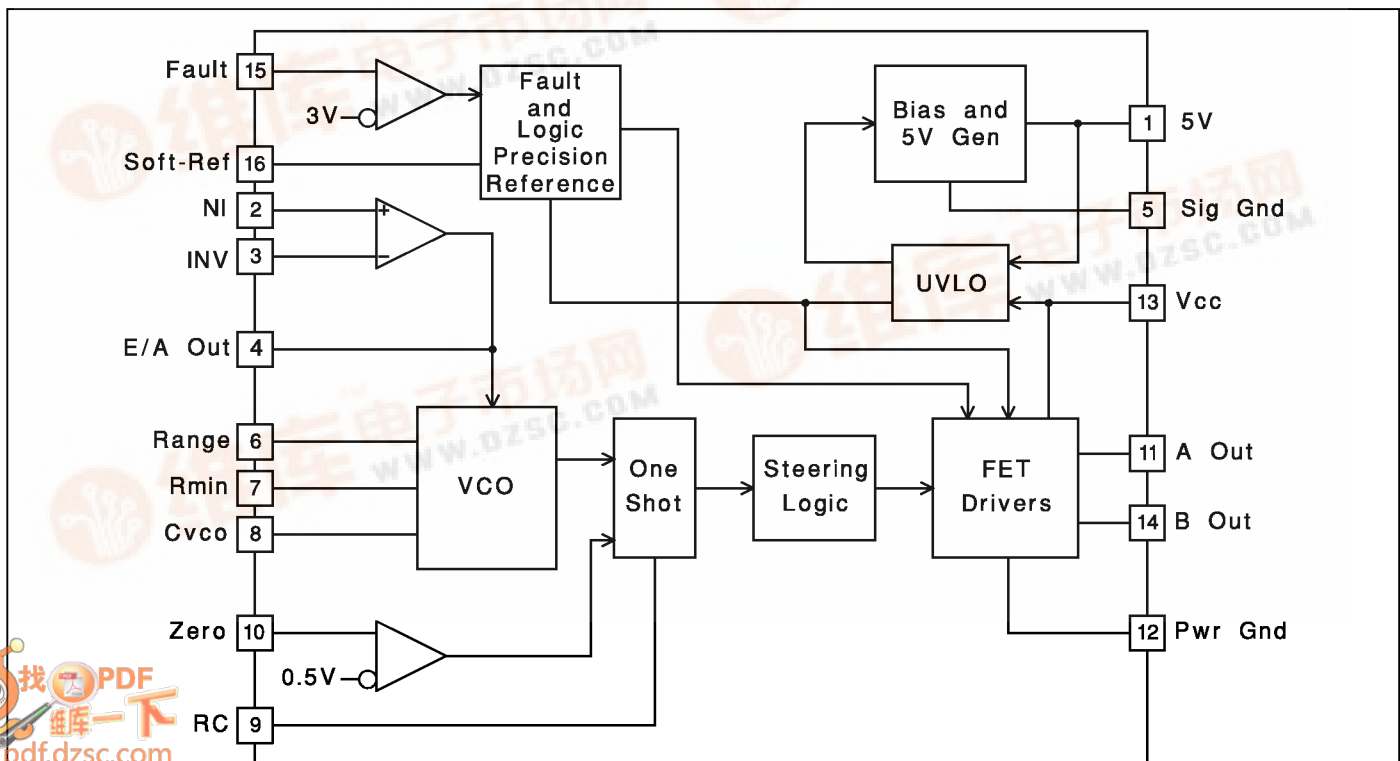
The primary control blocks implemented include an error amplifier to compensate the overall system loop and to drive a voltage controlled oscillator (VCO), featuring programmable minimum and maximum frequencies. Triggered by the VCO, the one-shot generates pulses of a programmed maximum width, which can be modulated by the Zero Detection comparator. This circuit facilitates "true" zero current or voltage switching over various line, load, and temperature changes, and is also able to accommodate the resonant components' initial tolerances.

Under-Voltage Lockout is incorporated to facilitate safe starts upon power-up. The supply current during the under-voltage lockout period is typically less than 150μA, and the outputs are actively forced to the low state.

(continued)

Device	1861	1862	1863	1864	1865	1866	1867	1868
UVLO	16.5/10.5	16.5/10.5	360/14	360/14	16.5/10.5	16.5/10.5	360/14	360/14
Outputs	Alternating	Parallel	Alternating	Parallel	Alternating	Parallel	Alternating	Parallel
"Fixed"	Off Time	Off Time	Off Time	Off Time	On Time	On Time	On Time	On Time

BLOCK DIAGRAM



DESCRIPTION (cont.)

UVLO thresholds for the UC1861/62/65/66 are 16.5V (ON) and 10.5V (OFF), whereas the UC1863/64/67/68 thresholds are 8V (ON) and 7V (OFF). After V_{CC} exceeds the UVLO threshold, a 5V generator is enabled which provides bias for the internal circuits and up to 10mA for external usage.

A Fault comparator serves to detect fault conditions and set a latch while forcing the output drivers low. The Soft-Ref pin serves three functions: providing soft start, re-

start delay, and the internal system reference.

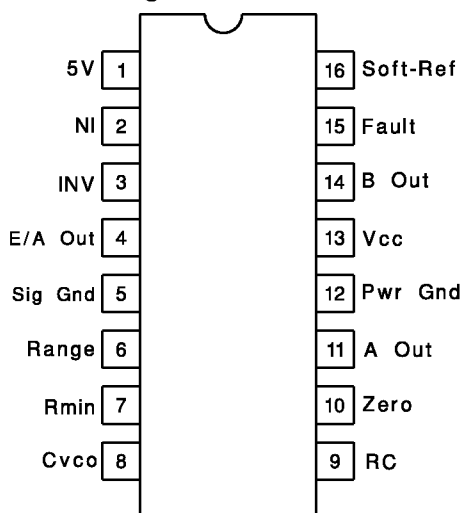
Each device features dual 1 Amp peak totem pole output drivers for direct interface to power MOSFETS. The outputs are programmed to alternate in the UC1861/63/65/67 devices. The UC1862/64/66/68 outputs operate in unison allowing a 2 Amp peak current.

ABSOLUTE MAXIMUM RATINGS

V_{CC}	22V
Output Current	
Source or Sink (Pins 11 & 14)	0.5A
DC Pulse (0.5 μ s)	1.5A
Power Ground Voltage	± 0.2 V
Inputs (Pins 2, 3, 10, & 15)	-0.4 to 7V
Error Amp Output Current	± 2 mA
Power Dissipation	1W
Junction Temperature (Operating)	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

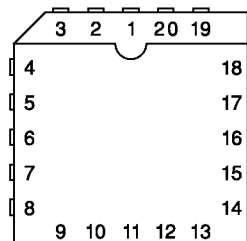
All voltages are with respect to signal ground and all currents are positive into the specified terminal. Pin numbers refer to the J and N packages. Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

DIL-16, SOIC-16 (Top View)
J or N, DW Packages



CONNECTION DIAGRAMS

PLCC-20 & LCC-20 (Top View)
Q & L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
Soft Ref	1
5V	2
NI	3
INV	4
E/A Out	5
Sig Gnd	6
Range	7
RMIN	8
Cvco	9
RC	10
Zero	11
NC	12
NC	13
A Out	14
Pwr Gnd	15
Pwr Gnd	16
Vcc	17
B Out	18

UC1861-1868
UC2861-2868
UC3861-3868

ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications apply for $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ for the UC186x, $-25^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ for the UC286x, and $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ for the UC386x, $V_{CC}=12\text{V}$, $C_{VCO}=1\text{nF}$, $\text{Range}=7.15\text{k}$, $R_{\text{MIN}}=86.6\text{k}$, $C=200\text{pF}$, $R=4.02\text{k}$, and $C_{\text{sr}}=0.1\mu\text{F}$. $T_A=T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
5V Generator					
Output Voltage	$12\text{V} \leq V_{CC} \leq 20\text{V}$, $-10\text{mA} \leq I_O \leq 0\text{mA}$	4.8	5.0	5.2	V
Short Circuit Current	$V_O = 0\text{V}$	-150		-15	mA
Soft-Reference					
Restart Delay Current	$V = 2\text{V}$	10	20	35	μA
Soft Start Current	$V = 2\text{V}$	-650	-500	-350	μA
Reference Voltage	$T_J = 25^{\circ}\text{C}$, $I_O = 0\text{A}$	4.95	5.00	5.05	V
	$12\text{V} \leq V_{CC} \leq 20\text{V}$, $-200\mu\text{A} \leq I_O \leq 200\mu\text{A}$	4.85		5.15	V
Line Regulation	$12\text{V} \leq V_{CC} \leq 20\text{V}$		2	20	mV
Load Regulation	$-200\mu\text{A} \leq I_O \leq 200\mu\text{A}$		10	30	mV
Error Amplifier (Note 3)					
Input Offset Voltage	$V_{CM} = 5\text{V}$, $V_O = 2\text{V}$, $I_O = 0\text{A}$	-10		10	mV
Input Bias Current	$V_{CM} = 0\text{V}$	-2.0	-0.3		μA
Voltage Gain	$V_{CM} = 5\text{V}$, $0.5\text{V} \leq V_O \leq 3.7\text{V}$, $I_O = 0\text{A}$	70	100		dB
Power Supply Rejection Ratio	$V_{CM} = 5\text{V}$, $V_O = 2\text{V}$, $12\text{V} \leq V_{CC} \leq 20\text{V}$	70	100		dB
Error Amplifier (Note 3) (cont.)					
Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 6\text{V}$, $V_O = 2\text{V}$	65	100		dB
V_{OUT} Low	$V_{ID} = -100\text{mV}$, $I_O = 200\mu\text{A}$		0.17	0.25	V
V_{OUT} High	$V_{ID} = 100\text{mV}$, $I_O = -200\mu\text{A}$	3.9	4.2		V
Unity Gain Bandwidth	(Note 4)	0.5	0.8		MHz
Voltage Controlled Oscillator					
Maximum Frequency	V_{ID} (Error Amp) = 100mV, $T_J = 25^{\circ}\text{C}$	450	500	550	kHz
	V_{ID} (Error Amp) = 100mV	425		575	kHz
Minimum Frequency	V_{ID} (Error Amp) = -100mV, $T_J = 25^{\circ}\text{C}$	45	50	55	kHz
	V_{ID} (Error Amp) = -100mV	42		58	kHz
One Shot					
Zero Comparator V_{th}		0.45	0.50	0.55	V
Propagation Delay	(Note 4)		120	200	ns
Maximum Pulse Width	$V_{ZERO} = 1\text{V}$	850	1000	1150	ns
Maximum to Minimum Pulse Width Ratio	$V_{ZERO} = 0\text{V}$ UCx861 – UCx864	2.5	4	5.5	
	$V_{ZERO} = 0\text{V}$ UCx865 – UCx868, -55°C to $+85^{\circ}\text{C}$	4	5.5	7	
	$V_{ZERO} = 0\text{V}$ UCx865 – UCx868, $+125^{\circ}\text{C}$	3.8	5.5	7	
Output Stage					
Rise and Fall Time	$C_{LOAD} = 1\text{nF}$ (Note 4)		25	45	ns
Output Low Saturation	$I_O = 20\text{mA}$		0.2	0.5	V
	$I_O = 200\text{mA}$		0.5	2.2	V
Output High Saturation	$I_O = -200\text{mA}$, down from V_{CC}		1.7	2.5	V
UVLO Low Saturation	$I_O = 20\text{mA}$		0.8	1.5	V
Fault Comparator					
Fault Comparator V_{th}		2.85	3.00	3.15	V
Delay to Output	(Note 4) (Note 5)		100	200	ns

ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications apply for $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ for the UC186x, $-25^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ for the UC286x, and $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ for the UC386x, $V_{CC}=12\text{V}$, $C_{VCO}=1\text{nF}$, $\text{Range}=7.15\text{k}$, $R_{\text{MIN}}=86.6\text{k}$, $C=200\text{pF}$, $R=4.02\text{k}$, and $C_{sr}=0.1\mu\text{F}$. $T_A=T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UVLO					
V _{CC} Turn-on Threshold	UCx861, UCx862, UCx865, UCx866	15	16.5	18	V
	UCx863, UCx864, UCx867, UCx868	7	8.0	9	V
V _{CC} Turn-off Threshold	UCx861, UCx862, UCx865, UCx866	9.5	10.5	11.5	V
	UCx863, UCx864, UCx867, UCx868	6	7.0	8	V
I _{CC} Start	$V_{CC} = V_{CC(\text{on})} - 0.3\text{V}$		150	300	μA
I _{CC} Run	$V_{ID} = 100\text{mV}$		25	32	mA

Note 1: Currents are defined as positive into the pin.

Note 2: Pulse measurement techniques are used to insure that $T_J = T_A$.

Note 3: $V_{ID} = V(\text{NI}) - V(\text{INV})$.

Note 4: This parameter is not 100% tested in production but guaranteed by design.

Note 5: $V_i = 0$ to 4V $t_r(V_i) = 10\text{ns}$ $t_{pd} = t(V_o = 6\text{V}) - t(V_i = 3\text{V})$

APPLICATION INFORMATION

UVLO & 5V GENERATOR (See Figure 1): When power is applied to the chip and V_{CC} is less than the upper UVLO threshold, I_{CC} will be less than 300 μA , the 5V generator will be off, and the outputs will be actively held low.

When V_{CC} exceeds the upper UVLO threshold, the 5V generator turns on. Until the 5V pin exceeds 4.9V, the outputs will still remain low.

The 5V pin should be bypassed to signal ground with a 0.1 μF capacitor. The capacitor should have low equivalent series resistance and inductance.

FAULT AND SOFT-REFERENCE (See Figure 1): The Soft-Ref pin serves three functions: system reference, restart delay, and soft-start. Designed to source or sink 200 μA , this pin should be used as the input reference for the error amplifier circuit. This pin requires a bypass capacitor of at least 0.1 μF . This yields a minimum soft-start time of 1ms.

Under-Voltage Lockout sets both the fault and restart delay latches. This holds the outputs low and discharges the Soft-Ref pin. After UVLO, the fault latch is reset by the low voltage on the Soft-Ref pin. The reset fault latch resets the delay latch and Soft-Ref charges via the 0.5mA current source.

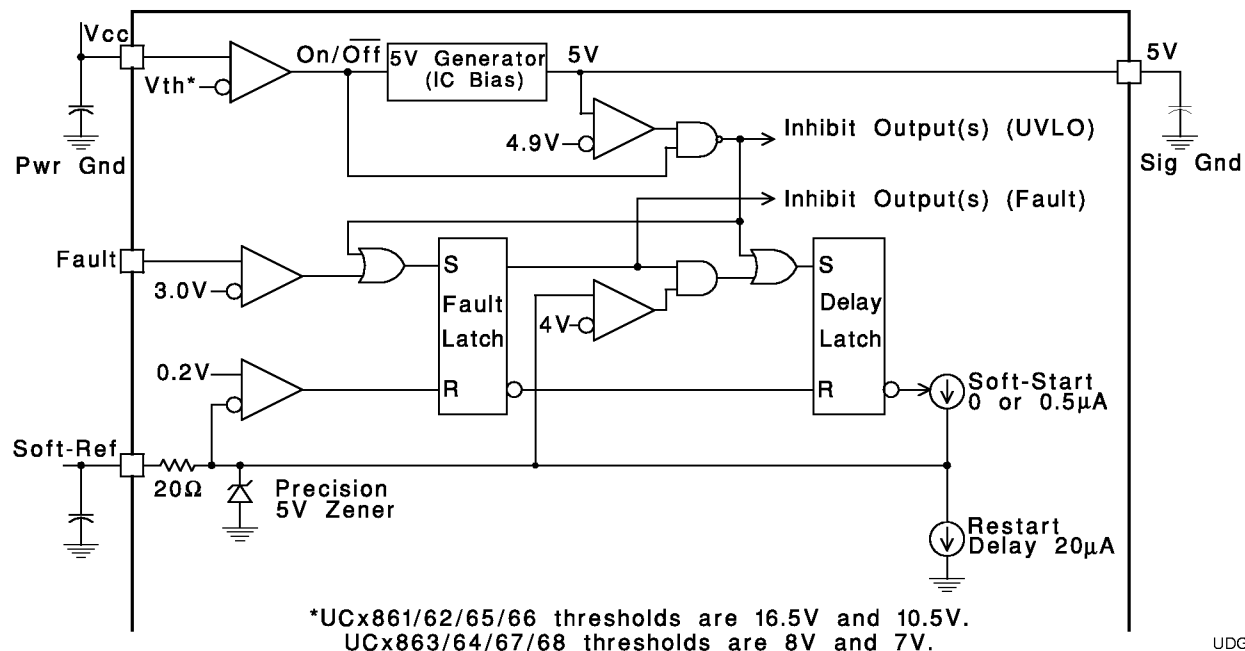
The fault pin is input to a high speed comparator with a threshold of 3V. In the event of a detected fault, the fault latch is set and the outputs are driven low. If Soft-Ref is above 4V, the delay latch is set. Restart delay is timed as Soft-Ref is discharged by 20 μA . When Soft-Ref is fully discharged, the fault latch is reset if the fault input signal is low. The Fault pin can be used as a system shutdown pin.

If a fault is detected during soft-start, the fault latch is set and the outputs are driven low. The delay latch will remain reset until Soft-Ref charges to 4V. This sets the delay latch, and restart delay is timed. Note that restart delay for a single fault event is longer than for recurring faults since Soft-Ref must be discharged from 5V instead of 4V.

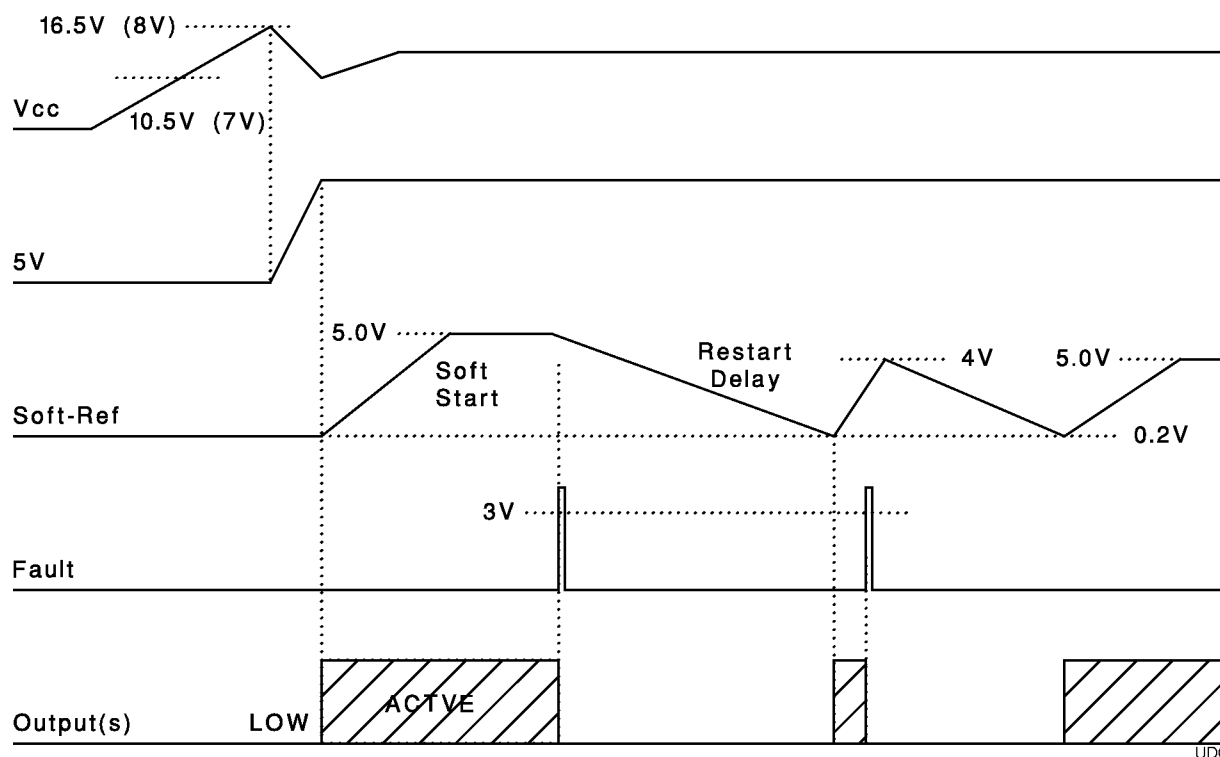
The restart delay to soft-start time ratio is 24:1 for a fault occurring during normal operation and 19:1 for faults occurring during soft-start. Shorter ratios can be programmed down to a limit of approximately 3:1 by the addition of a 20k Ω or larger resistor from Soft-Ref to ground.

A 100k Ω resistor from Soft-Ref to 5V will have the effect of permanent shut down after a fault since the internal 20 μA current source can't pull Soft-Ref low. This feature can be used to require recycling V_{CC} after a fault. Care must be taken to insure Soft-Ref is indeed low at start up, or the fault latch will never be reset.

APPLICATION INFORMATION

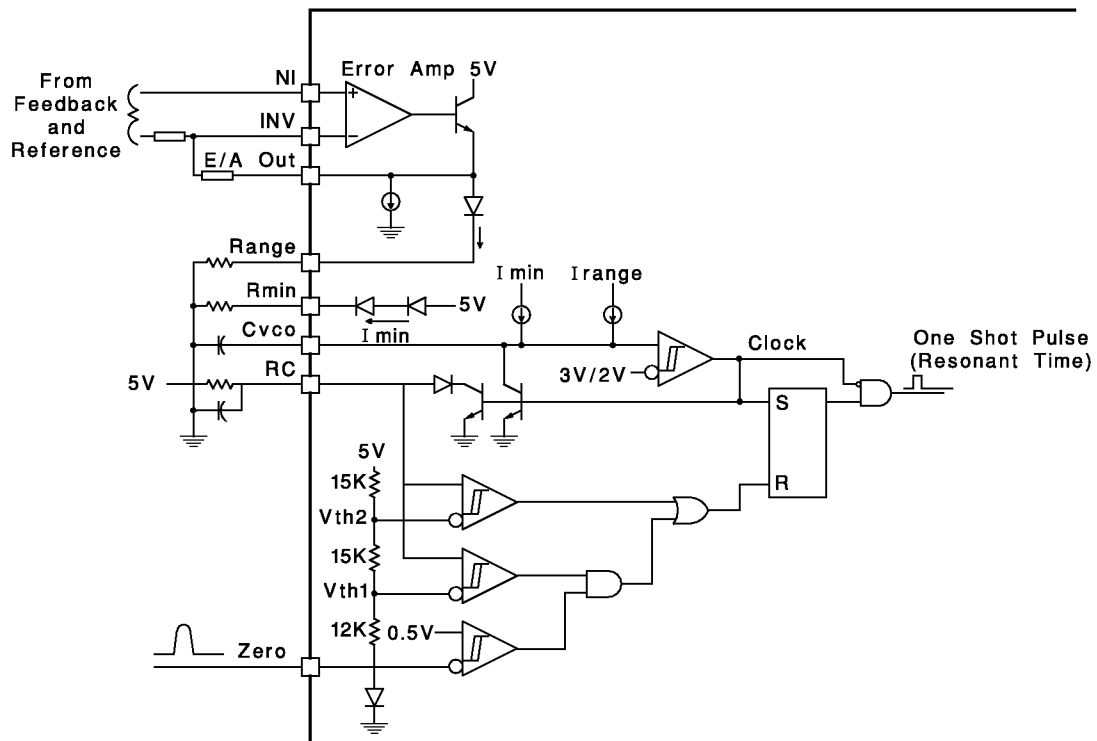


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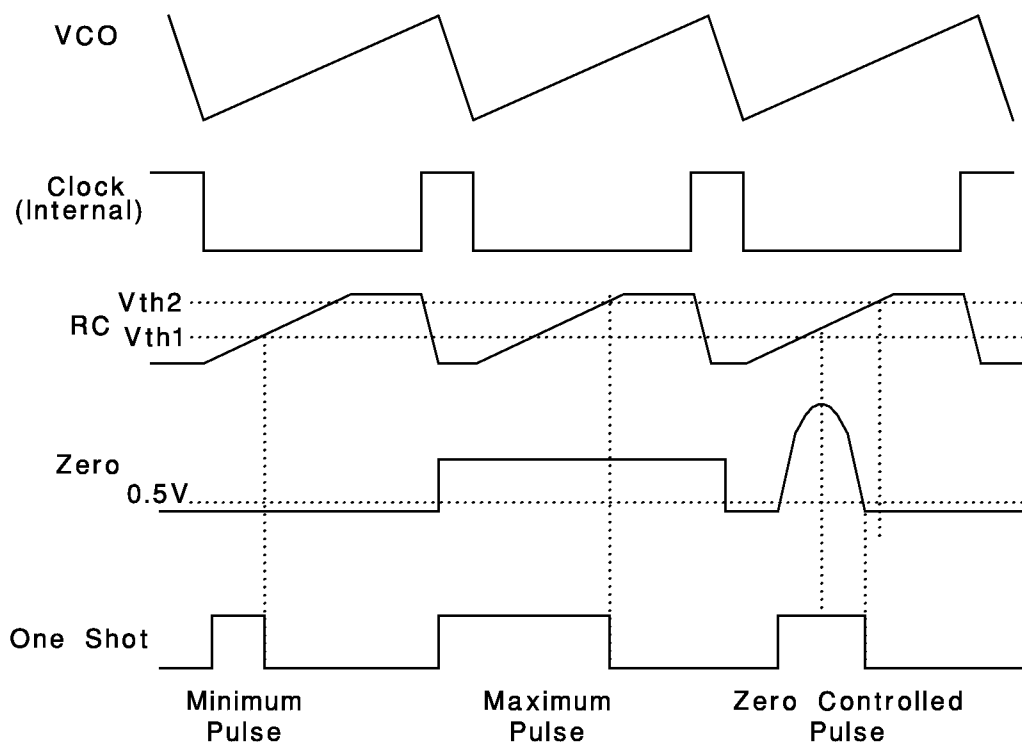


UDG-92021-1

Figure 1. UVLO, 5V, fault and soft-ref.



UDG-92022-1



UDG-92023-1

Figure 2. Error Amp, Voltage Controlled Oscillator, and One Shot

APPLICATION INFORMATION

Minimum oscillator frequency is set by R_{min} and C_{vco} . The minimum frequency is approximately given by the equation:

$$F_{MIN} \cong \frac{4.3}{R_{MIN} \cdot C_{VCO}}$$

Maximum oscillator frequency is set by R_{min} , Range & C_{vco} . The maximum frequency is approximately given by the equation:

$$F_{MAX} \cong \frac{3.3}{(R_{MIN} // Range) \cdot C_{VCO}}$$

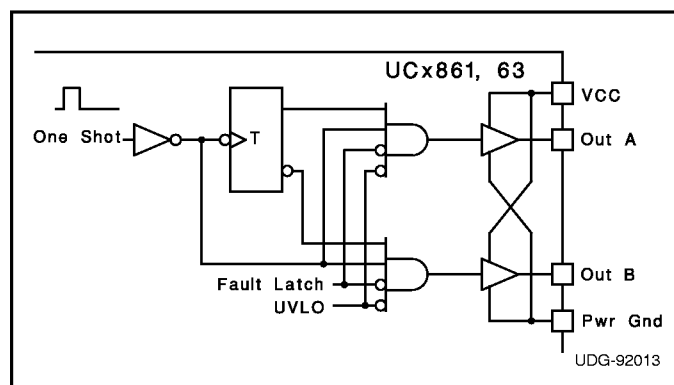
The Error Amplifier directly controls the oscillator frequency. E/A output low corresponds to minimum frequency and output high corresponds to maximum frequency. At the end of each oscillator cycle, the RC pin is discharged to one diode drop above ground. At the beginning of the oscillator cycle, $V(RC)$ is less than V_{th1} and so the output of the zero detect comparator is ignored. After $V(RC)$ exceeds V_{th1} , the one shot pulse will be terminated as soon as the zero pin falls below 0.5V or $V(RC)$ exceeds V_{th2} . The minimum one shot pulse width is approximately given by the equation:

$$Tp_{w(min)} = 0.3 R C.$$

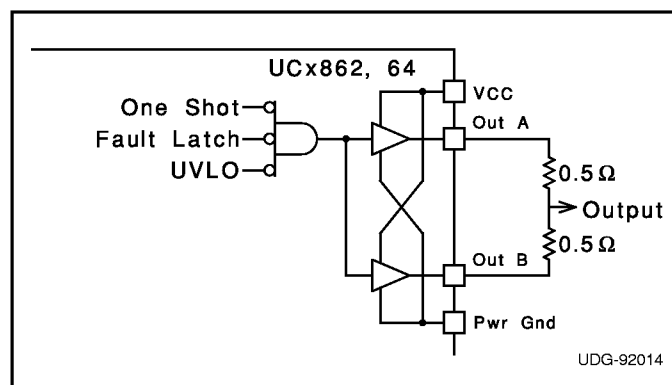
The maximum pulse width is approximately given by:

$$Tp_{w(max)} = 1.2 R C.$$

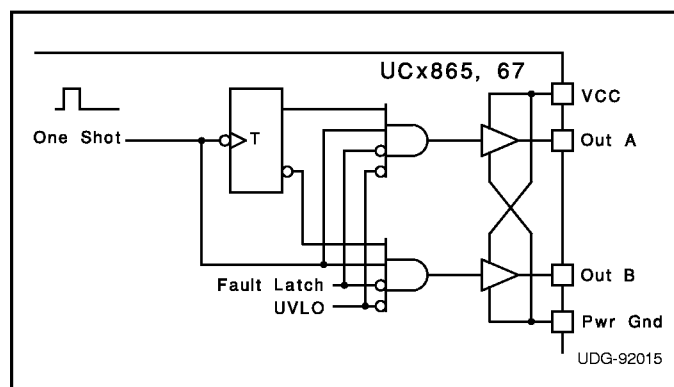
STEERING LOGIC



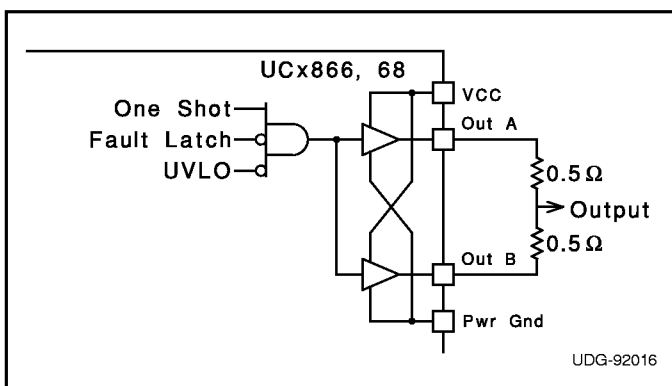
The steering logic is configured on the UC1861,63 to result in dual non-overlapping square waves at outputs A & B. This is suited to drive dual switch ZVS systems.



The steering logic is configured on the UC1862,64 to result in inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZVS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.



The steering logic is configured on the UC1865,67 to result in alternating pulse trains at outputs A & B. This is suited to drive dual switch ZCS systems.



The steering logic is configured on the UC1866,68 to result in non-inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZCS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.

APPLICATION INFORMATION (cont.)

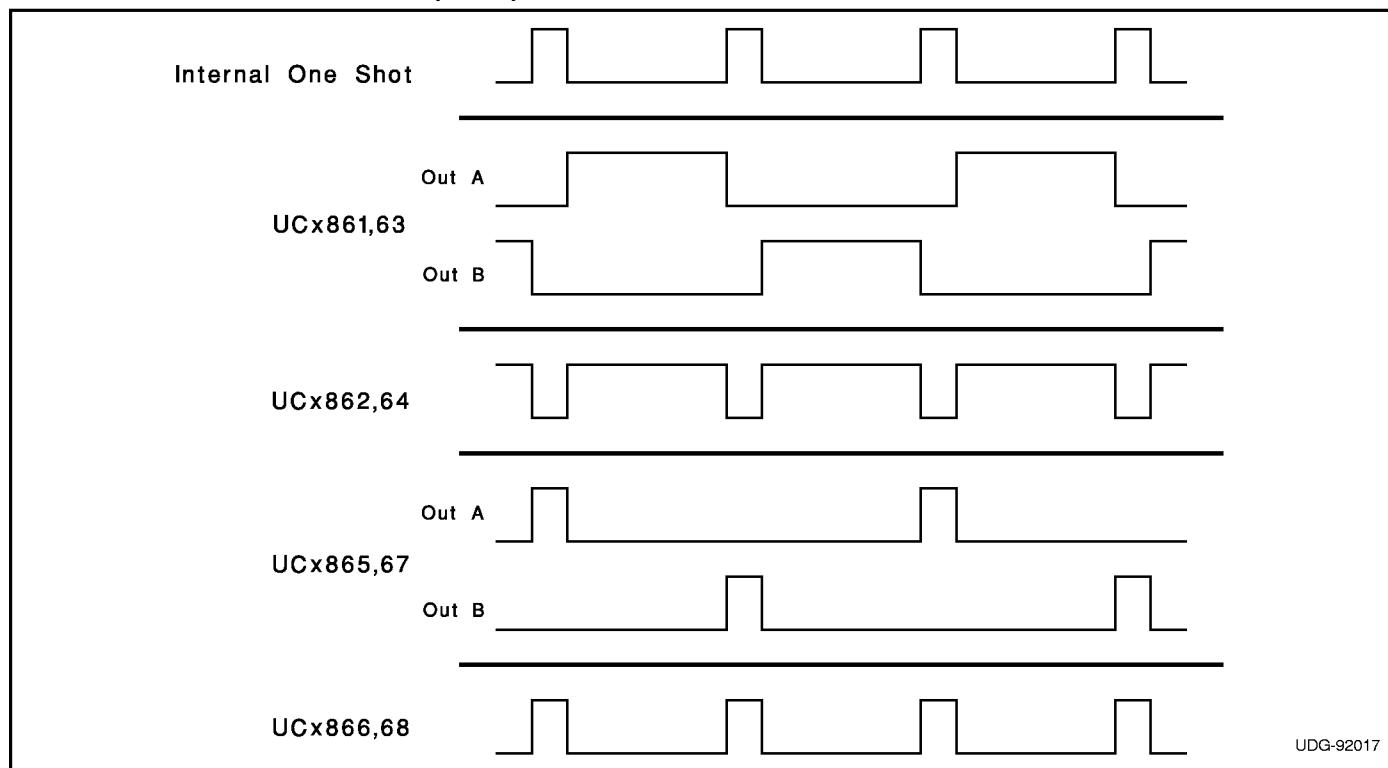


Figure 3. Current waveforms.

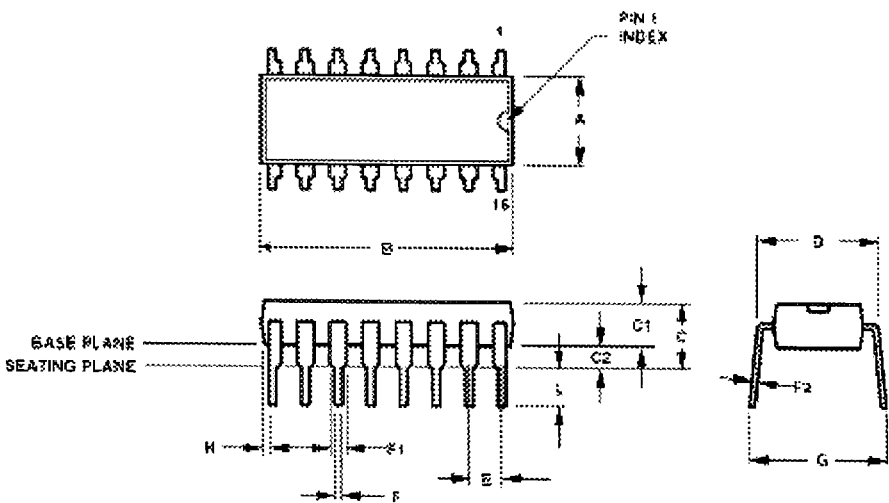


Mechanical Drawings

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16-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.745	.775	18.92	19.68	1
C	-	.210	-	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	-	0.13	-	
L	.115	.160	2.92	4.06	



NOTES:

1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ± 0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

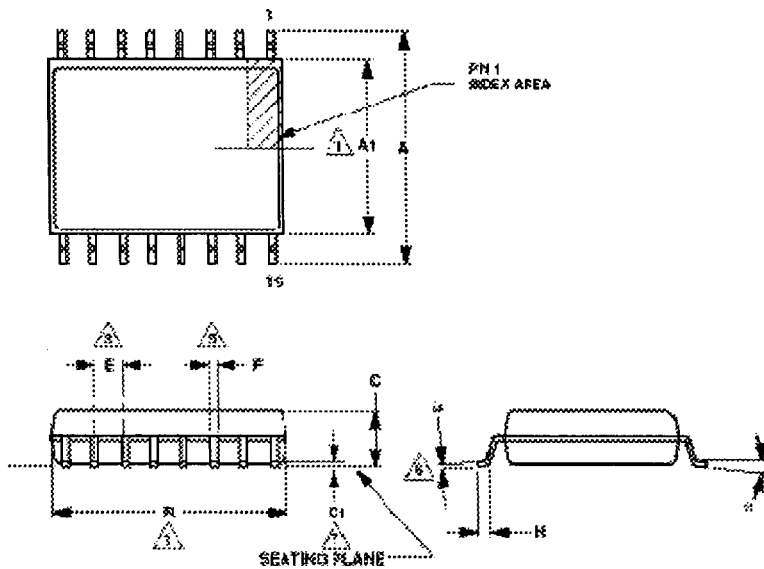


Mechanical Drawings

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16-PIN SOIC SURFACE MOUNT~ DW PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.403	.413	10.24	10.49
C	.097	.104	2.48	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
Ø	0°	8°	0°	8°



NOTES:

- 1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
- 2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
- 3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
- 4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
- 5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- 6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
- 7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

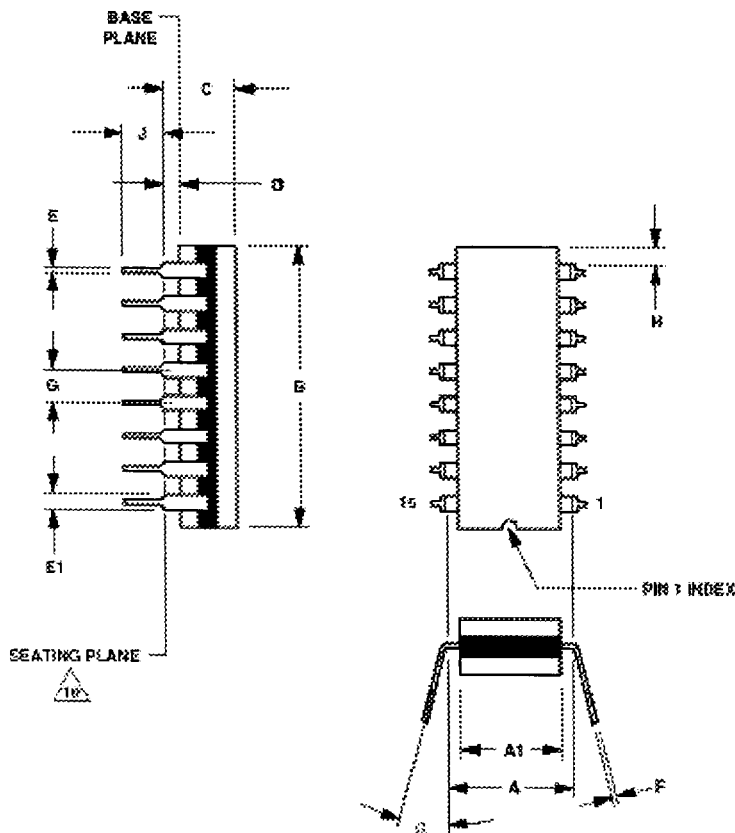


Mechanical Drawings

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16-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	-	0.840	-	21.34	4
C	-	0.200	-	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	-	0.13	-	6
J	0.125	0.200	3.18	5.08	
K	0°	15°	0°	15°	



NOTES:

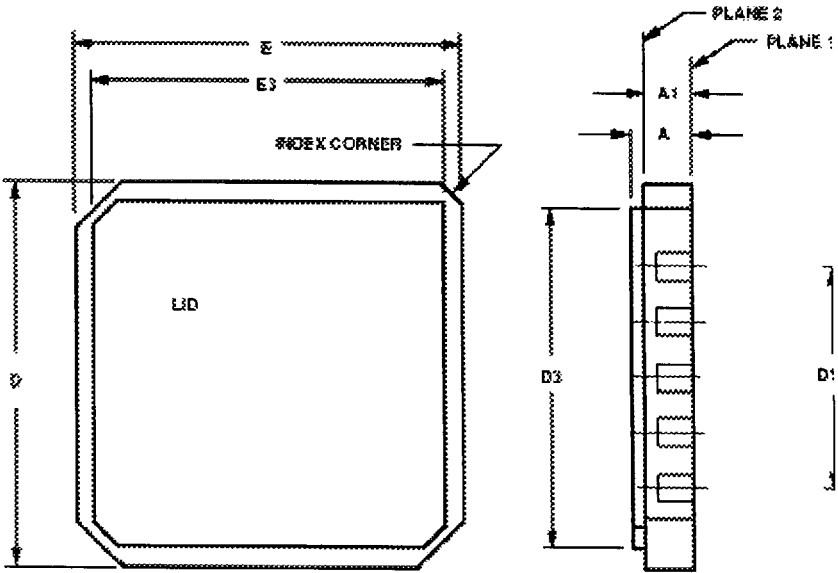
1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'E1' MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 8, 9 AND 16 ONLY.
3. DIMENSION 'D' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ± 0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 8, 9 AND 16).
7. DIMENSION 'A' SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0^\circ$.
8. THE MAXIMUM LIMITS OF DIMENSIONS 'E' AND 'F' SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.



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20-PIN CERAMIC LEADLESS SURFACE MOUNT ~ L PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.060	.100	1.52	2.54	6
A1	.050	.088	1.27	2.24	
B1	.022	.028	0.56	0.71	1,3
B2	.072 REF.		1.83 REF.		
B3	.006	.022	0.15	0.56	8
D/E	.342	.358	8.69	9.09	
D1/E1	.200 BSC		5.08 BSC		
D2/E2	.100 BSC		2.54 BSC		
D3/E3	-	.358	-	9.09	4
L	.045	.055	1.14	1.40	
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.90	2.41	5
L3	.003	.015	0.08	0.38	
N	20		20		2
ND/NE	5		5		2
e	.050 BSC		1.27 BSC		10



NOTES:

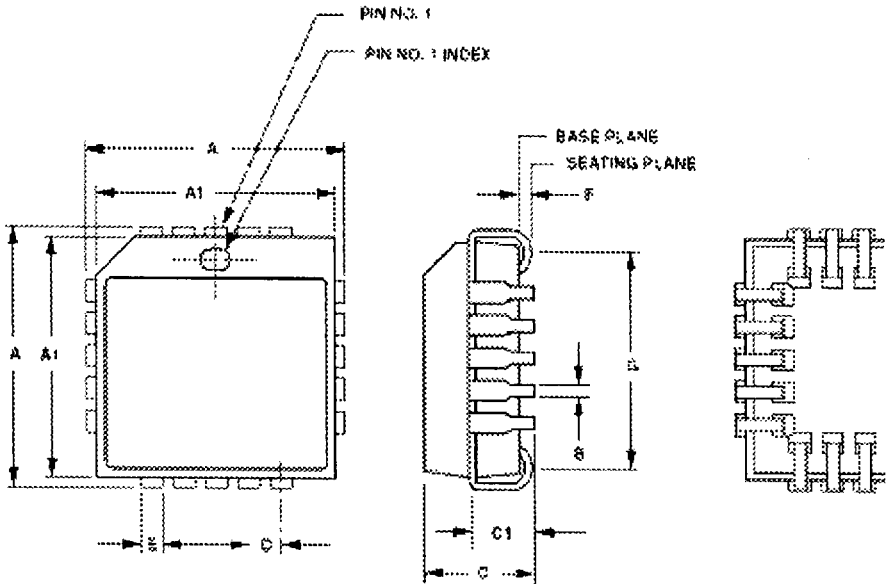
1. A MINIMUM CLEARANCE OF 0.015 IN. (0.38mm) SHALL BE MAINTAINED BETWEEN ADJACENT TE
2. 'N' IS THE MAXIMUM QUANTITY OF TERMINAL POSITIONS. 'ND' AND 'NE' ARE THE NUMBERS OF AND 'E' RESPECTIVELY.
3. ELECTRICAL CONNECTION TERMINALS ARE REQUIRED ON PLANE 1 AND OPTIONAL ON PLANE THEY SHALL BE ELECTRICALLY CONNECTED TO OPPOSING TERMINALS ON PLANE 1.
4. A MINIMUM CLEARANCE OR 0.015 IN. (0.38mm) SHALL BE MAINTAINED BETWEEN A METAL LID TERMINALS, METALLIZED CASTELLATIONS, ETC.) THE LID SHALL NOT EXTEND BEYOND THE E
5. THE INDEX FEATURE FOR NUMBER 1 TERMINAL IDENTIFICATION, OPTIONAL ORIENTATION OR AREA DEFINED BY DIMENSIONS 'B2' AND 'L2' ON PLANE 1.
6. DIMENSION 'A' CONTROLS THE OVERALL PACKAGE THICKNESS.
7. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
8. CASTELLATIONS ARE REQUIRED ON BOTTOM TWO LAYERS. CASTELLATIONS IN THE TOP LAYE
9. WHEN SOLDER DIP LEAD FINISH APPLIES, SOLDER BUMP HEIGHT SHALL NOT EXCEED 0.007 INC NOT EXCEED 0.006 INCHES.
10. THE BASIC TERMINAL SPACING IS 0.050 INCHES BETWEEN CENTERLINES. EACH TERMINAL CEN INCHES OF ITS EXACT TRUE POSITION.



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20-PIN PLASTIC PLCC SURFACE MOUNT~ Q PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.385	.395	9.78	10.03	
A1	.350	.356	8.89	9.04	1
B	.013	.021	0.33	0.53	
C	.170	.180	4.32	4.57	
C1	.100	.110	2.54	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	-	0.51	-	3, 4
G	.290	.330	7.37	8.38	



NOTES:

- 1. 'A1' DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
- 2. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL LOCATED WITHIN ± 0.004 IN. OF ITS EXACT TRUE POSITION.
- 3. 'F' IS MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
- 4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
- 5. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.