HD61200
(LCD Driver with 80-Channel Outputs)

Description

The HD61200 is a column driver LSI for a large-area dot matrix LCD. It employs 1/32 or more duty cycle multiplexing method. It receives serial display data from a micro controller or a display control LSI, HD61830, etc., and generates liquid crystal driving signals.

Ordering Information

Type No.	Package
HD61200	100-pin plastic QFP(FP-100)

Features

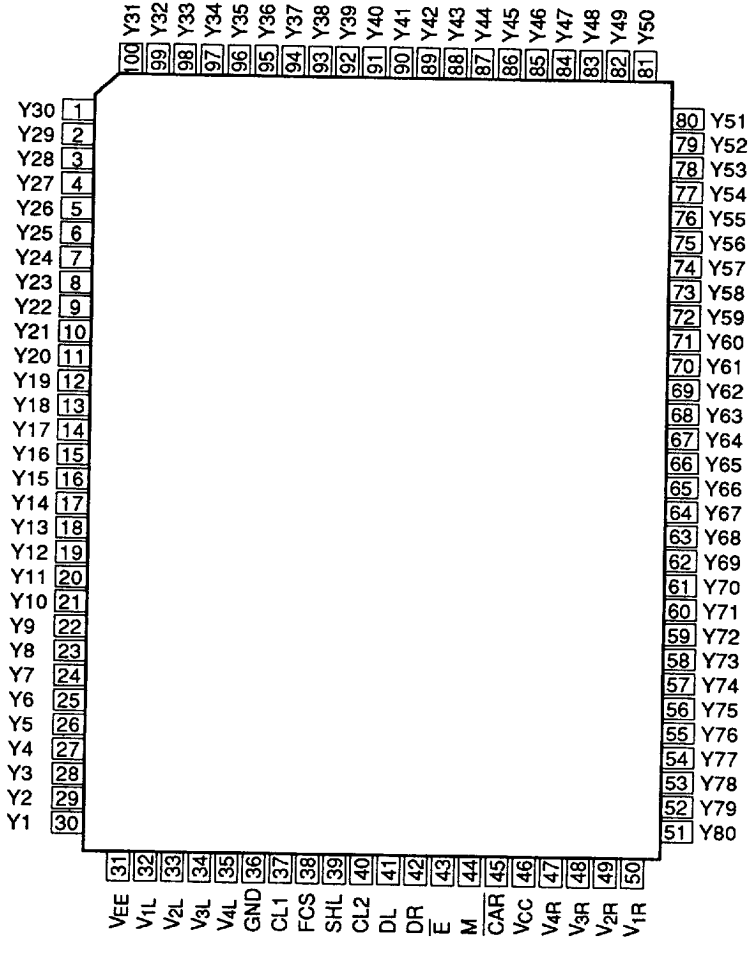
- Liquid crystal display driver with serial/parallel conversion function
- Internal liquid crystal display driver: 80 drivers
- Drives liquid crystal panels with 1/32-1/128 duty cycle multiplexing
- Can interface to LCD controllers, HD61830 and HD61830B
- Data transfer rate: 2.5 MHz max
- Power supply: V_{CC}: 5 V ± 10% (Internal logic)
- Power supply voltage for liquid crystal display drive: 8 V to 17 V
- CMOS process

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	−0.3 to +7.0	V	2
Supply voltage (2)	V_{EE}	V_{CC} − 19.0 to V_{CC} + 0.3	V	
Terminal voltage (1)	V_{T1}	−0.3 to V_{CC} + 0.3	V	2, 3
Terminal voltage (2)	V_{T2}	V_{EE} − 0.3 to V_{CC} + 0.3	V	4
Operating temperature	Topr	−20 to +75	°C	
Storage temperature	Tstg	−55 to +125	°C	

Notes:
1. LSIs may be permanently destroyed if being used beyond the absolute maximum ratings. In ordinary operation, it is desirable to use them within the limits of electrical characteristics, because using them beyond these conditions may cause malfunction and poor reliability.
2. All voltage values are referenced to GND = 0 V.
3. Applies to input terminals, FCS, SHL, CL1, CL2, DL, DR, E, and M.
4. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R}. Must maintain $V_{CC} \geq V_{1L} = V_{1R} \geq V_{3L} = V_{3R} \geq V_{4L} = V_{4R} \geq V_{2L} = V_{2R} \geq V_{EE}$. Connect a protection resistor of 15 Ω ± 10% to each terminal in series.

Pin Arrangement



(Top View)

Electrical Characteristics

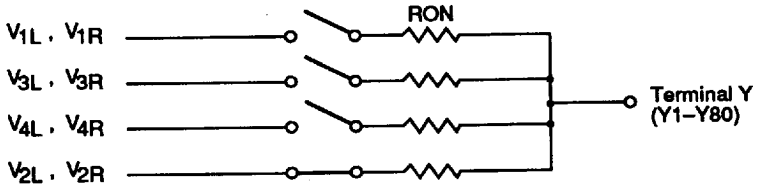
DC Characteristics

(V_{CC} = 5 V ± 10%, GND = 0 V, V_{CC} – VEE = 8 V to 17 V, Ta = –20 to 75°C)

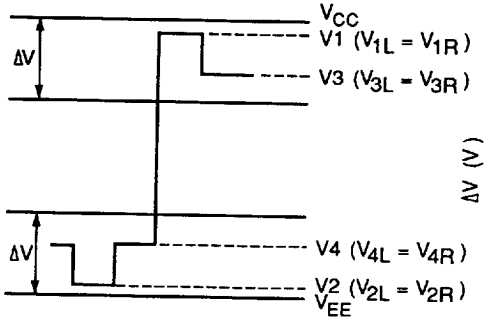
Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	0.7 × V_{CC}	—	V_{CC}	V		1
Input low voltage	V_{IL}	0	—	0.3 × V_{CC}	V		1
Output high voltage	V_{OH}	V_{CC} –0.4	—	—	V	I_{OH} = 400 µA	2
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 400 µA	2
Driver on resistance	R_{ON}	—	—	7.5	kΩ	Load current = 100 µA	5
Input leakage current	I_{IL1}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	1
Input leakage current	I_{IL2}	–2	—	2	µA	V_{IN} = V_{EE} to V_{CC}	3
Dissipation current (1)	I_{GND}	—	—	1.0	mA		4
Dissipation current (2)	I_{EE}	—	—	0.1	mA		4

Notes:
1. Applies to CL1, CL2, SHL, $\overline{E}$, M, DL, and DR.
2. Applies to $\overline{CAR}$.
3. Applies to V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R}.
4. Specified when display data is transferred under following conditions:
   CL2 frequency f_{CP2} = 2.5 MHz (data transfer rate)
   CL1 frequency f_{CP1} = 4.48 kHz (data latch frequency)
   M frequency f_M = 35 Hz (frame frequency/2)
   Specified at V_{IH} = V_{CC} (V), V_{IL} = 0 V and load on outputs.
   I_{GND}: currents between V_{CC} and GND.
   I_{EE}: currents between V_{CC} and V_{EE}.
5. Resistance between terminal Y and terminal V (one of V_{1L}, V_{1R}, V_{2L}, V_{2R}, V_{3L}, V_{3R}, V_{4L}, and V_{4R} when load current flows through one of the terminals Y1 to Y80. This value is specified under the following condition:

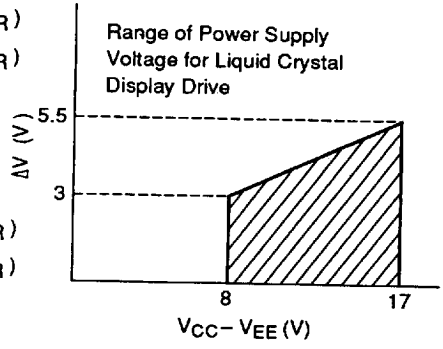
$$V_{CC} - V_{EE} = 17\ V$$
$$V_{1L} = V_{1R},\ V_{3L} = V_{3R} = V_{CC} - 2/7\ (V_{CC} - V_{EE})$$
$$V_{2L} = V_{2R},\ V_{4L} = V_{4R} = V_{EE} + 2/7\ (V_{CC} - V_{EE})$$



The following here is a description of the range of power supply voltage for liquid crystal display drivers. Apply positive voltage to $V_{1L} = V_{1R}$ and $V_{3L} = V_{3R}$ and negative voltage to $V_{2L} = V_{2R}$ and $V_{4L} = V_{4R}$ within the ΔV range. This range allows stable impedance on driver output (RON). Notice the ΔV depends on power supply voltage V_{CC}–V_{EE}.



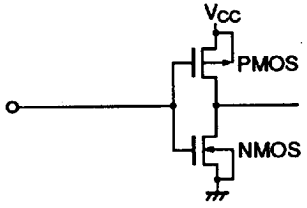
Correlation between Driver Output Waveform and Power Supply Voltages for Liquid Crystal Display Drive



Correlation between Power Supply Voltage V_{CC}– V_{EE} and ΔV

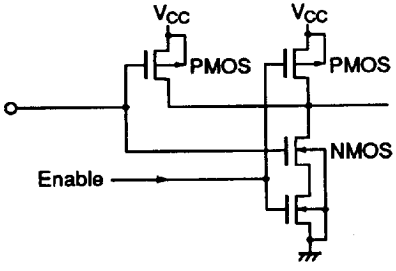
Terminal Configuration

Input Terminal

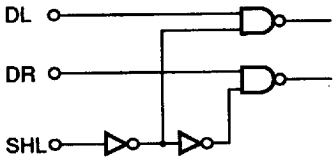


Applicable terminals :
CL1, CL2, SHL, $\overline{E}$, M

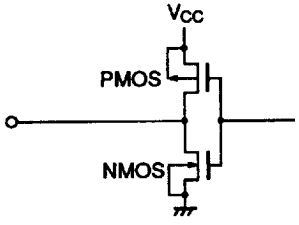
Input Terminal (with Enable)



Applicable terminals: DL, DR

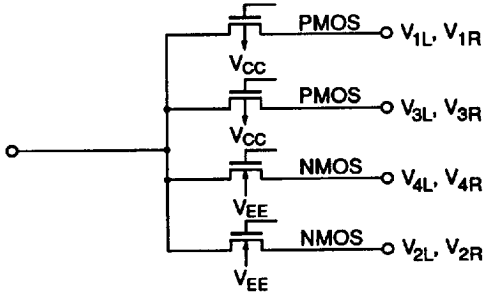


Output Terminal



Applicable terminal: $\overline{CAR}$

Output Terminal



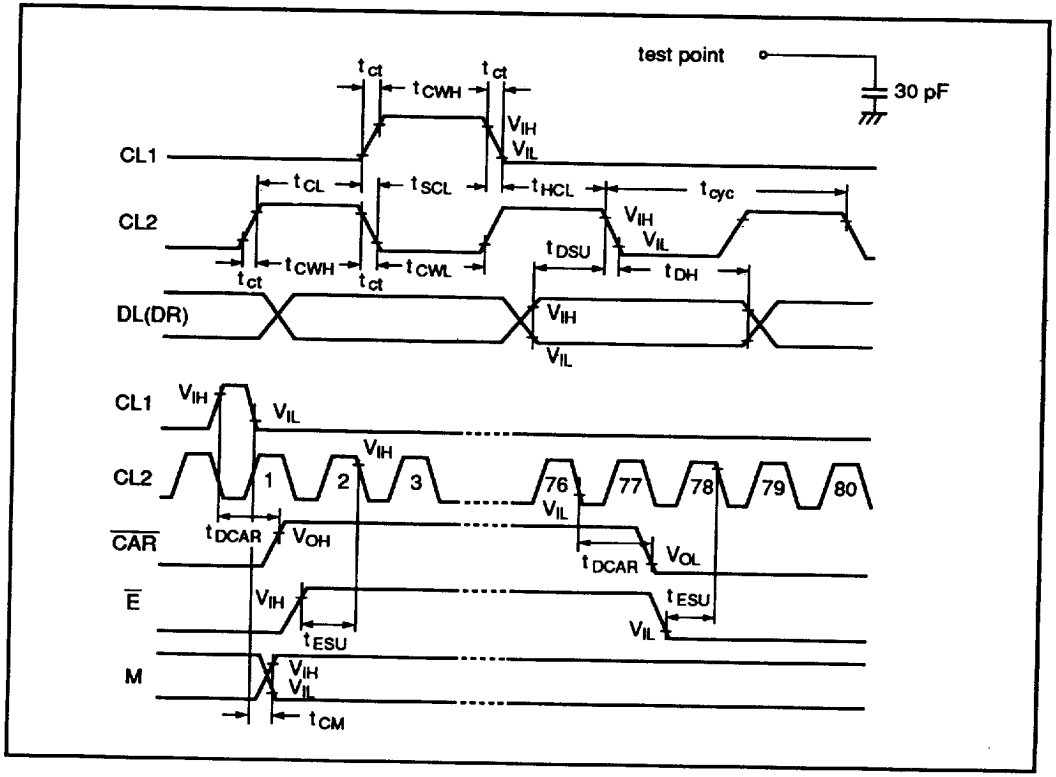
Applicable terminals:
Y1–Y80

AC Characteristics

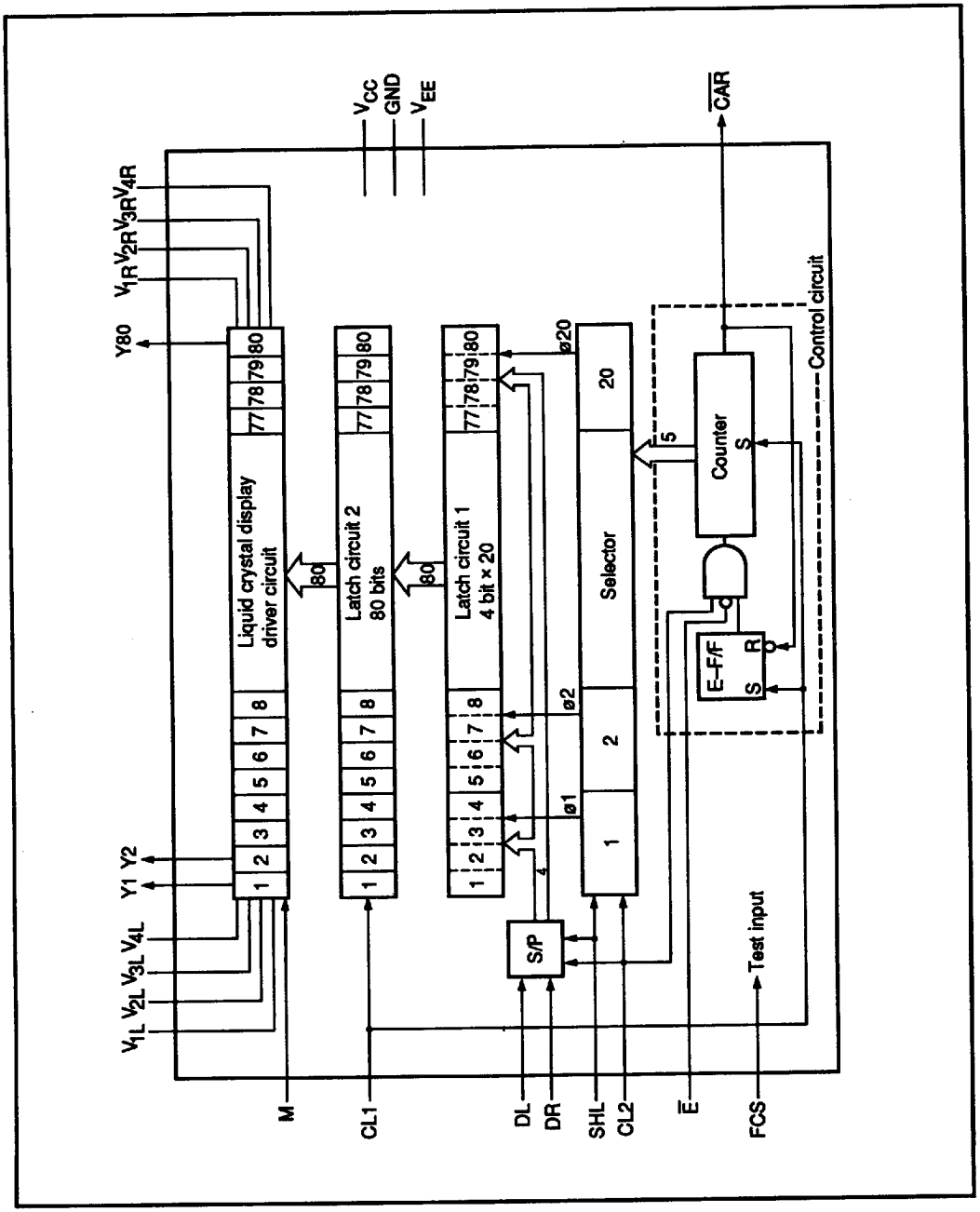
(V_{CC} = 5 V ± 10%, GND = 0 V, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Clock cycle time	t_{CYC}	400	—	—	ns		
Clock high level width	t_{CWH}	150	—	—	ns		
Clock low level width	t_{CWL}	150	—	—	ns		
Clock setup time	t_{SCL}	100	—	—	ns		
Clock hold time	t_{HCL}	100	—	—	ns		
Clock rise/fall time	t_{Ct}	—	—	30	ns		
Clock phase different time	t_{CL}	100	—	—	ns		
Data setup time	t_{DSU}	80	—	—	ns		
Data hold time	t_{DH}	100	—	—	ns		
E setup time	t_{ESU}	200	—	—	ns		
Output delay time	t_{DCAR}	—	—	300	ns		1
M phase difference time	t_{CM}	—	—	300	ns		

Note: 1. The following load circuit is connected for specification:



Block Diagram



Block Function

Liquid Crystal Display Driver Circuit

The combination of the data from the latch circuit 2 and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

80-bit Latch Circuit 2

The data from latch circuit 1 is latched at the fall of CL1 and output to liquid crystal display driver circuit.

S/P

Serial/parallel conversion circuit which converts 1-bit data into 4-bit data. When SHL is low level, data from DL is converted into 4-bit data and transferred to the latch circuit 1. In this case, don't connect any lines to terminal DR.

When SHL is high level, input data from terminal DR without connecting any lines to terminal DL.

80-bit Latch Circuit 1

The 4-bit data is latched at $\phi 1$—$\phi 20$ and output to latch circuit 2. When SHL is low level, the data from DL are latched in order of 1→2→3 ... →80 of each latch. When SHL is high level, they are latched in a reverse order (80→79→78 ... →1).

Selector

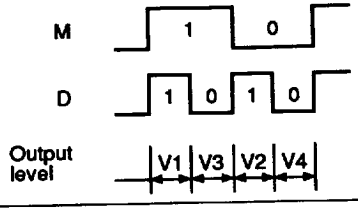
The selector decodes output signals from the counter and generates latch clock $\phi 1$ to $\phi 20$. When the LSI is not active, $\phi 1$–$\phi 20$ are not generated, so the data at latch circuit 1 is stored even if input data (DL, DR) changes.

Control Circuit

Controls operation: When E–F/F (enable F/F) indicates 1, S/P conversion is started by inputting low level to $\overline{E}$. After 80-bit data has been all converted, $\overline{CAR}$ output turns into low level and E–F/F is reset to 0, and consequently the conversion stops. E–F/F is RS flip-flop circuit which gives priority to SET over RESET and is set at high level of CL1.

The counter consists of 7 bits, and the output signals upper 5 bits are transferred to the selector. $\overline{CAR}$ signal turns into high level at the rise of CL1. The number of bits that can be S/P-converted can be increased by connecting $\overline{CAR}$ terminal with $\overline{E}$ terminal of the next HD61200.

Terminal Functions Description

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND V_{EE}	1 1 1		Power supply	V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for LCD drive circuit
V_{1L}–V_{4L} V_{1R}–V_{4R}	8		Power supply	Power supply for liquid crystal drive. V_{1L} (V_{1R}), V_{2L} (V_{2R}): Selection level V_{3L} (V_{3R}), V_{4L} (V_{4R}): Non-selection level Power supplies connected with V_{1L} and V_{1R} (V_{2L} & V_{2R}, V_{3L} & V_{3R}, V_{4L} & V_{4R}) should have the same voltages.
Y1-Y80	80	O	LCD	Liquid crystal driver outputs. Selects one of the 4 levels, V1, V2 V3, and V4. Relation among output level, M, and display data (D) is as follows: 
M	1	I	Controller	Switch signal to convert liquid crystal drive waveform into AC.
CL1	1	I	Controller	Synchronous signal (a counter is reset at high level). Latch clock of display data (falling edge triggered). Synchronized with the fall of CL1, liquid crystal driver signals corresponding to the display data are output.
CL2	1	I	Controller	Shift clock of display data (D). Falling edge triggered.
DL, DR	2	I	Controller	Input of serial display data (D). (D) / Liquid Crystal Driver Output / Liquid Crystal Display 1 (High level) / Selection level / On 0 (Low level) / Non-selection level / Off
SHL	1	I	V_{CC} or GND	Selects the shift direction of serial data. When the serial data (D) is input in order of D1→ ... →D80, the relations between the data (D) and output Y are as follows: SHL: Y1 / Y2 / Y3 / .... / Y80 Low: D1 / D2 / D3 / .... / D80 High: D80 / D79 / D78 / .... / D1

Terminal Functions Description (cont)

Terminal Name	Number of Terminals	I/O	Connected to	Functions
SHL (cont)	1	I	V_{CC} or GND	When SHL is low, data is input from the DL terminal. No lines should be connected to the DR terminal. When SHL is high, the relation between DL and DR reverses.
$\overline{E}$	1	I	GND or the terminal $\overline{CAR}$ of the HD61200	Controls the S/P conversion. The operation stops on high level, and the S/P conversion starts on low level.
$\overline{CAR}$	1	O	Input terminal $\overline{E}$ of the HD61200	Used for cascade connection with the HD61200 to increase the number of bits that can be S/P converted.
FCS	1	I	GND	Input terminal for test. Connect to GND.

Operation of the HD61200

The following describes an LCD panel with 64 × 240 dots on which characters are displayed with 1/64 duty cycle dynamic drive. Figure 1 is an example of liquid crystal display and connection to HD61200s. Figure 2 is a time chart of HD61200 I/O signals.

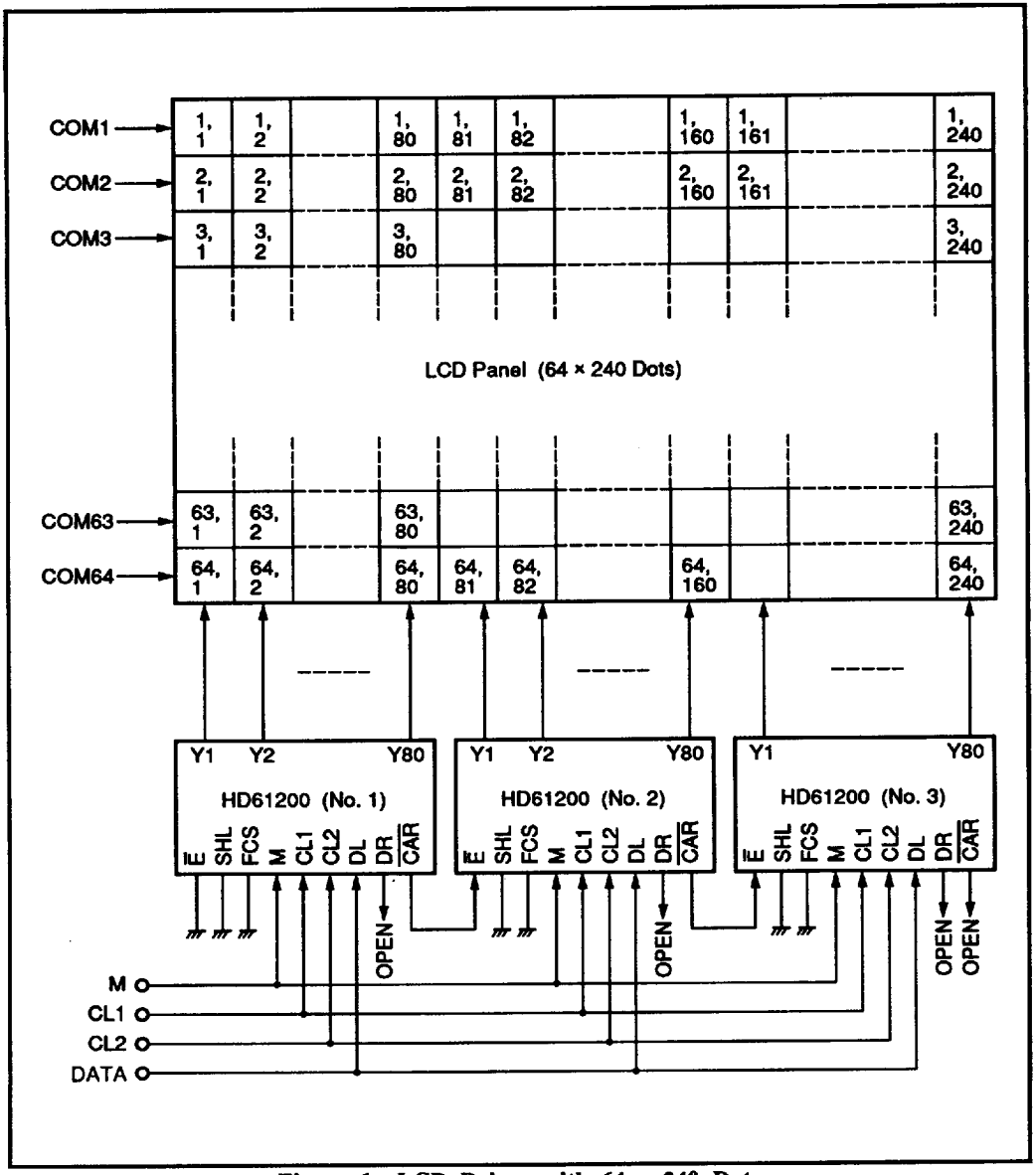


Figure 1 LCD Driver with 64 × 240 Dots

Cascade three HD61200s. Input data to the DL terminal of No. 1, No. 2, and No. 3. Connect $\overline{E}$ of No. 1 to GND. Don't connect any lines to $\overline{CAR}$ of No. 3. Connect common signal terminals (COM1–COM64) to X1–X64 of common driver HD61203. (m, n) of LCD panel is the address corresponding to each dot.

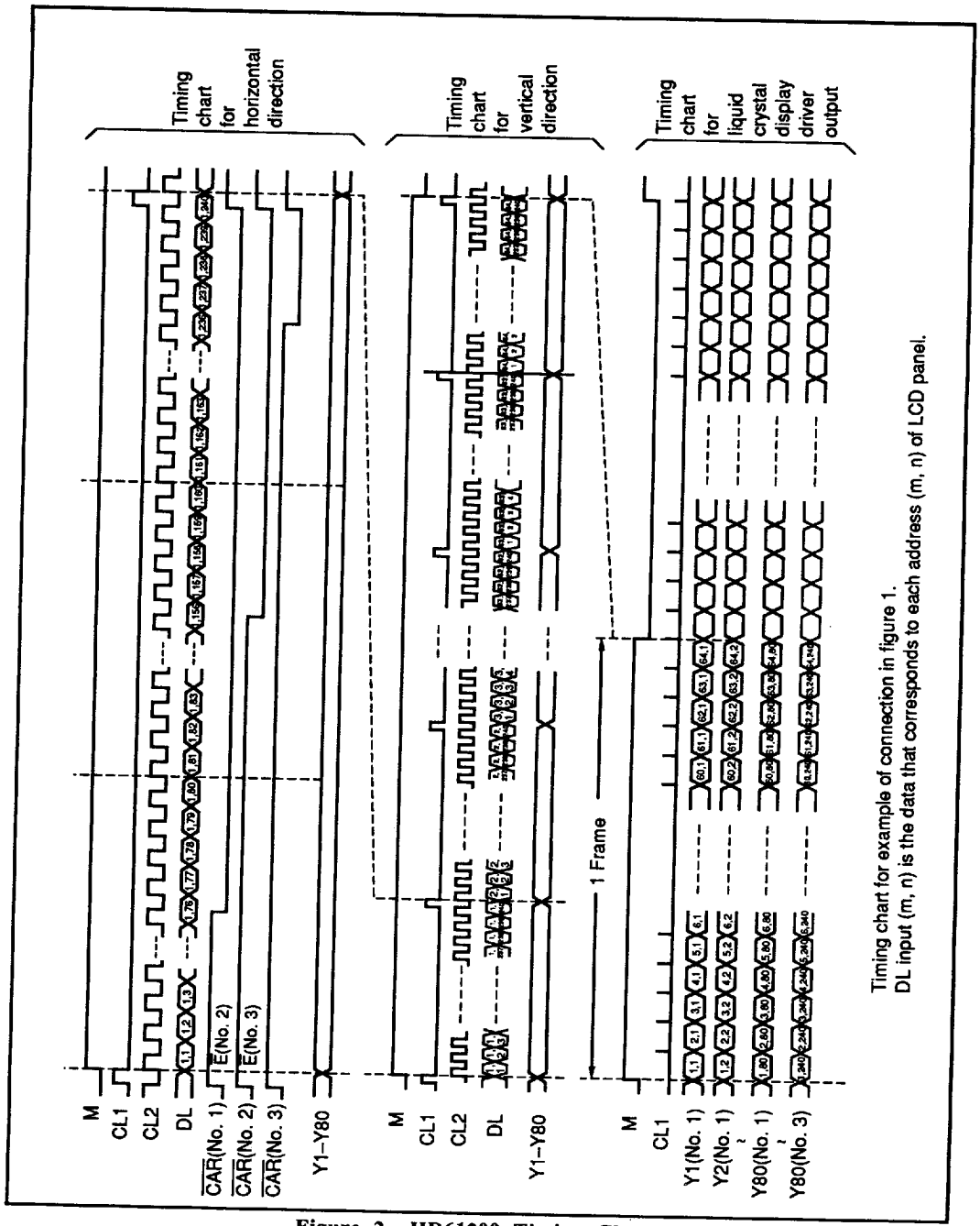


Figure 2 HD61200 Timing Chart

Application Example

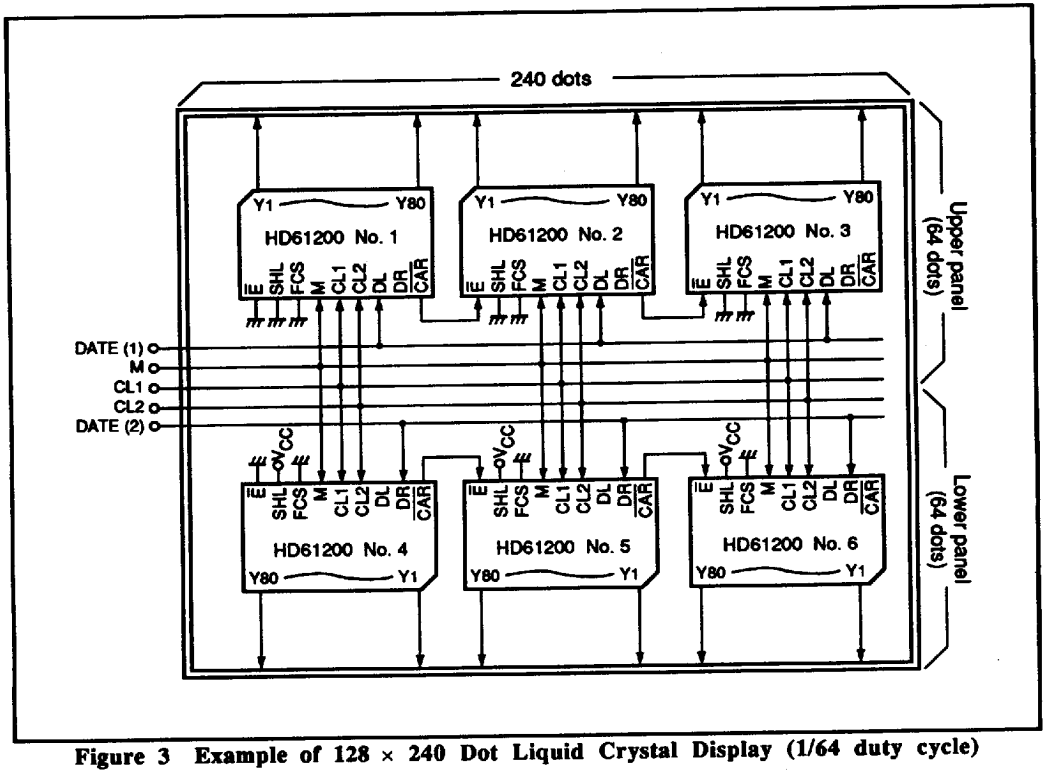


Figure 3 Example of 128 × 240 Dot Liquid Crystal Display (1/64 duty cycle)

The liquid crystal panel is divided into upper and lower parts. These two parts are driven separately. HD61200s No. 1 to No. 3 drive the upper half. Serial data, which are input from the DATA (1) terminal, appear at $Y_1 \rightarrow Y_2 \rightarrow \text{-- } Y_{80}$ terminal of No. 1, then at $Y_1 \rightarrow Y_2 \rightarrow \text{-- } Y_{80}$ of No. 2 and then at $Y_1 \rightarrow Y_2 \rightarrow \text{-- } Y_{80}$ of No. 3 in the order in which they were input (in the case of SHL = low). HD61200s No. 4 to No. 6 drive the lower half. Serial data, which are input from DATA (2) terminal, appear at $Y_{80} \rightarrow Y_{79} \rightarrow \text{-- } Y_1$ of No. 4, then at $Y_{80} \rightarrow Y_{79} \rightarrow \text{-- } Y_1$ of No. 5 and then $Y_{80} \rightarrow Y_{79} \rightarrow \text{-- } Y_1$ of No. 6 in the order in which they were input (in the case of SHL = high).

As shown in this example, a PC board for a display divided into upper and lower half can be easily designed by using the SHL terminal effectively.