

Advance Information Remote Control Encoder/ Decoder CMOS

The MC145030 encodes and decodes nine bits of information, which allows 512 different codes.

The encoder section samples the 9-bit parallel address input, encodes the bits into Manchester Code, and sends the serial information via the ENC_{out} pin. The address is issued twice per encoding sequence; initialization occurs with a rising edge on ENC ENB.

The decoder accepts serial information at the DEC_{in} pin, and decodes the Manchester information. The decoded address is compared with the local address. If a match occurs, DEC_{out} toggles once per sequence. The active-high DRST input is used to clear DEC_{out} .

The Status pin, when high, indicates the device is encoding. During decoding or standby, Status is low.

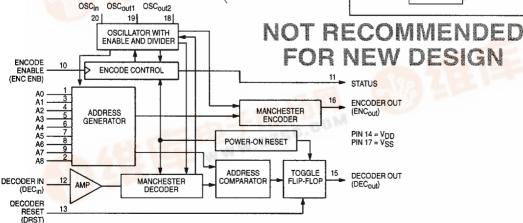
Applications:

Cordless Phones and Half-Duplex Remote Control

Interfaces with RF, Ultrasonic, or Infrared Modulators and Demodulators

- Operating Temperature Range: 40 to 85°C
- Operating Voltage Range: 2 to 6 V
- Standby Supply Current: 20 μA Maximum @ 2.0 V
- Operating Supply Current: 700 μA Maximum @ 2.5 V
- Address Inputs Have On-Chip Pull-Up Devices
- RC Oscillator, No Crystal Required
- On-Chip Amplifier in Decode Section
- Power-On Reset Forces DEC_{out} Low and Initializes the Decoder and Encoder Sections
- See Application Notes AN1016 and AN1126 and Article Reprint AR255

BLOCK DIAGRAM



The document contains information on a new product Specifications and information herein are subject to change without notice.

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	P SUFFIX PLASTIC DIP CASE 738
C CREATER OF	DW SUFFIX SOG CASE 751D
ORDERING IN	FORMATION
MC145030P	Plastic DIP
MC145030DW	SOG Package

PIN ASSIGMENT					
A0 [1•	20	osc _m		
A8 [2	19] OSC _{out1}] OSC _{out2}		
A1 [3	18	OSCout2		
A2 [4	17) v _{ss}		
A3 [5	16] ENCout		
A4 [6	15	DECout		
A5 [7	14	D v _{od}		
A6 [8	13	DIDRST		
A7 [9	12			
ENC ENB	10	11) STATUS		

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MAXIMUM RATINGS* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
VDD	DC Supply Voltage	- 0.5 to + 7.0	V
Vin	DC Input Voltage	- 0.5 to V _{DD} + 0.5	V
Vout	DC Output Voltage	- 0.5 to V _{DD} + 0.5	V
lin	DC Input Current, per Pin	± 10	mA
lout	DC Output Current, per Pin	± 10	mA
IDD	DC Supply Current, VDD and VSS Pins	± 30	mA
PD	Power Dissipation, per Package†	500	mW
Tstg	Storage Temperature	- 65 to + 150	°C
т	Lead Temperature (10-Second Soldering)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range VSS \leq (Vin or Vout) \leq VDD.

Except for the Address Inputs, unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). The Address inputs may be left open; see Pin Descriptions. Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

† Power Dissipation Temperature Derating: - 12 mW/°C from 65 to 85°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V _{DD} V	Guaranteed Limit	Unit
VDD	Power Supply Voltage Range		—	2.0 to 6.0	v
VIL	Maximum Low-Level Input Voltage (Except DECin)		2.5 6.0	0.3 1.2	v
۷н	Minimum High-Level Input Voltage (Except DECin)		2.5 6.0	1.9 4.5	v
V _{sig}	Minimum Output Voltage of Signal Source Driving DECin	Square-Wave Source See Figure 1	2.5 6.0	200 200	m∨ _{p-p}
VOL	VOL Maximum Low-Level Output Voltage	$I_{out} = 0 \ \mu A$ $I_{out} = 0.4 \ mA$	2.5	0.15 0.4	V
		$I_{out} = 0 \ \mu A$ $I_{out} = 1.0 \ mA$	6.0	0.15 0.4	
VOH	Minimum High-Level Output Voltage	$I_{out} = 0 \ \mu A$ $I_{out} = -0.4 \ mA$	2.5	2.35 2.0	v
	$I_{out} = 0 \ \mu A$ $I_{out} = -1.0 \ m A$	6.0	5.85 5.5		
lin	Maximum Input Current DEC _{in} ENC ENB, DRST, OSC _{in}	V _{in} = V _{DD} or V _{SS}	6.0	±60 ±0.3	μA
ŀН	Maximum High-Level Input Leakage Current A0-A8	V _{in} = V _{DD}	6.0	0.3	μΑ
μL	Maximum Low-Level Pull-Up Current A0-A8	V _{In} = V _{SS}	6.0	- 100	μA
loz	Maximum Three-State Leakage Current ENCout	V _{out} = V _{DD} or V _{SS}	6.0	± 500	nA
DD	Maximum Quiescent Supply Current	Device in Standby Mode V _{in} = V _{SS} or V _{DD} for ENC ENB, DEC _{in} , DRST, OSC _{in} V _{in} = V _{SS} , V _{DD} , or Open for A0–A8 I _{out} = 0 µA	2.0 6.0	20 100	μA
lqq	Maximum RMS Operating Supply Current	Oscillator Frequency = 500 kHz Vin = VSS or VDD for ENC ENB, DECin, DRST, OSCin Vin = VSS, VDD, or Open for A0-A8 Iout = 0 µA	2.5 6.0	700 2500	μA

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AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, C_L = 50 pF, V_{DD} = 2.5 to 6 V unless otherwise stated)

Symbol	Parameter	Figure #	V _{DD} V	Guaranteed Limit	Unit
fosc	Maximum Oscillator Frequency (~ 50% Duty Cycle)*	2	—	500	kHz
^t PLH, ^t PHL	System Propagation Delay, ENC ENB (of an encoding device) to DEC _{OUt} (of a decoding device)	3, 5	_	384-608	OSC Cycles
ťа	Debounce Time, ENC ENB (guarantees 1 encoding sequence)		—	608	OSC Cycles
tw	Minimum Input Pulse Width, ENC ENB or DRST	4	2.5 6.0	200 80	ns
C _{in}	Maximum Input Capacitance		—	10	pF

*See Pin Descriptions and Application Example for component tolerances.

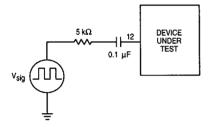
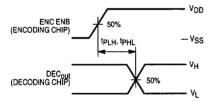
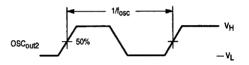


Figure 1. Decoder Input Sensitivity Test



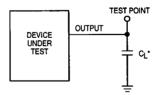












*Includes all probe and fixture capacitance.

Figure 5. Test Circuit

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PIN DESCRIPTIONS

INPUT PINS

A0--A8

Local Address Inputs (Pins 1, 3-9, 2)

These binary inputs provide the address for both the encoder and decoder; 512 addresses are possible. The local address is sent serially from ENC_{out} with 2 sync bits appearing first, followed by A0. The decoder compares the local address with the received address stream.

On-chip pullup devices are provided on the address inputs to facilitate interface to SPST switches or jumpers to VSS. During standby, A0–A8 are in the high-impedance state (i.e., the pull-up devices are inactive to minimize standby power consumption).

The inputs are left open (or tied to V_{DD}) for a high level and tied to V_{SS} for a low level.

ENC ENB

Edge-Sensitive Encode Enable (Pin 10)

A low-to-high transition on this pin aborts any decoding sequence in progress and initiates an encoding sequence. This input is debounced 608 oscillator cycles. See Figures 8 and 9.

DECin

Decoder In (Pin 12)

Decoder In is the input to the on-chip amplifier. The incoming signal is usually capacitively-coupled to this pin. Direct coupling may be used if the signal level is rail-to-rail (VSS to VDD).

DRST

Level-Sensitive Decoder Reset (Pin 13)

When this input is taken high, DEC_{out} is cleared to a low level. This pin may be used to override a response from a DEC_{in} data stream.

OUTPUT PINS

STATUS

Encode/Decode Status (Pin 11)

This pin is high during the encoding sequence and low during decoding or idle.

When Status is low, the ENCout pin is in the high-impedance state.

DECout

Toggle Flip-Flop Decoder Output (Pin 15)

The encoder sends the same address twice to complete a sequence. If one or both of the decoded addresses matches the local address, DEC_{OUI} toggles once per sequence (unless overridden by DRST). See Figures 6 and 7.

ENCout

Three-State Encoder Output (Pin 16)

This is the serial output of the Manchester-encoded local address. A0 appears before A8 in the bit stream. The local address is sent twice to complete a sequence which is initialized by ENC ENB. When a sequence is complete, ENC_{out} returns to the high-impedance state. See Figures 8 and 9.

OSCILLATOR PINS

OSCin, OSCout1, OSCout2

Oscillator Input, Oscillator Outputs 1/2 (Pins 20, 19, 18)

As shown in Figure 10, these pins are used in conjunction with external resistors and a capacitor to form an oscillator. Polystyrene or mylar capacitors are recommended. Susceptibility to externally induced noise signals may occur if resistors utilized are greater than 1 M Ω . See Figure 10 for component tolerances.

When the on-chip oscillator is used, the frequency may be up to 500 kHz. The oscillator is active only during encoding or decoding.

When an external frequency source is used to drive OSC_{in} , OSC_{out1} and OSC_{out2} may be left floating. The signal applied to OSC_{in} should swing rail-to-rail and may be dc to 500 kHz.

POWER SUPPLY PINS

Vss

Negative Power Supply (Pin 17)

This pin is the negative supply potential and is usually ground.

VDD

Positive Power Supply (Pin 14)

This pin is the positive supply potential and may range from + 2 to + 6 V with respect to V_{SS}.

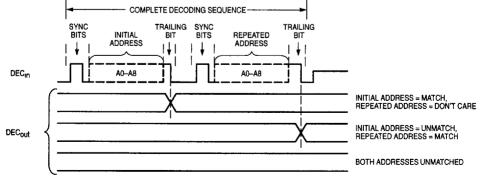
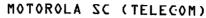
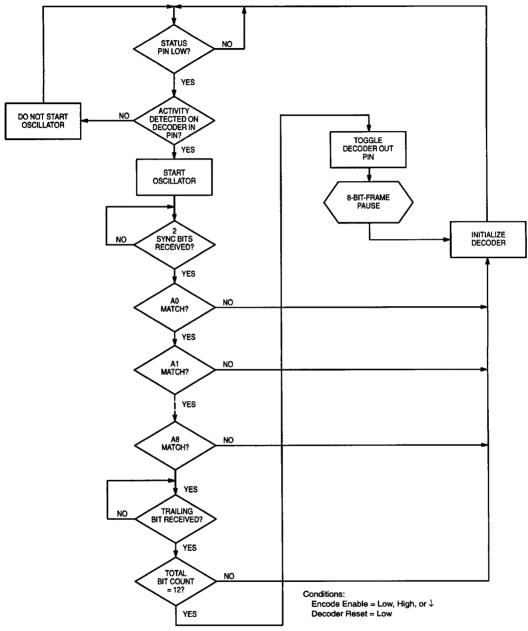


Figure 6. Decoder Timing Diagram







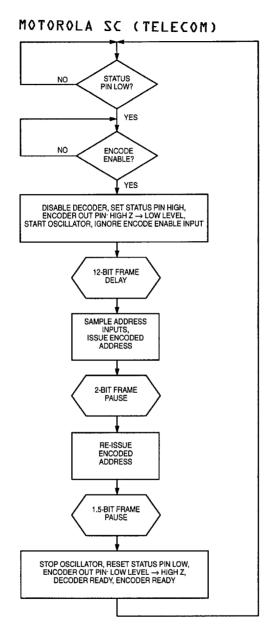
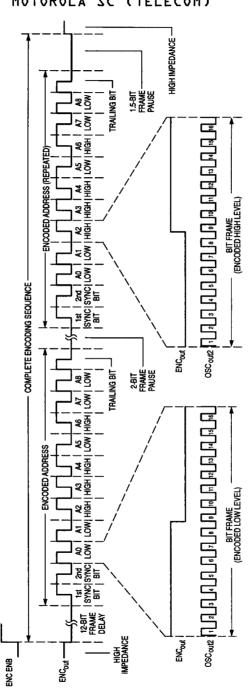
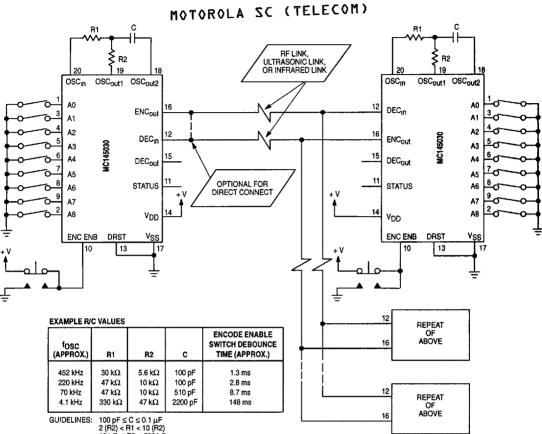


Figure 8. Encoder Flowchart



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 $10 \text{ k}\Omega \leq \text{R2} \leq 500 \text{ k}\Omega$ $B1 \le 1 M\Omega$

The maximum oscillator frequency difference allowable from encoding IC to decoding IC is ± 11%. The ambient temperature and supply voltage differences between ICs affect this frequency difference. Therefore, the tolerances of the frequency-determining components R2 and C are determined by the rule of thumb: $[\Delta \mathsf{R2} + \Delta \mathsf{C} + \Delta \mathsf{f}_{\mathsf{IC}} + \Delta \mathsf{f}_{\mathsf{temp}} + \Delta \mathsf{f}_{\mathsf{sup}}] \leq \pm 11\%,$

where

- R2 = tolerance of R2 in percent
- C = tolerance of C in percent

fIC = IC frequency variation from part to part (expected value: ± 4%)

ftemp = IC frequency variation over temperature (expected value: ± 2% @ 25°C ± 40°)

f_{sup} = IC frequency variation with supply (expected value: ± 2% @ 5 V ± 0.5 V) For

the above variances:
$$[\Delta R2 + \Delta C + (\pm 4\%) + (\pm 2\%) + (\pm 2\%)] \le \pm 11\%$$

$$[\Delta R2 + \Delta C] \le \pm 3\%$$

Choose R2 with a ± 1% tolerance and C2 with a ± 2% tolerance. R1 may be ± 5%.

Figure 10. Application Example