OKI Semiconductor
This version: Nov. 1997
Previous version: Mar. 1996

MSM6660-01,02,03

1/2, 1/3 DUTY LCD DRIVER WITH 3-DOT COMMON DRIVER AND 62-DOT SEGMENT DRIVER

GENERAL DESCRIPTION

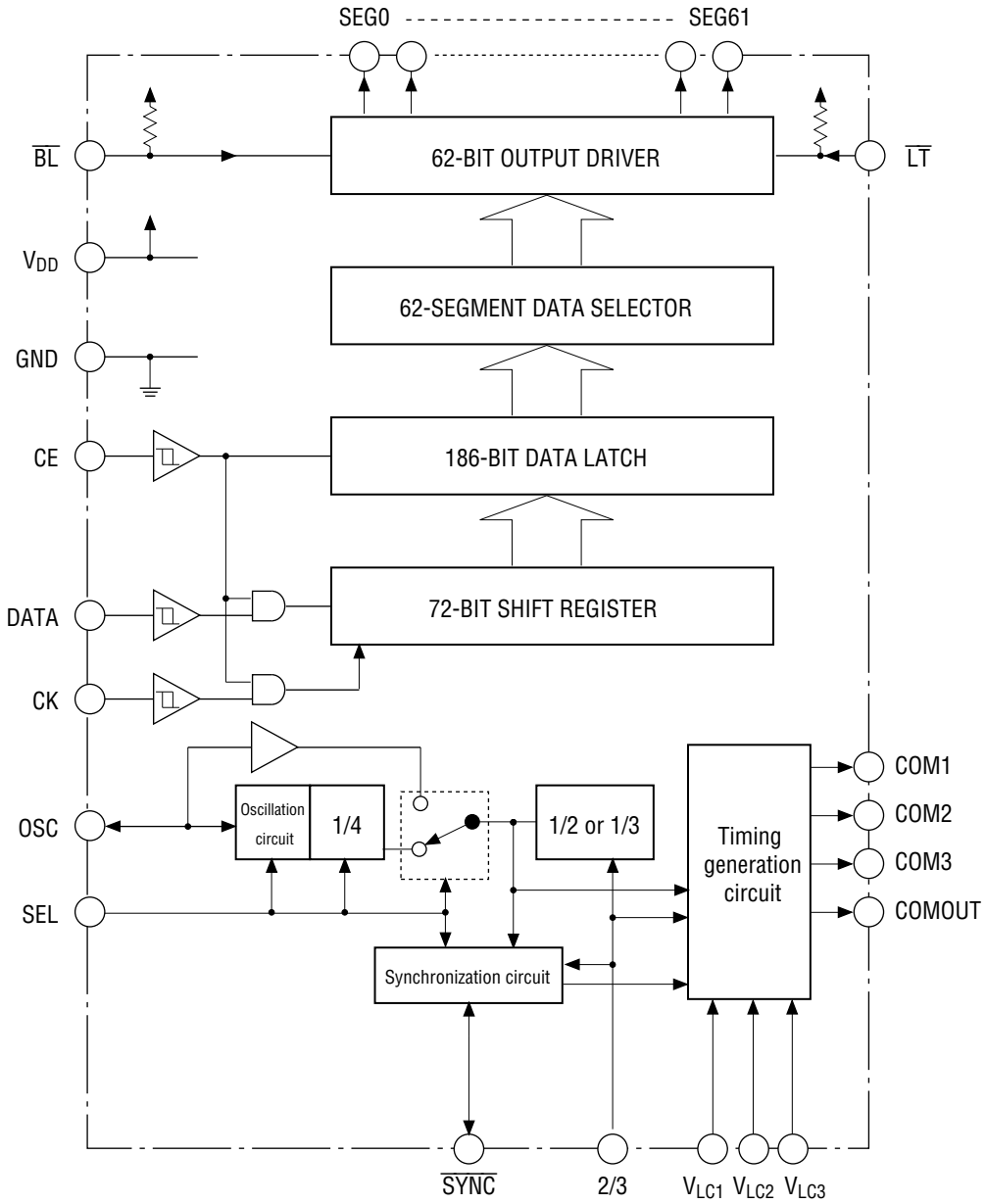
The MSM6660 is a dynamic display LCD driver, equipped with a function that can switch between 1/2 and 1/3 duty. The MSM6660 can directly drive LCDs with up to 124 or 186 segments, depending on whether 1/2 or 1/3 duty is selected.
The MSM6660's on-board display synchronization circuit allows display in a multi-chip configuration.

FEATURES

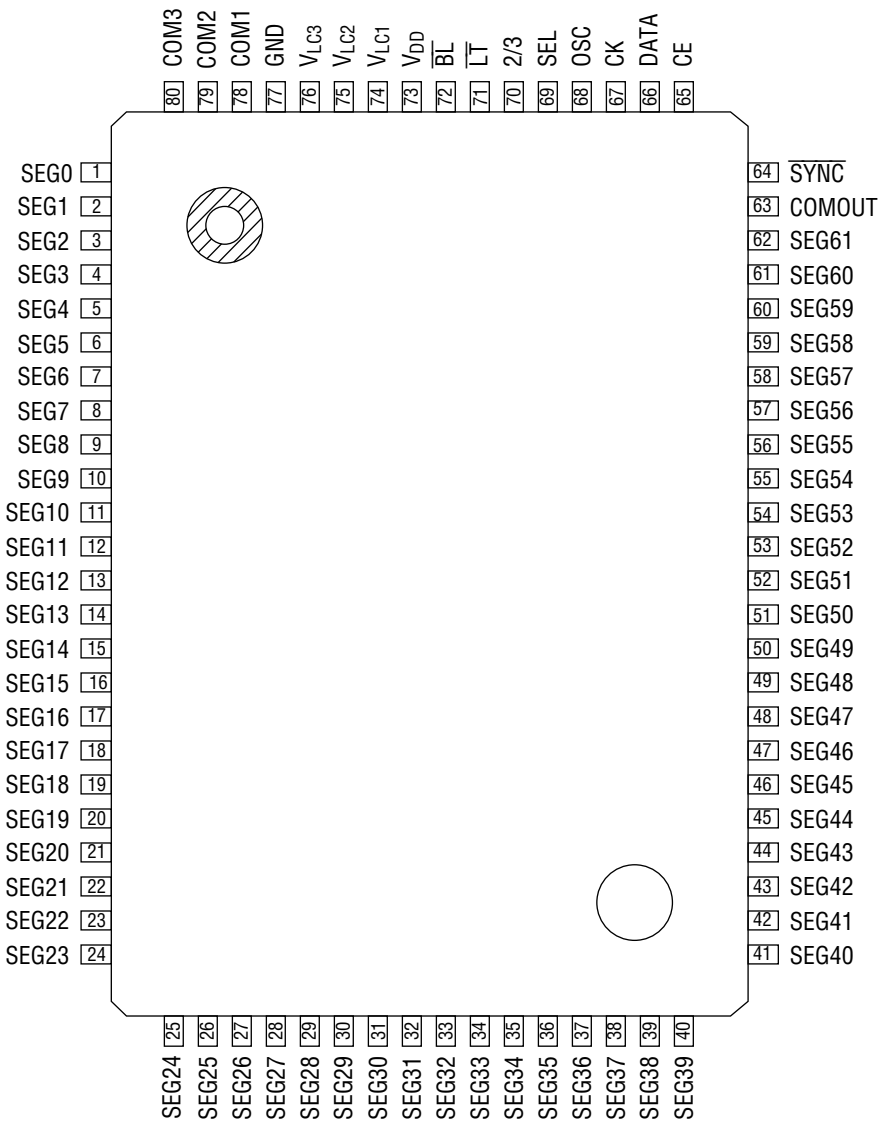
- Power supply voltage : 4 to 6 V (for both logic and LCD driver)
- Operating temperature : –40°C to +85°C
- Applicable LCD duty : 1/2 (1/2 bias), 1/3 (1/3 bias)
- Common output : 2 (1/2 duty), 3 (1/3 duty)
- Segment output : 62
- Serial transfer clock rate : 2 MHz Maximum
- On-board display synchronization circuit which enables display in a multi-chip configuration.
- CE, DATA, and CK are provided for microcomputer interface.
- Handling of display data segments in three blocks enables efficient data transfer.
- Equipped with display-blanking input and display segment test input functions.
- A built-in voltage dividing resistor for bias voltage generation.
  - 01: No internal resistance
  - 02: 1 kΩ internal resistance
  - 03: 30 kΩ internal resistance
- A built-in RC oscillation circuit which uses an external RC.
- Package options:

80-pin plastic QFP (QFP80-P-1420-0.80-K)	(Product name: MSM6660-01GS-K)
	(Product name: MSM6660-02GS-K)
	(Product name: MSM6660-03GS-K)
80-pin plastic QFP (QFP80-P-1420-0.80-BK)	(Product name: MSM6660-01GS-BK)
	(Product name: MSM6660-02GS-BK)
	(Product name: MSM6660-03GS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



80-Pin Plastic QFP

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Ta=25°C	–0.3 to +7	V
Input Voltage	V_{IN}	Ta=25°C	–0.3 to V_{DD}+0.3	V
Power Dissipation	P_D	Ta=85°C	300	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	—	4 to 6	V
"H" Input Voltage	V_{IH}	—	$V_{DD} \times 0.7$ to V_{DD}	V
"L" Input Voltage	V_{IL}	—	0 to $V_{DD} \times 0.3$	V
Shift Frequency	f_{CK}	—	0.1 to 2	MHz
Operating Temperature	T_{op}	—	–40 to +85	°C

Oscillation Circuit

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation Resistance	R_O	—	20	100	120	kΩ
Oscillation Capacitance	C_O	—	0.0047	0.01	0.047	μF
Oscillation Frequency	f_{OSC}	—	—	1.4	—	kHz
COMOUT Frequency	f_{COM}	—	—	350	—	Hz

ELECTRICAL CHARACTERISTICS

DC Characteristics

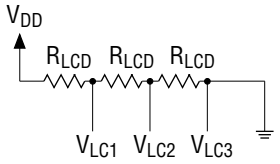
(V_{DD} = 5V±20%, Ta = –40 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
"H" Input Voltage1	V_{IH1}		*1	$V_{DD} \times 0.7$	—	—	V
"L" Input Voltage1	V_{IL1}		*1	—	—	$V_{DD} \times 0.3$	V
"H" Input Voltage2	V_{IH2}		*12	$V_{DD} \times 0.85$	—	—	V
"L" Input Voltage2	V_{IL2}		*12	—	—	0.4	V
Hysteresis Width	V_{HS}		*2	—	0.8	—	V
"H" Input Current	I_{IH}	$V_{IH} = V_{DD}$	*3	–1	—	1	µA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	*4	–1	—	1	µA
"L" Input Current 2	I_{IL2}	V_{DD} = 5V, V_{IL} = GND	*5	–15	–50	–100	µA
Leakage Current	I_Z	$V_I = V_{DD}$ or GND	*6	–1	—	1	µA
"H" Output Voltage	V_{OH}	V_{DD} = 4V, I_{OH} = –0.4mA	*7	3.5	—	—	V
"L" Output Voltage	V_{OL}	V_{DD} = 4V, I_{OH} = 0.4mA	*7	—	—	0.4	V
Segment Output ON Resistance	R_{ONDP}	V_{DD} = 5V, I_O = –0.5mA	*8,*11	—	—	1	kΩ
	R_{ONV1}	V_{LC1} = 3.33V, I_O = ±0.5mA	*8,*11	—	—	3	kΩ
	R_{ONV2}	V_{LC2} = 1.67V, I_O = ±0.5mA	*8,*11	—	—	3	kΩ
	R_{ONV3}	V_{LC3} = 0.0V, I_O = 0.5mA	*8,*11	—	—	3	kΩ
Common Output ON Resistance	R_{ONDP}	V_{DD} = 5V, I_O = –0.5mA	*9,*11	—	—	1	kΩ
	R_{ONV1}	V_{LC1} = 3.33V, I_O = ±0.5m	*9,*11	—	—	3	kΩ
	R_{ONV2}	V_{LC2} = 1.67V, I_O = ±0.5mA	*9,*11	—	—	3	kΩ
	R_{ONV3}	V_{LC3} = 0.0V, I_O = 0.5mA	*9,*11	—	—	3	kΩ
Supply Current	I_{DD}	f_{OSC} = 1.4kHz, no load, CK=DC	*10	—	0.3	1.0	mA

*1 Applicable to all input pins except OSC pin on the master side.
*2 Applicable to CE, CK, and DATA input.
*3 Applicable to CE, CK, DATA, SEL, 2/3, $\overline{BL}$, and $\overline{LT}$.
*4 Applicable to CE, CK, DATA, SEL, and 2/3.
*5 Applicable to $\overline{BL}$ and $\overline{LT}$ input.
*6 Applicable to $\overline{SYNC}$.
*7 Applicable to $\overline{SYNC}$ and COMOUT.
*8 Applicable to SEG0 - SEG61.
*9 Applicable to COM1 - COM3.
*10 If a voltage-dividing resistor for bias voltage generation is included (- 02 and - 03), the value does not include the current that flows through the resistor.
*11 If a voltage-dividing resistor for bias voltage generation is included (- 02 and - 03), the output ON resistance value depends on the built-in dividing resistor.
*12 Applicable to the OSC pin on the master side.

Voltage-dividing resistor for bias voltage generation

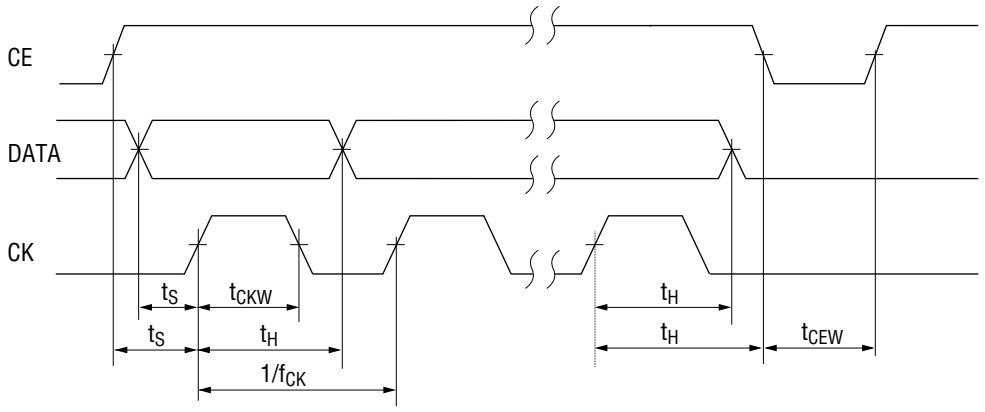
Code Name	Symbol	Condition	Min.	Typ.	Max.	Unit
-02	R_{LCD}	Ta = –40 to +85°C	0.6	1	1.4	kΩ
-03	R_{LCD}	Ta = –40 to +85°C	10	30	100	kΩ

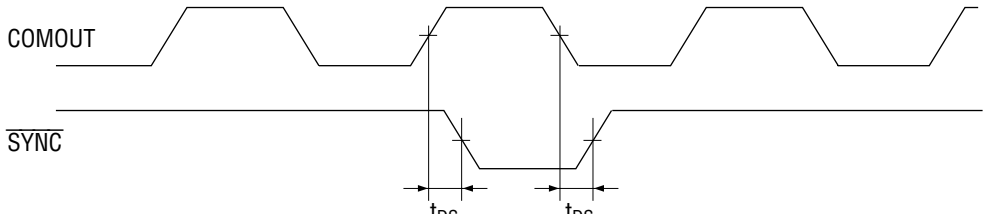


AC Characteristics

(V_{DD} = 5V ± 20%, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum Clock Frequency	f_{CK}	—	2	—	—	MHz
Clock Pulse Width	t_{CKW}	—	200	—	—	ns
Data Set-up Time	t_S	—	200	—	—	ns
Data Hold Time	t_H	—	200	—	—	ns
CE Pulse Width	t_{CEW}	—	200	—	—	ns
COMOUT-$\overline{SYNC}$ Delay Time	t_{DS}	C_L=50pF	—	—	40	ns
Oscillation Frequency	f_{OSC}	OSC Pin Operating Frequency	—	1.4	50	kHz





FUNCTIONAL DESCRIPTION

Pin Functional Description

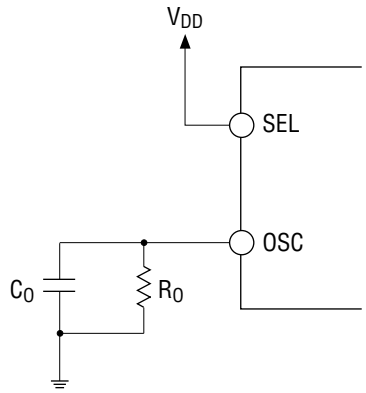
- **OSC (pin 68)**

When the master mode is selected, connect an external resistor and capacitor for the RC oscillation circuit to this pin. When the slave mode is selected, this pin becomes the input pin for an external clock signal.

The relationship of oscillation frequency to external C_O and R_O, when the master mode is selected, is shown below.

$$f_{OSC} \fallingdotseq \frac{1}{0.69 \times R_O \times C_O} \quad (Ta = 25°C)$$

Example: When $C_O = 0.01\mu F$ and $R_O = 100\,k\Omega$, the oscillation frequency, f_{OSC}, is approximately 1.4 kHz.



- **CE (pin 65)**

This is a chip select input pin. Input data is valid only when this pin is set to "H". Data that is input into the 72-stage shift register synchronously with the rising edge of CK will be latched with the falling edge of this pin, and the display will be updated. A Schmitt trigger is built into the input area.

- **DATA (pin 66)**

This is a data input pin. Data input is valid only when the CE pin is set to "H". The 72-stage shift register contents are latched with the falling edge of this pin, and the display will be updated. A Schmitt trigger is built into the input area.

- **CK (pin 67)**

This is a serial data shift lock input pin. Data is input synchronously with the rising edge of the shift clock. A Schmitt trigger is built into the input area. Data can be latched even if the shift clock is stopped, since a static shift register is used.

- **SEL (pin 69)**

This is an input pin used to switch between the master and the slave modes when a multi-chip configuration is used. Set this pin to "H" to select the master mode, and to "L" to select the slave mode.

- **$\overline{\text{SYNC}}$ (pin 64)**

When the master mode is selected, this pin becomes an output pin for synchronous signals.

- **2/3 (pin 70)**
  This pin is used to switch between 1/2 and 1/3 duty.
  Set this pin to "H" to select 1/2 duty, and to "L" to select 1/3 duty.

- **COMOUT (pin 63)**
  This is an output pin for clock synchronization. A frequency equal to $f_{OSC}/4$ is output from this pin.

- **V_{LC1} (pin 74), V_{LC2} (pin 75) and V_{LC3} (pin 76)**
  When the code is -01, these pins are used as input pins for LCD bias voltage. The V_{LC3} pin should be connected with GND. The settings for these pins should be as follows:
  $V_{DD} \geq V_{LC1} \geq V_{LC2} \geq V_{LC3} = GND$
  When the code is -02 or -03, V_{LC1} and V_{LC2} pins should be left open, and V_{LC3} pin connected with GND since a voltage-dividing resistor for bias voltage generation has been built in. (However, when the code setting is -02 or -03, and if 1/2 duty is selected, V_{LC1} and V_{LC2} should be externally shorted.)

- **COM1-COM3 (pins 78 to 80)**
  These are common signal output pins for driving the LCD. In the 1/2 duty mode, leave the COM3 pin open.

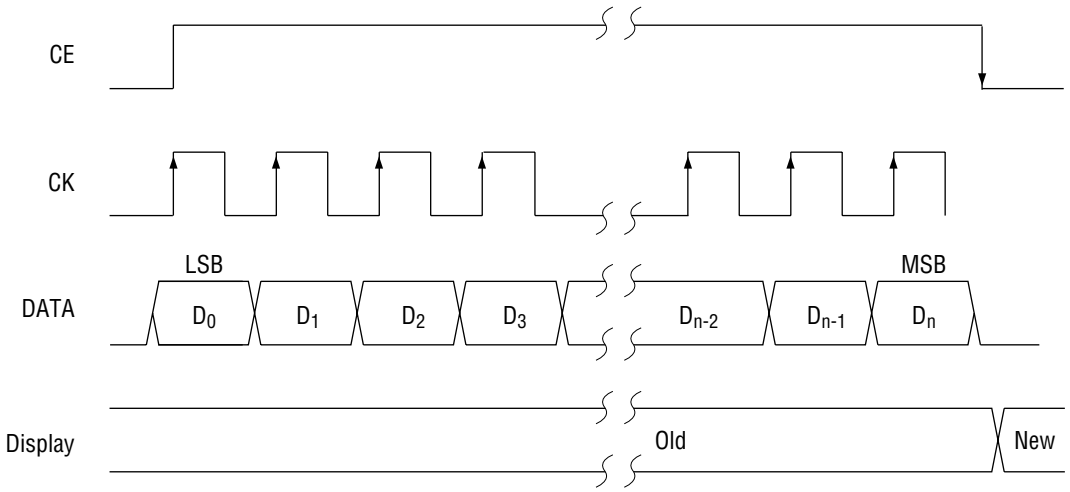
- **SEG0-SEG61 (pins 1 to 62)**
  These are segment signal output pins for driving the LCD. 1/2 or 1/3 duty can be selected using the 2/3 pin, and 1/2 or 1/3 bias can be selected using pins V_{LC1} through V_{LC3}.

- **$\overline{LT}$ (pin 71)**
  This is an input pin for controlling the display on the LCD. If this pin is set to "L", all segments will be turned on. A pull-up resistor is included.

- **$\overline{BL}$ (pin 72)**
  This is an input pin for controlling the display on the LCD. If this pin is set to "L", all segments will be turned off. A pull-up resistor is included.

Data Input

Display data should be input according to the timing diagram below.



* Display Data

Duty Mode	2/3 Pin	Data Length	COM Data
1/2 Duty	H	48-Bit (D0 - D47) × 3	COM1: D0, D2.....D0+2n COM2: D1, D3.....D1+2n n = 0 - 61
1/3 Duty	L	72-Bit (D0 - D71) × 3	COM1: D0, D3.....D0+3n COM2: D1, D4.....D1+3n COM2: D2, D5.....D2+3n n = 0 - 61

* Address Data

The most significant 3 bits (the last 3 bits) contain the address data.

Address data: "100" — SEG0 - SEG20
"010" — SEG21 - SEG41
"001" — SEG42 - SEG61

Since the last 3 bits correspond to each group of segments, if the address is "110", SEG0 - SEG20 and SEG21 - SEG41 are all updated at a time in accordance with the data.

1) Data format when 1/2 duty (124 segments) is selected.

D0	D1	D2	D3	D4	D5		D39	D40	D41	D42-	D44	D45	D46	D47
S0 C1	S0 C2	S1 C1	S1 C2	S2 C1	S2 C2		S19 C2	S20 C1	S20 C2			1	0	0

D42 - D44 are Dummy Data

D0	D1	D2	D3	D4	D5		D39	D40	D41	D42-	D44	D45	D46	D47
S21 C1	S21 C2	S22 C1	S22 C2	S23 C1	S23 C2		S40 C2	S41 C1	S41 C2			0	1	0

D42 - D44 are Dummy Data

D0	D1	D2	D3	D4		D37	D38	D39	D40-	D44	D45	D46	D47
S42 C1	S42 C2	S43 C1	S43 C2			S60 C2	S61 C1	S61 C2			0	0	1

D40 - D44 are Dummy Data

2) Data format when 1/3 duty (186 segments) is selected.

D0	D1	D2	D3	D4	D5		D60	D61	D62	D63-	D68	D69	D70	D71
S0 C1	S0 C2	S0 C3	S1 C1	S1 C2	S1 C3		S20 C1	S20 C2	S20 C3			1	0	0

D63 - D68 are Dummy Data

D0	D1	D2	D3	D4	D5		D60	D61	D62	D63-	D68	D69	D70	D71
S21 C1	S21 C2	S21 C3	S22 C1	S22 C2	S22 C3		S41 C1	S41 C2	S41 C3			0	1	0

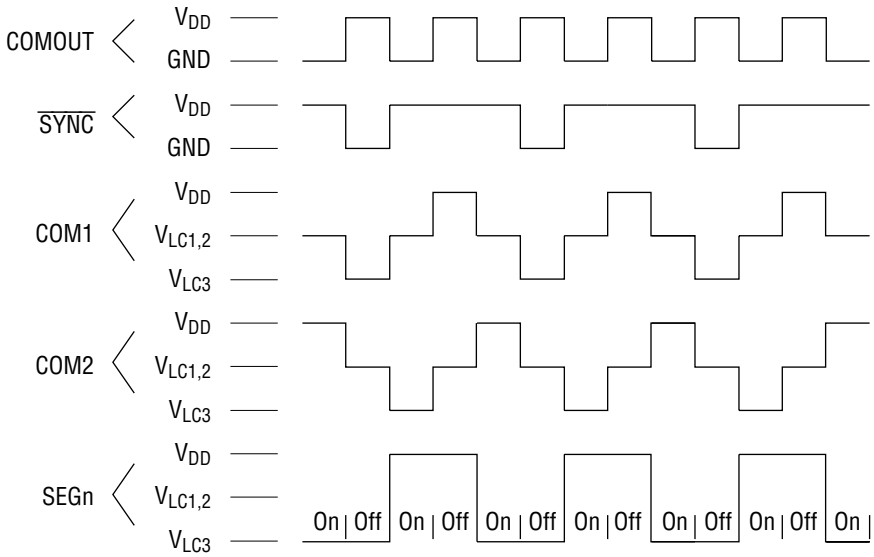
D63 - D68 are Dummy Data

D0	D1	D2	D3	D4		D57	D58	D59	D60-	D68	D69	D70	D71
S42 C1	S42 C2	S42 C3	S43 C1			S61 C1	S61 C2	S61 C3			0	0	1

D60 - D68 are Dummy Data

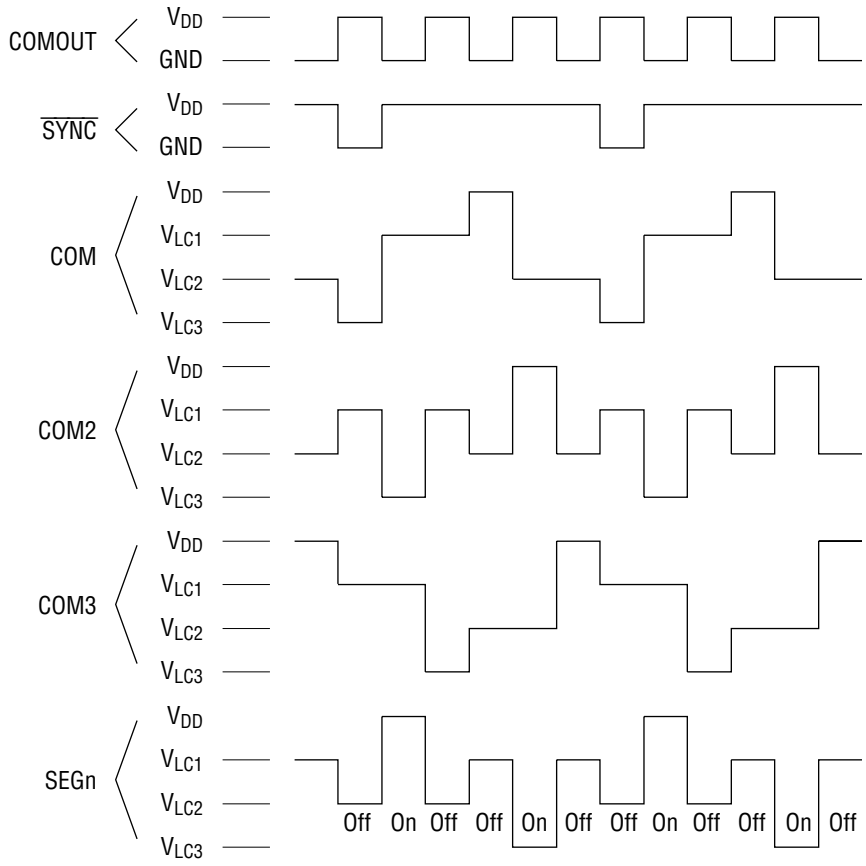
LCD Display Timing

1) 1/2 duty mode (2/3 = "H")



Note: When 1/2 duty is selected and 1/2 bias is used, perform the following:
- When the code is -01, short V_{LC1} and V_{LC2}, and supply the bias voltage.
- When the code is -02 or -03, externally short V_{LC1} and V_{LC2}.

2) 1/3 duty mode (2/3 = "L")



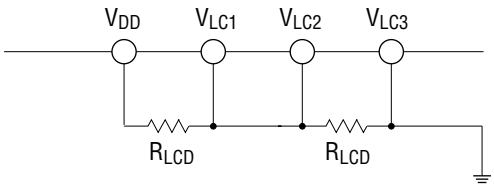
Pin Functions in a Multi-chip Configuration

When MSM6660 ICs are used in a multi-chip configuration, one of them is used in the master mode to generate the common frequency and the synchronization signal. These signals are then received by the slave mode ICs to enable synchronous operation.

Symbol	Pin	Master Mode LSI	Slave Mode LSI
COMOUT	63	Connect to Slave IC OSC	Open (Unused)
$\overline{\text{SYNC}}$	64	Connect to Slave IC $\overline{\text{SYNC}}$	Connect to Master IC $\overline{\text{SYNC}}$
OSC	68	Connect an external resistor and capacitor	Connect to Master IC COMOUT
SEL	69	"H" (V_{DD}) level	"L" (GND) level

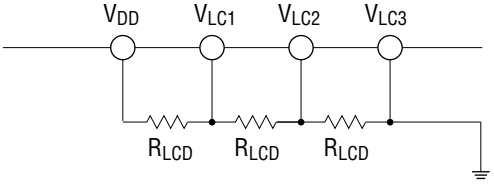
LCD Bias Voltage Application Method

1) For 1/2 bias (when 1/2 duty is selected)



Note: The above case is for code -01. When the code is -02 or -03, an external voltage-dividing resistor is not needed, because it is already built into the type signified by these settings. However, pins V_{LC1} and V_{LC2} must be shorted externally.

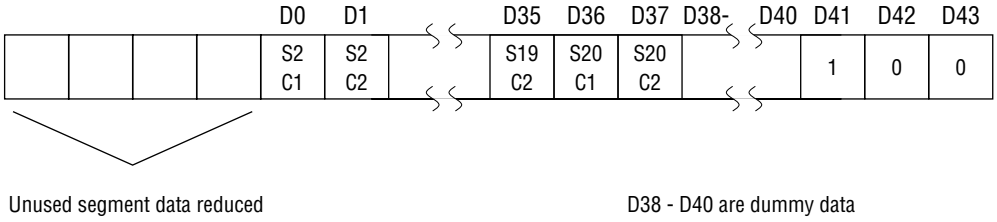
2) For 1/3 bias (when 1/3 duty is selected)



Note: The above case is for the code -01. When the code is -02 or -03, an external voltage-dividing resistor is not needed, because it is already built into the type signified by these settings. Leave V_{LC1} through V_{LC3} open.

Method of Reducing the Transfer Time When Unused Segments Exist

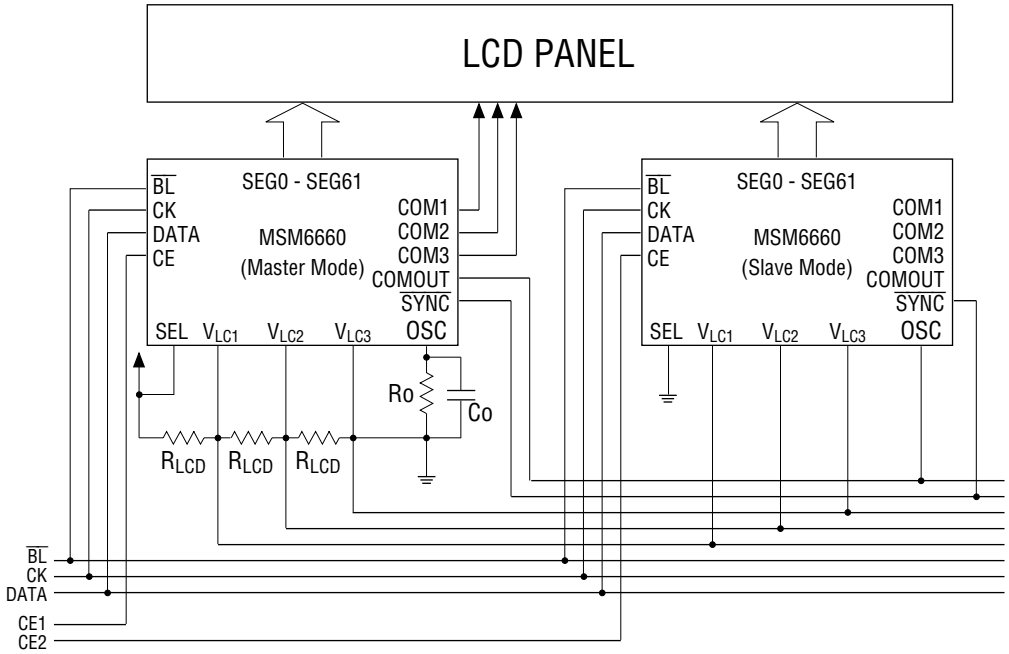
When unused segments exist, it is not required to transfer the data of unused segments. This allows the data transfer time to be reduced. However, the last 3 bits are address data.



When SEG0 and 1 are not used, the data can be reduced from the original 48 bits to 44 bits.

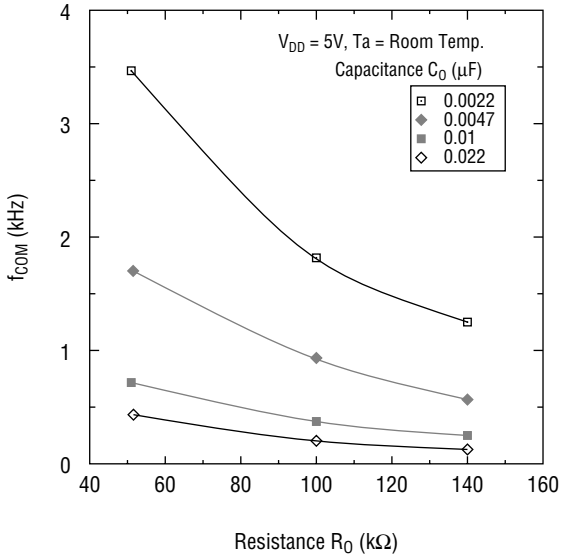
APPLICATION CIRCUIT

For 1/3 duty, 1/3 bias (when the code setting is -01)

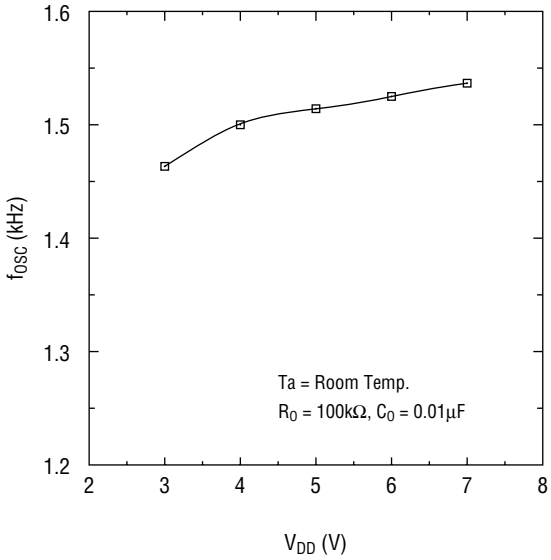


REFERENCE DATA

f_{COM} vs. R_O, C_O



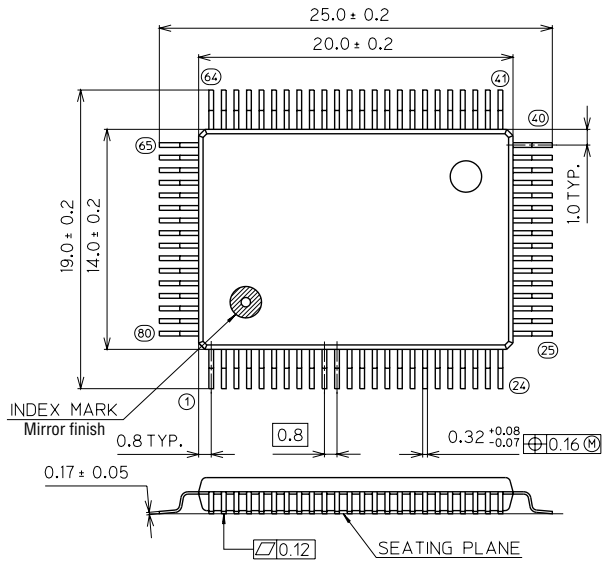
f_{OSC} vs. V_{DD}

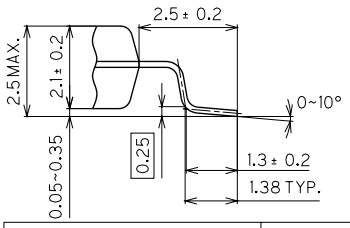


PACKAGE DIMENSIONS

(Unit : mm)

QFP80-P-1420-0.80-K





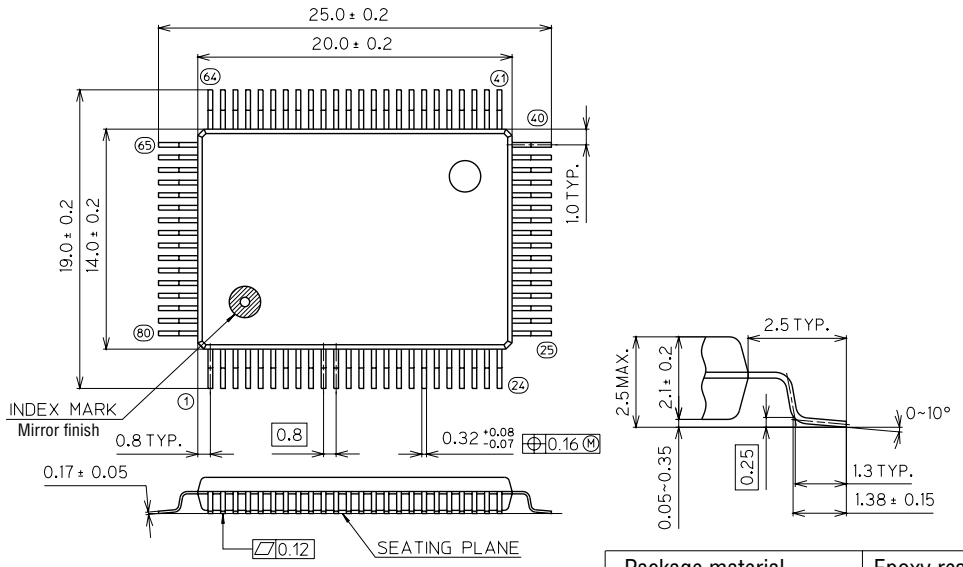
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.27 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP80-P-1420-0.80-BK



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Solder plate thickness	5 μm or more
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