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μPD71065/66 Floppy-Disk Interface

Description

The μPD71065 and μPD71066 are CMOS devices that interface a floppy-disk drive (FDD) with a floppy-disk controller (FDC). The controller can be μPD765A/B, μPD7265, μPD72065/B, μPD72066, μPD7260, or one of the FD179X series.

The floppy-disk interface can operate at various data rates, including the 300-kb/s rate that results from using high-density 5-inch drives with media formatted at the standard 250-kb/s rate. Also, the μPD71065/66 generates the write clock needed by the selected controller and provides synchronous switching when changing data rates.

Features

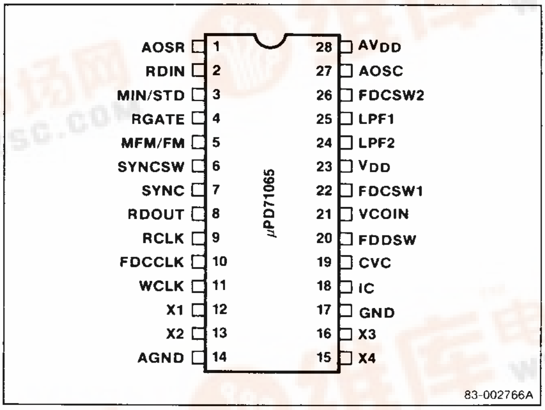
- ☐ Compatible with all industry-standard controllers
- ☐ Multiple data rates: 500/300/250/150/125 kb/s
- ☐ Internal or external sync field detection logic
- ☐ Head-loading timer for FD179X-series controllers
- ☐ No analog adjustments required
- ☐ CMOS, low power consumption
- ☐ 5-volt power supply

Ordering Information

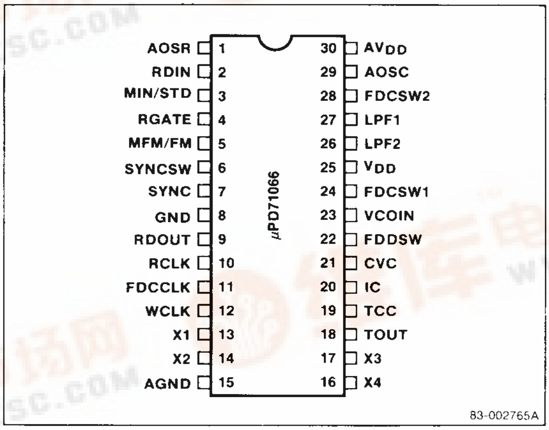
Part Number	Package	Internal Timer
μPD71065G	28-pin plastic SO	Not included
μPD71066CT	30-pin plastic shrink DIP	Implemented to FD179X-series controllers as head-loading timer.

Pin Configurations

28-Pin Plastic SO



30-Pin Plastic Shrink DIP



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Pin Identification

Symbol	Input/Output	Function
ACOS		Capacitor connection pin for analog one-shot
AGND		Ground for analog circuits
AOSR		Resistor connection pin for analog one-shot
AV_{DD}		Power supply for analog circuits
CVC		Capacitor connection pin for VCO
FDCCLK	Output	Clock to FDC
FDCSW1	Input*	FDC selection pin or timer trigger input
FDCSW2	Input*	FDC selection pin
FDDSW	Input*	Data transfer rate selection pin
GND		Ground
IC		Internally connected; should be left open
LPF1, LPF2	Output	Connection pins to external lowpass filter
MFM/FM	Input*	Recording density selection pin
MIN/STD	Input*	5- or 8-inch FDD selection pin
RCLK	Output	Read data sampling clock
RDOUT	Output	Read data to FDC
RGATE	Input*	Read enable/disable
RDIN	Input*	Read data from FDD
SYNC	Input*	External PLL gain selection
SYNCSW	Input*	Determines whether gain selection is internal or external
TCC		External RC time constant connection to internal timer (μPD71066)
TOUT	Output	Timer signal (μPD71066)
VCOIN	Input	External lowpass filter output to internal VCO
V_{DD}		+5-volt power supply
WCLK	Output	Write clock to FDC
X1, X2		Connection pins for 16-MHz crystal (X1, X2) or external clock input (X1)
X3, X4		Connection pins for 19.2-MHz crystal (X3, X4) or external clock input (X3)

*Input pin has an on-chip pull-up resistor

Pin Functions

The following paragraphs supplement the brief descriptions of certain pins in the preceding table. Pin symbols are in alphabetical order.

FDCSW1 and FDCSW2. The μPD71065/66 is configured for the applicable FDC by applying logic levels L and H (or open) to these pins.

FDCSW1	FDCSW2	Floppy-Disk Controller
Open or H	Open or H	μPD765A/7265
L	Open or H	μPD7260
*	L	FD179X series

*FDCSW1 is the trigger input to the timer circuit when FDCSW2 is low.

FDDSW. The logic level applied to this pin selects the data transfer rate of the FDD.

FDDSW	Data Transfer Rate
Open or H	500/250/125 kb/s
L	500/250/300/150 kb/s

MFM/FM Pin. The logic level applied to this pin and the FDCSW2 pin selects the modulation type. Double-density and single-density recording use MFM (modified FM) and FM modulation, respectively.

FDCSW2	MFM/FM	Modulation
H	H	MFM
H	L	FM
L	H	FM
L	L	MFM

MIN/STD. Logic level L on this pin selects a 5-inch FDD. An open or H selects an 8-inch FDD.

RDIN. This is a composite read data and clock signal input from the FDD.

RDOUT. The read data output from this pin is synchronized with the read clock (RCLK) derived from the RDIN composite signal.

RGATE. In conjuction with FDCSW2, RGATE enables or disables the read operation that is sent from the FDC.

FDCSW2	RGATE	Read Operation
H	H	Enable
H	L	Disable
L	H	Disable
L	L	Enable

SYNC and SYNCSW. The PLL gain is determined by the intput signal at the SYNC pin and the logic levels at the FDCSW1 and SYNCSW pins.

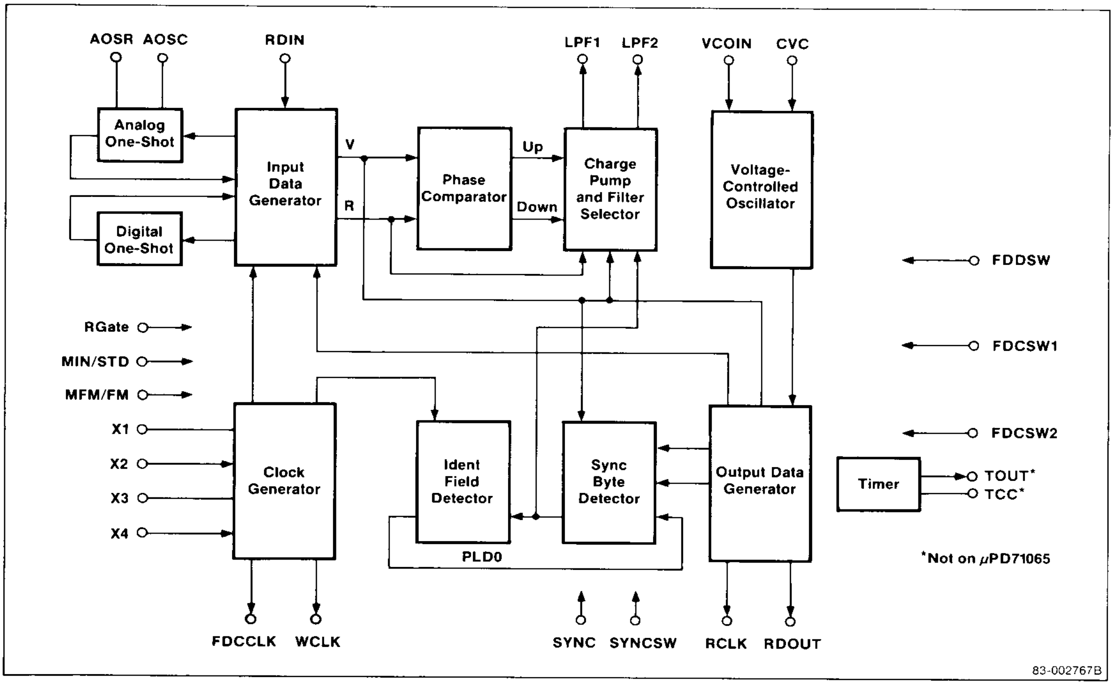
FDCSW1	SYNCSW	SYNC	PLL Gain
Open or H	Open or H	H (1)	Low
		L (1)	High
	L	H (2)	Low
		L (2)	High

Note:

(1) Input signal at SYNC is the PLL gain selection signal between the ID and DATA fields.

(2) Input signal at SYNC Is the SYNC field detection signal from the FDC.

Block Diagram



Functions of the block diagram components are explained below.

Clock Generator. Using both 16-MHz and 19.2-MHz oscillators, outputs clock signals corresponding to the mode used to the FDCCLK and WCLK pins.

Input Data Generator. According to the input data, generates the R and V signals to be input to the phase comparator. In addition to this, the input data generator determines whether the analog one-shot circuit or the digital one-shot circuit is used.

Charge Pump and Filter Selector. According to the PLL (phase-locked loop) gain selection signal, enables or disables the LPF2 side charge pump to control the PLL gain.

Output Data Generator. Generates the window signal (RCLK) and read data signal (RDOUT) depending on the mode and FDC to be used.

Sync Byte Detector. Detects the sync field within 16 to 20 pulses regardless of FM or MFM mode.

Ident Field Detector. Determines whether the sync field detected by the sync byte detector is ID or DATA field and sets the PLL gain.

Basic External Circuit

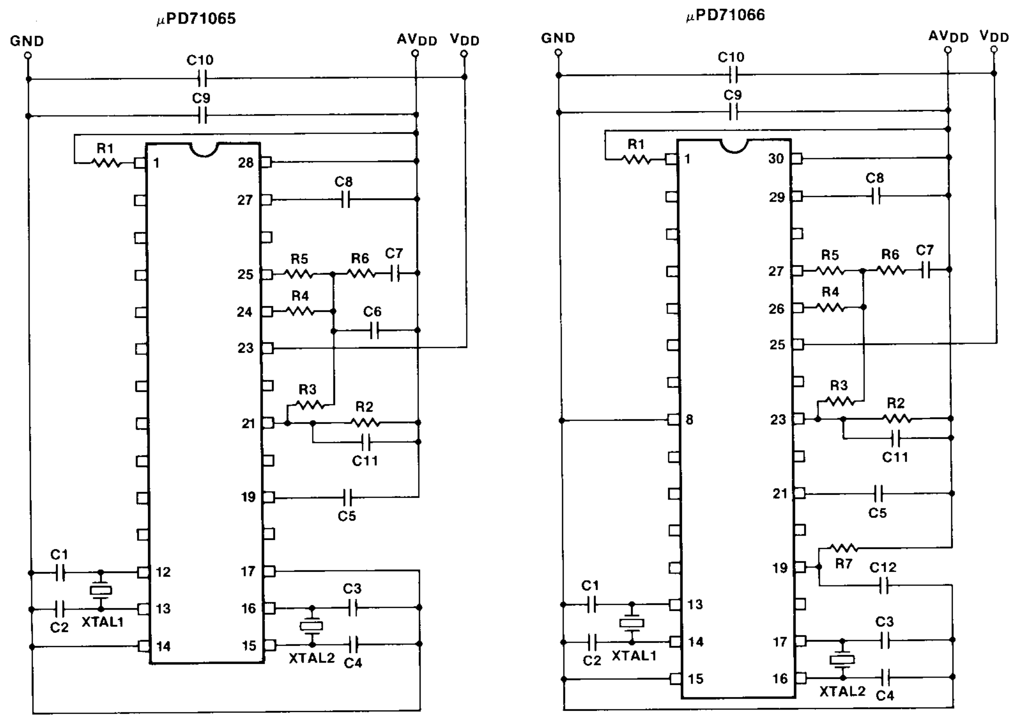
Figure 1 shows the basic external circuit including the lowpass filter and crystals. The data transfer rate is selected by strapping pins FDDSW, MIN/STD, and MFM/FM to L (low) or open (high). See table 1.

The VCO frequency and the phase delay between RDIN and RDOUT can be optimized by adjusting resistors R2 and R1, respectively.

VCO Frequency

For this procedure, the data transfer rate is undefined. Strap RGATE to H and RDIN to L. Adjust resistor R2 to set the VCO frequency at the RCLK pin to the same numerical value as the data transfer rate; for example, 500 kHz and 500 kb/s.

Figure 1. Basic External Circuit



C1	22 pF	R1	3 kΩ	XTAL1	16 MHz
C2	22 pF	R2	30 kΩ	XTAL2	19.2 MHz
C3	22 pF	R3	22 kΩ		
C4	22 pF	R4	1 kΩ		
C5	10 pF	R5	1.5 kΩ		
C6	1800 pF	R6	560 Ω		
C7	33,000 pF	R7	33 kΩ min		
C8	33 pF				
C9	10,000 pF				
C10	10,000 pF				
C11	1000 pF				
C12	1 µF				

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Data Read Phase Delay

For this procedure, set the data transfer rate to 500 kb/s, set the RDIN signal to a 2-µs cycle time, and strap RGATE to H. Adjust resistor R1 to set the value of t_{STW} (figure 2) to 950 ns.

Figure 2. Read Data Timing Diagram

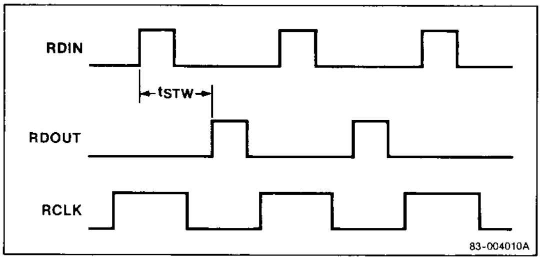

Table 1. Data Transfer Rate Selection

Floppy-Disk Controllers	Data Transfer Rate (kb/s)	Clock Output Frequencies from µPD71065/71066			Selection Pins (Note 1)		
		FDCCLK (MHz)	RCLK (kHz)	WCLK (kHz)	FDDSW	MIN/STD	MFM/FM
µPD765A, µPD7265, µPD72065, µPD72066 (Note 2)	250	4	250	500	Open	Open	Open
	125	4	125	250	Open	Open	L
	500	8	500	1 MHz	Open	L	Open
	250	8	250	500	Open	L	L
	300	4.8	300	600	L	Open	Open
	150	4.8	150	300	L	Open	L
	500	8	500	1 MHz	L	L	Open
	250	8	250	500	L	L	L
µPD7260 (Note 3)	250	4	500	500	Open	Open	Open
	125	4	250	250	Open	Open	L
	500	8	1 MHz	1 MHz	Open	L	Open
	250	8	500	500	Open	L	L
	300	4.8	600	600	L	Open	Open
	150	4.8	300	300	L	Open	L
	500	8	1 MHz	1 MHz	L	L	Open
	250	8	500	500	L	L	L
FD179X Series (Note 4)	250	1	250	500	Open	Open	L
	125	1	125	250	Open	Open	Open
	500	2	500	1 MHz	Open	L	L
	250	2	250	500	Open	L	Open
	300	1.2	300	600	L	Open	L
	150	1.2	150	300	L	Open	Open
	500	2	500	1 MHz	L	L	L
	250	2	250	500	L	L	Open

Note:

(1) Selection pin states: L = low; Open = open or H (high)

(2) µPD765A/7265/72065/72066:
FDCSW1 and FDCSW2 = Open

(3) µPD7260:
FDCSW1 = L and FDCSW2 = Open.
FDCLK clock is not used

(4) FD179X Series:
FDCSW1 = Don't care and FDCSW2 = L.
WCLK clock is not used.

Electrical Characteristics

Figures 3 through 8 are test circuits for verifying certain parameters in the dc and ac characteristics tables.

Absolute Maximum Ratings

$T_A = +25°C$

Power supply voltage, V_{DD}	−0.3 to +6 V
Input voltage, V_I	−0.3 to V_{DD} + 0.3 V
Output voltage, V_O	−0.3 to V_{DD} + 0.3 V
Operation temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−40 to +125°C

DC Characteristics

$T_A = -10$ to $+70°C$; $V_{DD} = +5\ V \pm 10\%$

		Limits					
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions	Test Circuit
Input voltage, low	V_{IL}	−0.3		0.8	V		
Input voltage, high	V_{IH}	2.2		V_{DD} + 0.3	V		
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2 mA	
Output voltage, high	V_{OH}	0.7 V_{DD}		V_{DD}	V	I_{OH} = − 200 μA	
Clock input level	$V_{Kp\text{-}p}$	1		V_{DD}	V		Figure 5
Input leakage current, low	I_{LIL}	−150		−50	μA	V_I = 0 V	
Input leakage current, high	I_{LIH}	−10		+10	μA	$V_I = V_{DD}$	
Output leakage current, low	I_{LOL}	−10			μA	V_O = 0.45 V	
Output leakage current, high	I_{LOH}			+10	μA	$V_O = V_{DD}$	
Power supply current	I_{DD}			25	mA	XTAL: 16 MHz, 19.2 MHz	Figure 3
				20	mA	XTAL: 16 MHz	Figure 4

AC Characteristics

$T_A = -10$ to $+70$°C; $V_{DD} = +5$ V ±10%

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	Test Circuit
Rise time	t_R	0		20	ns		
Fall time	t_F	0		20	ns		
RDOUT setup time to RCLK ↑	t_{SRR}	40			ns	For μPD7260	Figure 6
CLK high/low level width	t_{KK}	20			ns		
VCO oscillation frequency	f_o			8	MHz	$V_F = V_{DD}$	Figure 7
VCO free-run frequency	f_i	3.6	4	4.4	MHz	FDDSW = H, V_F = open	
		2.1	2.4	2.7	MHz	FDDSW = L, V_F = open	
VCO control voltage sensitivity	K_V	2.5	3.5	4.6	MHz/V	$\lvert(V_{DD}/2) - V_F\rvert \leq 0.5$ V	
K_V voltage coefficient	$\Delta K_V/V_{DD}$	−1	−19	−22	%/V		
f_i power supply voltage coefficient	$\Delta f_i/V_{DD}$	0		5	%/V		
f_i temperature coefficient	$\Delta f_i/T_A$	0	−500	−1000	ppm/°C		
Phase detect sensitivity	K_P	0.7	0.8	0.9	V/rad		
RCLK jitter	t_j	0	30	50	ns	500-kb/s mode	Figure 8
RDIN ↑ to RDOUT ↑ delay time	t_{DRR}	900	950	1000	ns		
Capture range (Note 1)	f_{CAP}	537		427	kHz	500-kb/s mode	
		286		213	kHz	250-kb/s mode	
		143		107	kHz	125-kb/s mode	
		343		256	kHz	300-kb/s mode	
		172		128	kHz	150-kb/s mode	
FDCCLK ↑ to WCLK ↑ delay time (Note 2)	t_{DFWR}			30	ns	$C_L = 15$ pF	Figure 1
FDCCLK ↑ to WCLK ↓ delay time (Note 2)	t_{DFWF}			30	ns	$C_L = 15$ pF	

Note:

(1) The frequencies in the Max and Min columns are the lower and upper limits, respectively, of the capture range. For example, in the 500-kb/s mode, the capture range is from 427 kHz (or lower) to 537 kHz (or higher).

(2) Clock outputs to FDC.

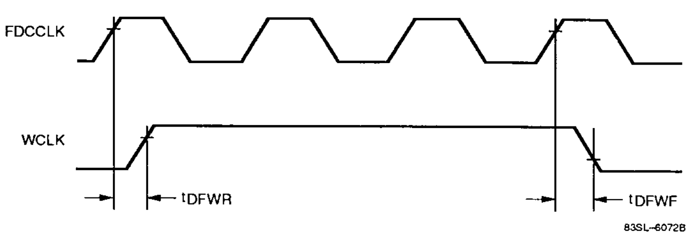

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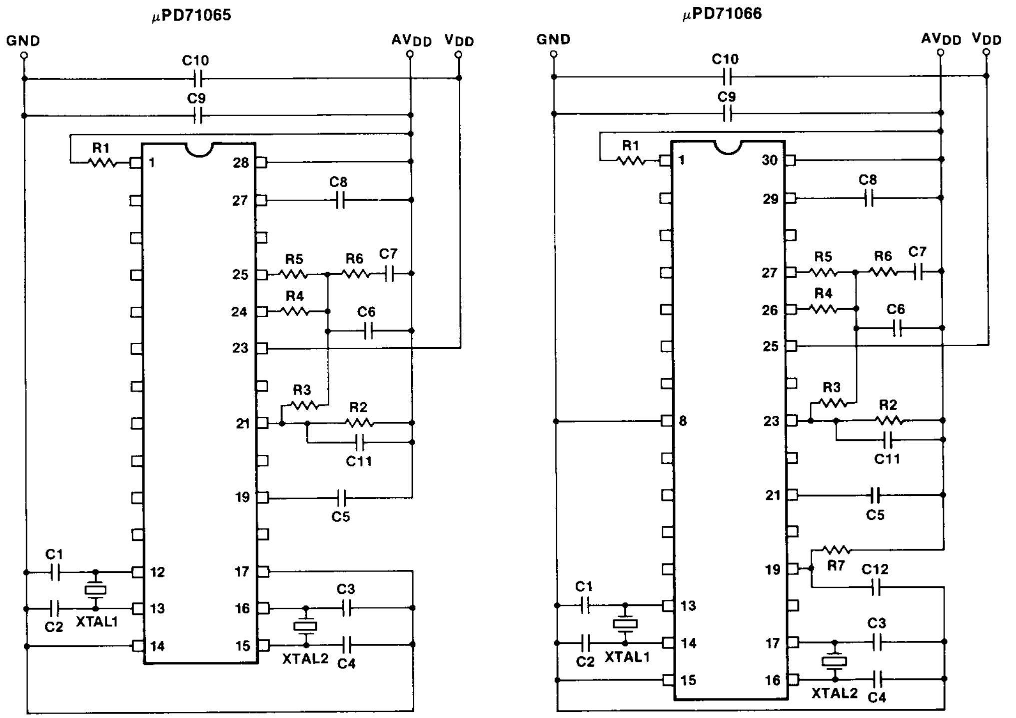
Figure 3. Test Circuit 1



C1	22 pF	R1	3 kΩ	XTAL1	16 MHz
C2	22 pF	R2	27 kΩ	XTAL2	19.2 MHz
C3	22 pF	R3	10 kΩ		
C4	22 pF	R4	1 kΩ		
C5	10 pF	R5	7.5 kΩ		
C6	1800 pF	R6	560 Ω		
C7	22,000 pF	R7	33 kΩ min		
C8	33 pF				
C9	10,000 pF				
C10	10,000 pF				
C11	120 pF				
C12	1 μF				

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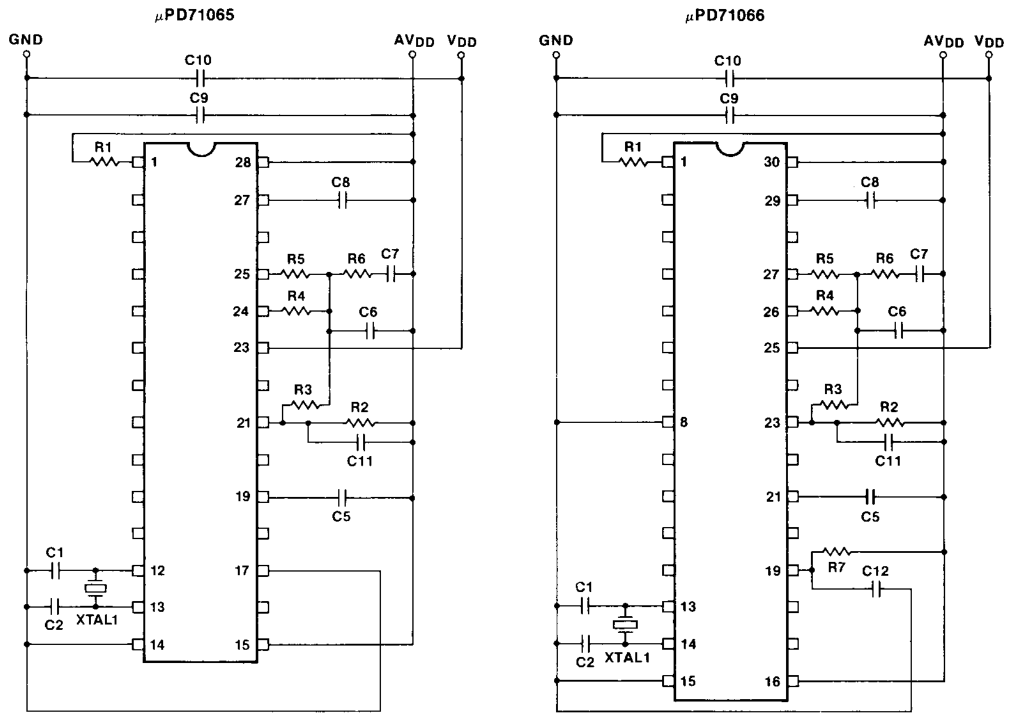
Figure 4. ***Test Circuit 2***



C1	22 pF	R1	3 kΩ	XTAL	16 MHz
C2	22 pF	R2	27 kΩ		
C5	10 pF	R3	10 kΩ		
C6	1800 pF	R4	1 kΩ		
C7	22,000 pF	R5	7.5 kΩ		
C8	33 pF	R6	560 Ω		
C9	10,000 pF	R7	33 kΩ min		
C10	10,000 pF				
C11	120 pF				
C12	1 μF				

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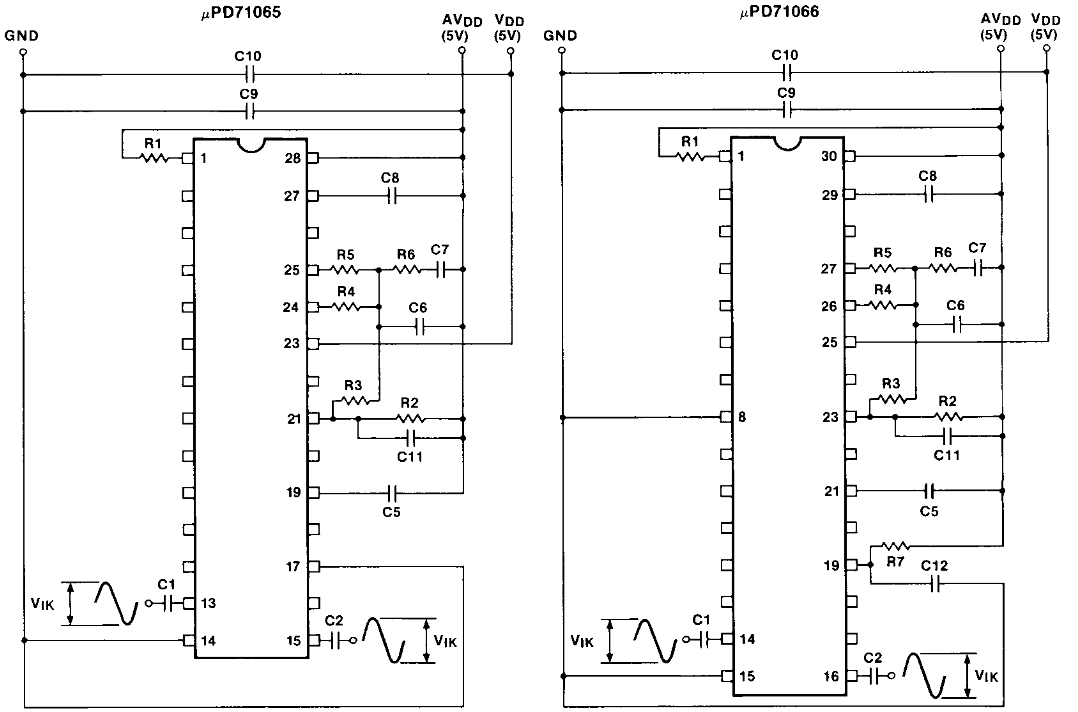
Figure 5. Test Circuit 3



C1	22 pF	R1	3 kΩ
C2	22 pF	R2	27 kΩ
C5	10 pF	R3	10 kΩ
C6	1800 pF	R4	1 kΩ
C7	22,000 pF	R5	7.5 kΩ
C8	33 pF	R6	560 Ω
C9	10,000 pF	R7	33 kΩ min
C10	10,000 pF		
C11	120 pF		
C12	1 μF		

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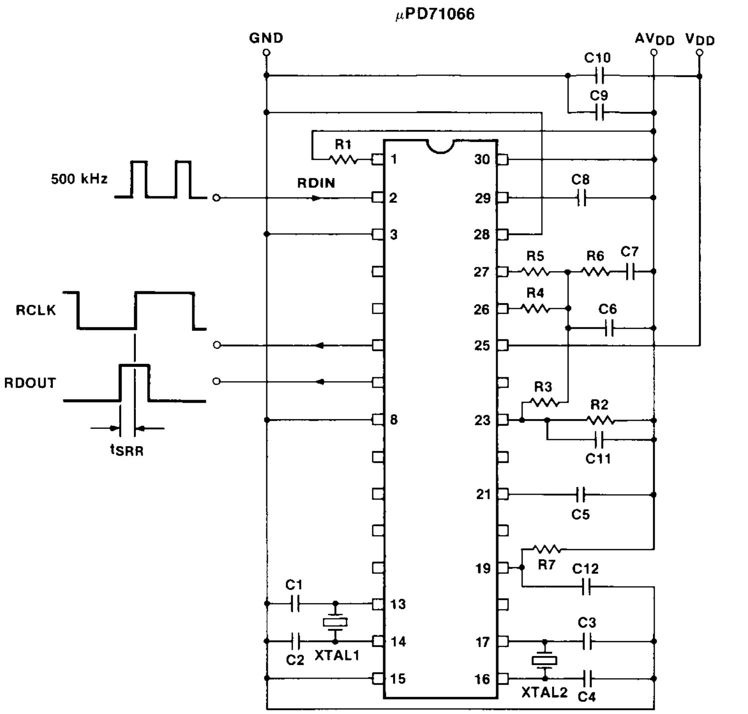
Figure 6. Test Circuit 4



C1	22 pF	R1	3 kΩ	XTAL1	16 MHz
C2	22 pF	R2	27 kΩ	XTAL2	19.2 MHz
C3	22 pF	R3	10 kΩ		
C4	22 pF	R4	1 kΩ		
C5	10 pF	R5	7.5 kΩ		
C6	1800 pF	R6	560 Ω		
C7	22,000 pF	R7	33 kΩ min		
C8	33 pF				
C9	10,000 pF				
C10	10,000 pF				
C11	120 pF				
C12	1 μF				

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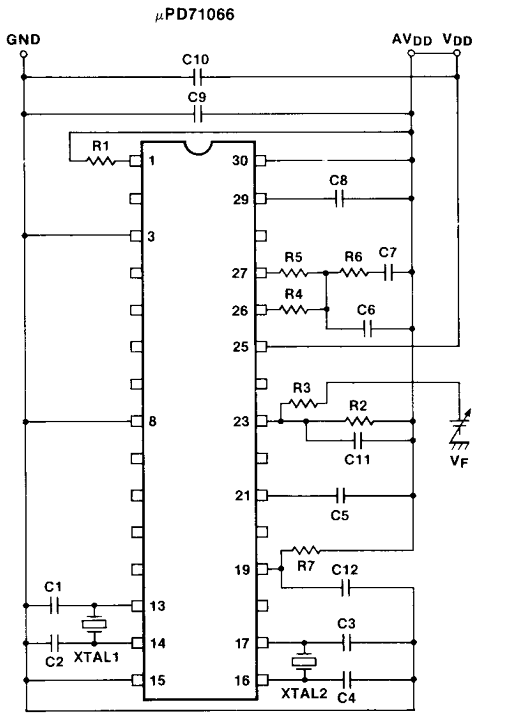
Figure 7. Test Circuit 5



$f_X = 8f_{RCLK}$

C1	22 pF	R1	3 kΩ	XTAL1	16 MHz
C2	22 pF	R2	27 kΩ	XTAL2	19.2 MHz
C3	22 pF	R3	10 kΩ		
C4	22 pF	R4	1 kΩ		
C5	10 pF	R5	7.5 kΩ		
C6	1800 pF	R6	560 Ω		
C7	22,000 pF	R7	33 kΩ min		
C8	33 pF				
C9	10,000 pF				
C10	10,000 pF				
C11	120 pF				
C12	1 μF				

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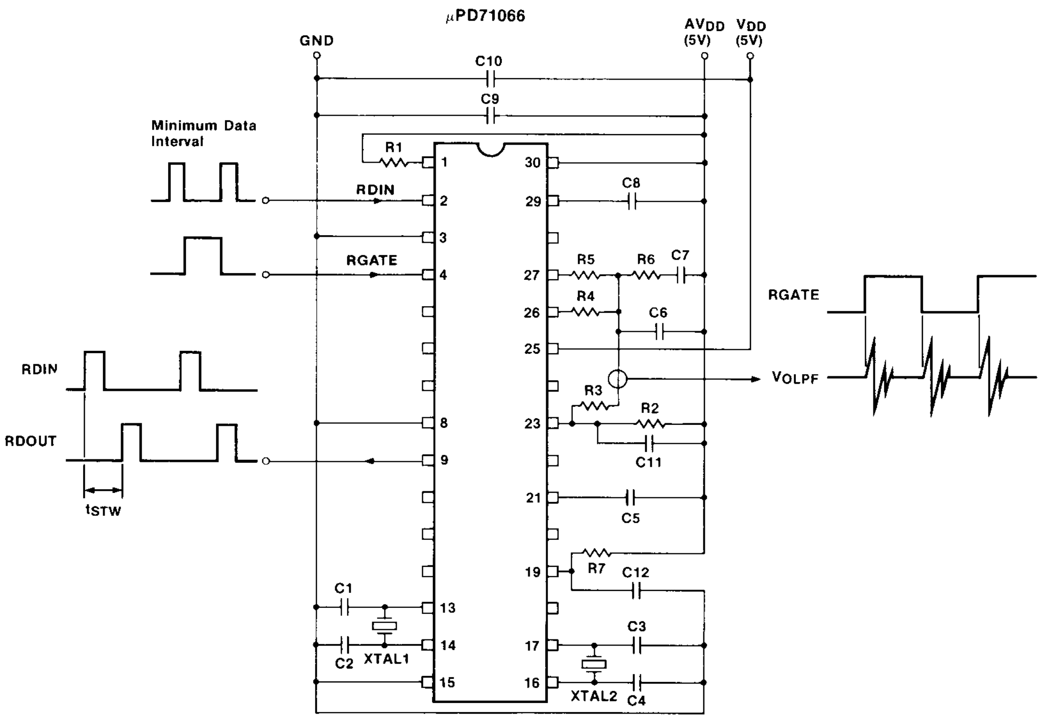
Figure 8. Test Circuit 6



$$f = \frac{1}{400 \times (\text{Min Data Interval})}$$

Duty = 50%

C1	22 pF	R1	3 kΩ	XTAL1	16 MHz
C2	22 pF	R2	27 kΩ	XTAL2	19.2 MHz
C3	22 pF	R3	10 kΩ		
C4	22 pF	R4	1 kΩ		
C5	10 pF	R5	7.5 kΩ		
C6	1800 pF	R6	560 Ω		
C7	22,000 pF	R7	33 kΩ min		
C8	33 pF				
C9	10,000 pF				
C10	10,000 pF				
C11	120 pF				
C12	1 μF				

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System Configurations

Figures 9 through 23 are system configuration examples of the μPD71065 and μPD71066 with various floppy-disk controllers and data transfer rates. See table 2.

For additional details and the values of resistors and capacitors, see figure 1.

Table 2. System Configuration Examples

Floppy-Disk Interface	Floppy-Disk Controllers	Data Transfer Rates (kb/s)	Figure
μPD71065	μPD765A, μPD7265, μPD72065, μPD72066	500/250/125	9
		300/150	10
		500/250/125 and 300/150	11
	μPD7260	500/250/125	12
		300/150	13
		500/250/125 and 300/150	14
μPD71066	μPD765A, μPD7265, μPD72065, μPD72066	500/250/125	15
		300/150	16
		500/250/125 and 300/150	17
	μPD7260	500/250/125	18
		300/150	19
		500/250/125 and 300/150	20
	FD179X	500/250/125	21
		300/150	22
		500/250/125 and 300/150	23

Figure 9. System Example 1: μPD71065 FDI and μPD765A FDC

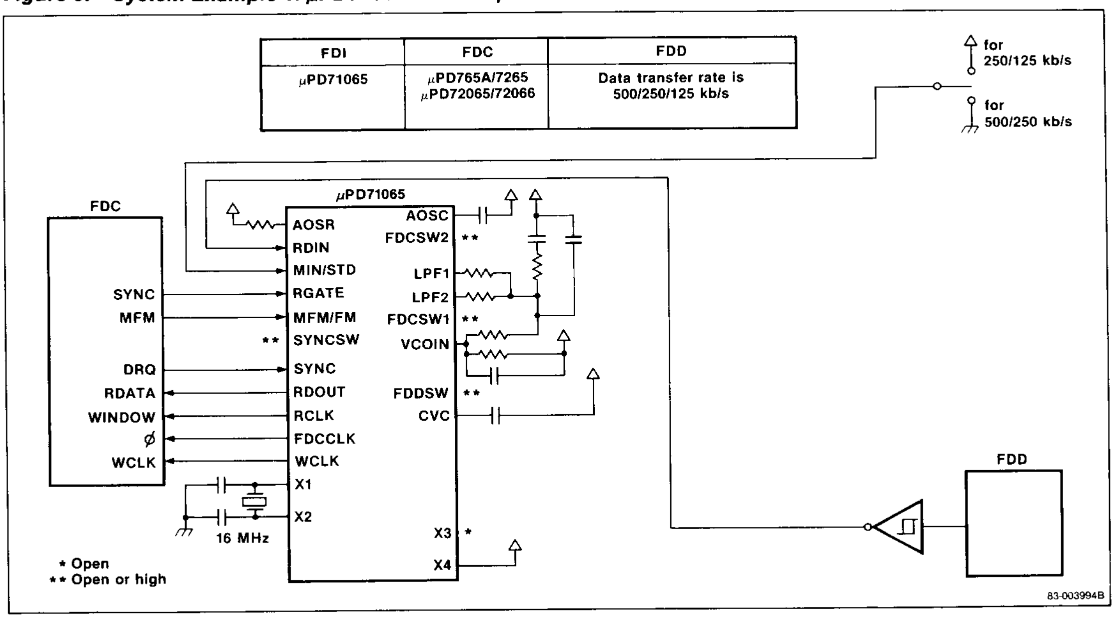

Figure 10. System Example 2: μPD71065 FDI and μPD765A FDC

FDI	FDC	FDD
μPD71065	μPD765A/7265 μPD72065/72066	Data transfer rate is 300/150 kb/s

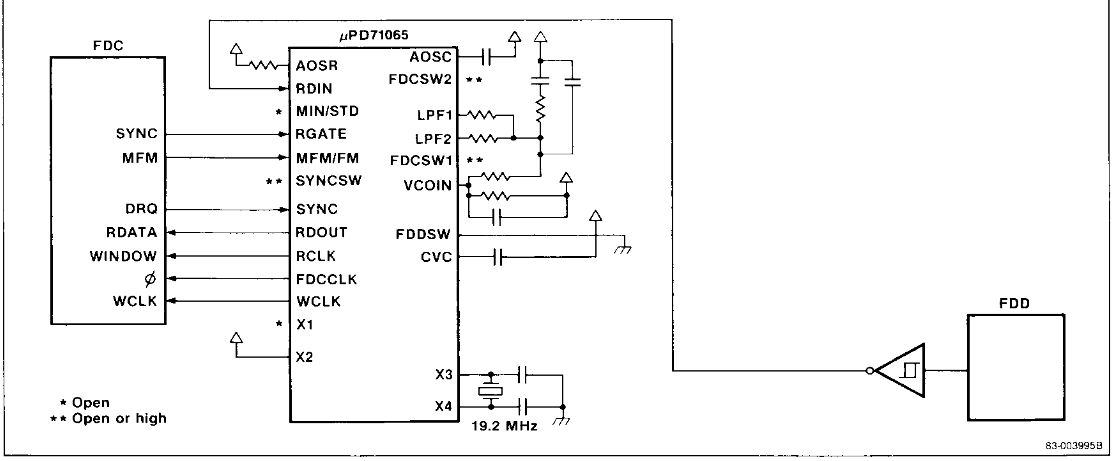

Figure 11. System Example 3: μPD71065 FDI and μPD765A FDC

FDI	FDC	FDD
μPD71065	μPD765A/7265 μPD72065/72066	Data transfer rates are both 500/250/125 kb/s & 300/150 kb/s

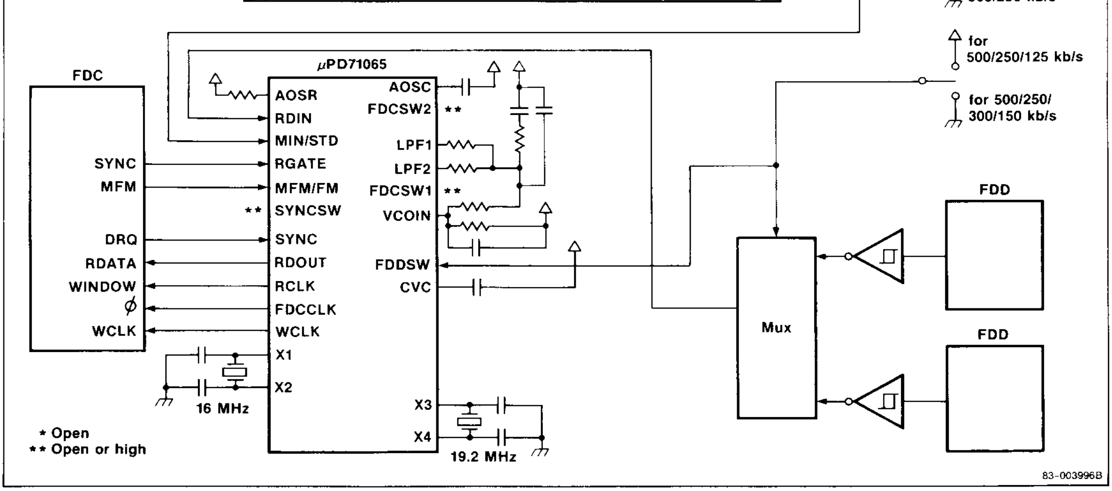

Figure 12. System Example 4: μPD71065 FDI and μPD7260 FDC

FDI	FDC	FDD
μPD71065	μPD7260	Data transfer rate is 500/250/125 kb/s

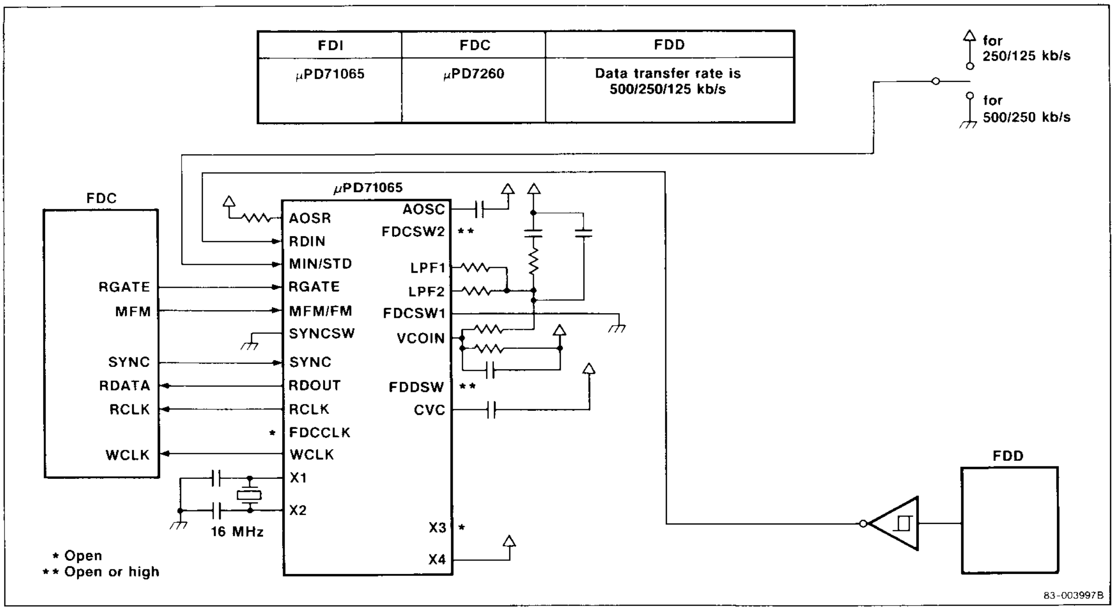

Figure 13. System Example 5: μPD71065 FDI and μPD7260 FDC

FDI	FDC	FDD
μPD71065	μPD7260	Data transfer rate is 300/150 kb/s

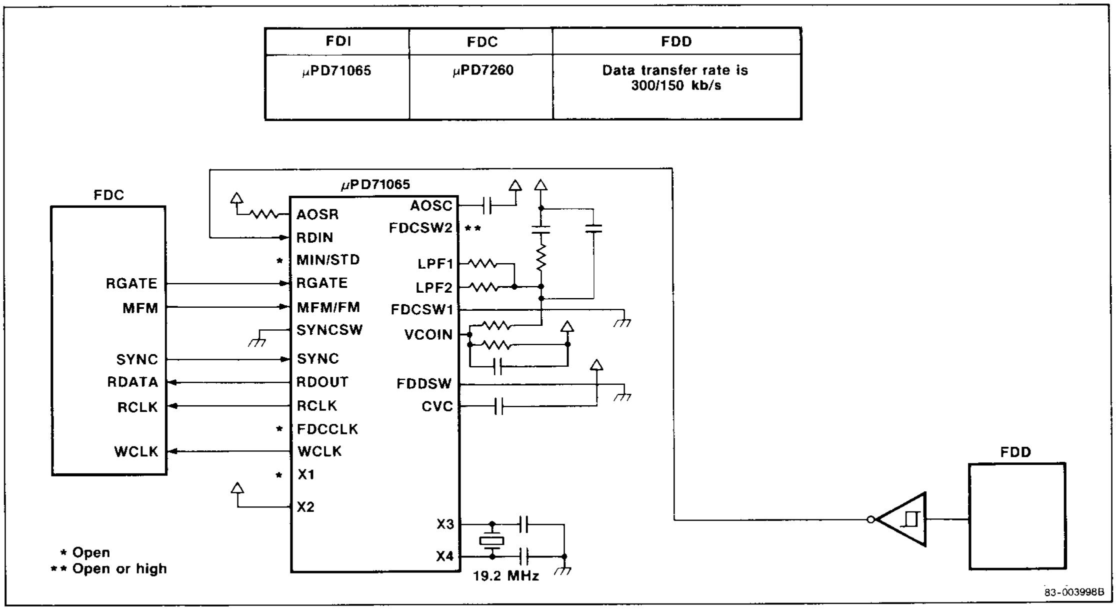

Figure 14. System Example 6: μPD71065 FDI and μPD7260 FDC

FDI	FDC	FDD
μPD71065	μPD7260	Data transfer rates are both 500/250/125 kb/s & 300/150 kb/s

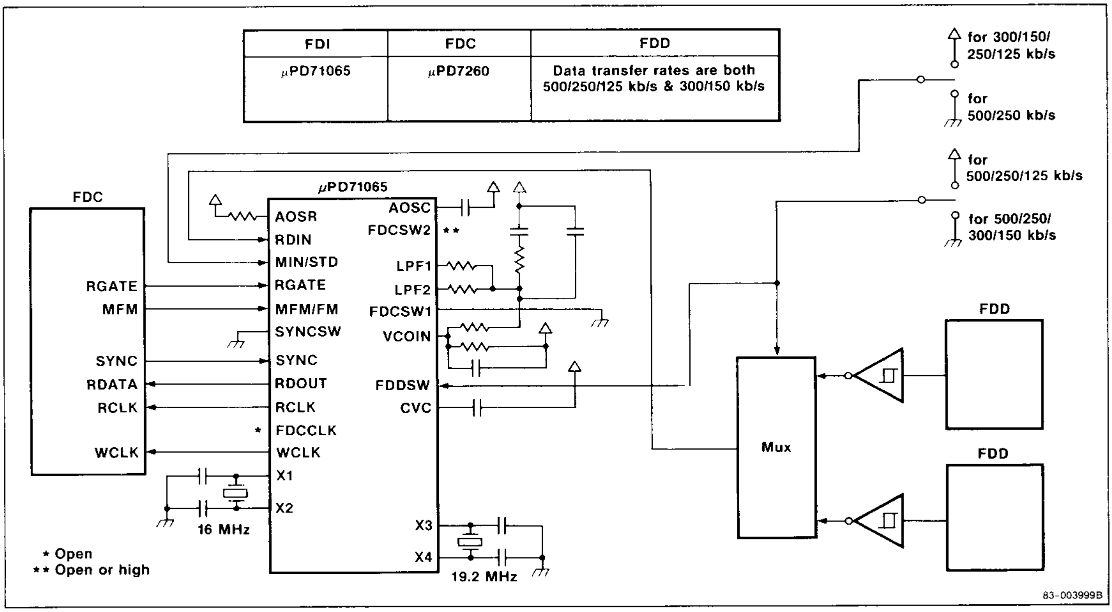

Figure 15. System Example 7: μPD71066 FDI and μPD765A FDC

FDI	FDC	FDD
μPD71066	μPD765A/7265 μPD72065/72066	Data transfer rate is 500/250/125 kb/s

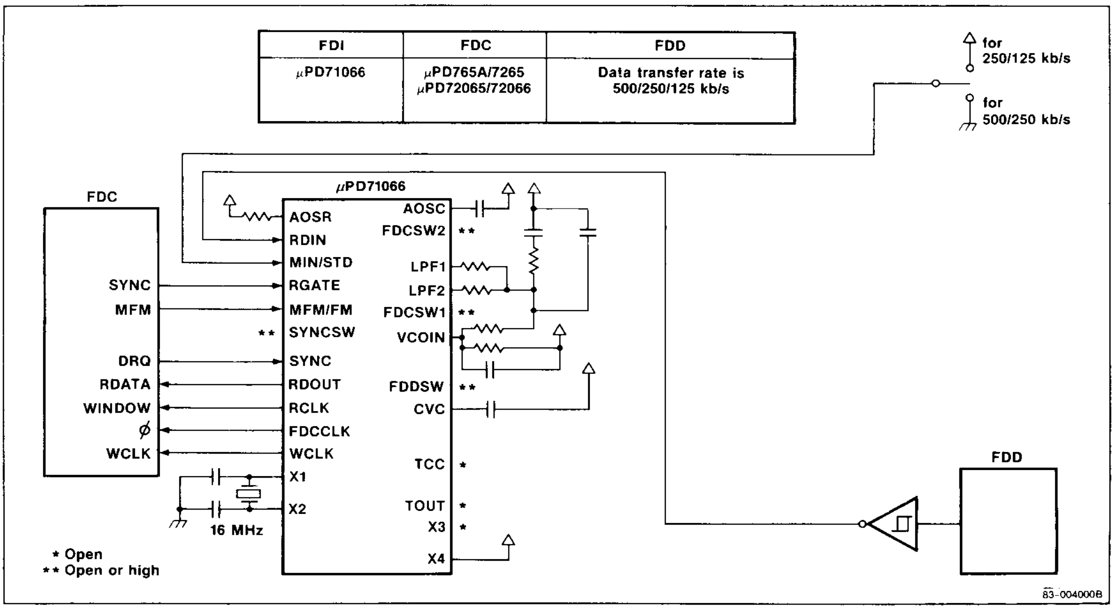

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Figure 16. System Example 8: μPD71066 FDI and μPD765A FDC

FDI	FDC	FDD
μPD71066	μPD765A/7265 μPD72065/72066	Data transfer rate is 300/150 kb/s

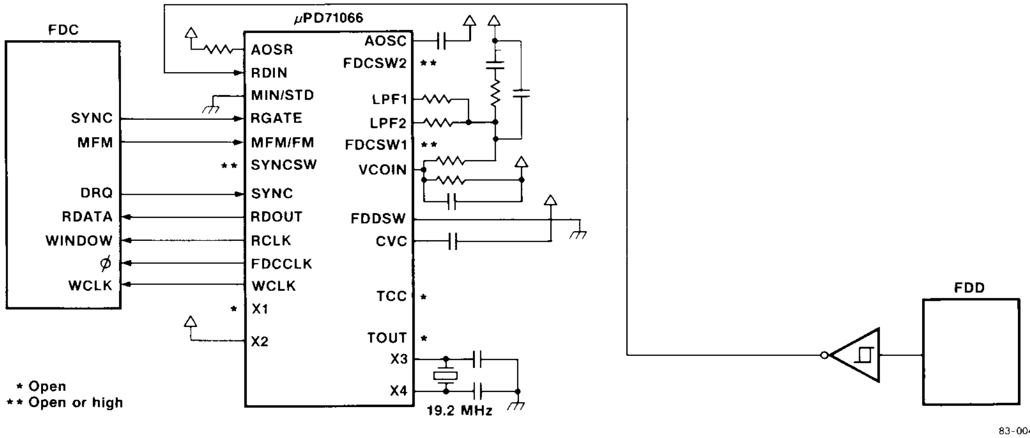

Figure 17. System Example 9: μPD71066 FDI and μPD765A FDC

FDI	FDC	FDD
μPD71066	μPD765A/7265 μPD72065/72066	Data transfer rates are both 500/250/125 kb/s & 300/150 kb/s

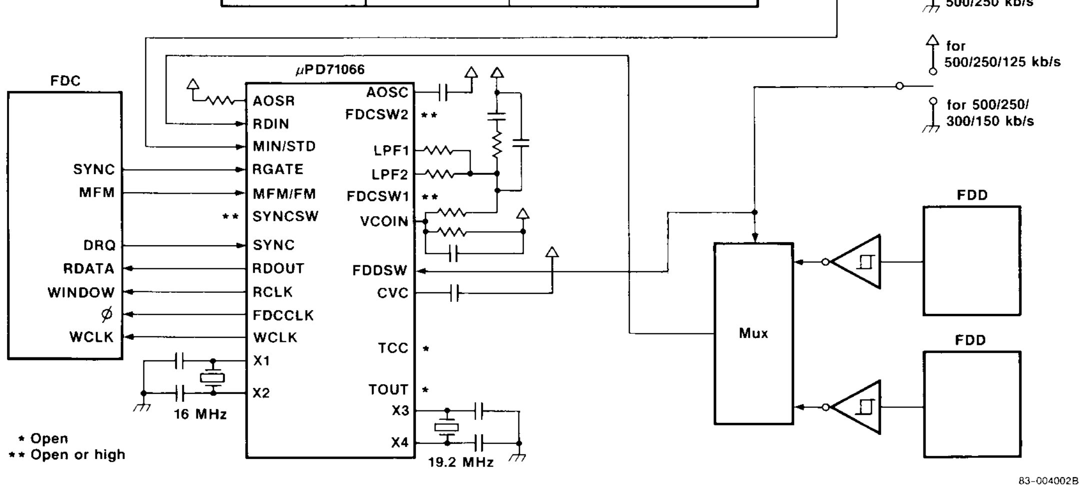

Figure 18. **System Example 10: μPD71066 FDI and μPD7260 FDC**

FDI	FDC	FDD
μPD71066	μPD7260	Data transfer rate is 500/250/125 kb/s

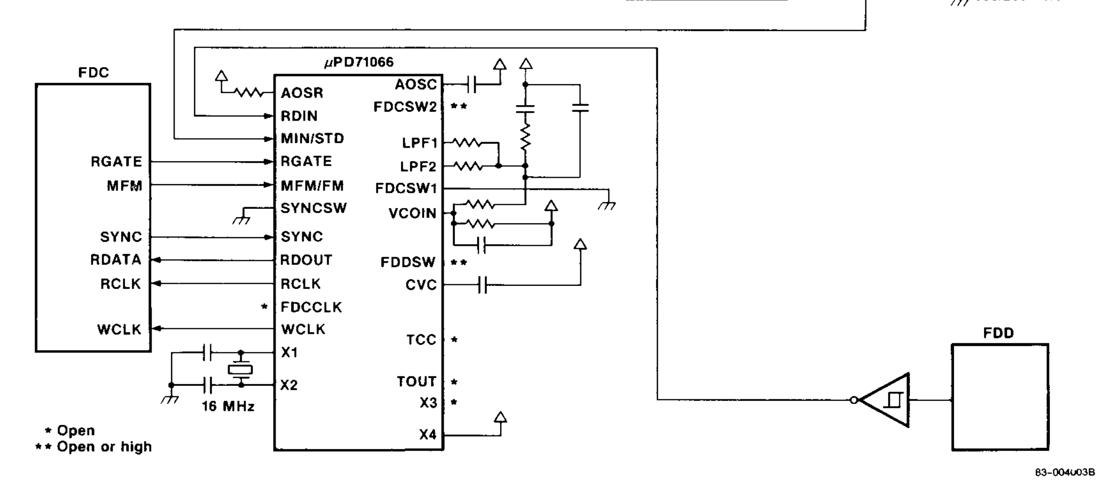

Figure 19. **System Example 11: μPD71066 FDI and μPD7260 FDC**

FDI	FDC	FDD
μPD71066	μPD7260	Data transfer rate is 300/150 kb/s

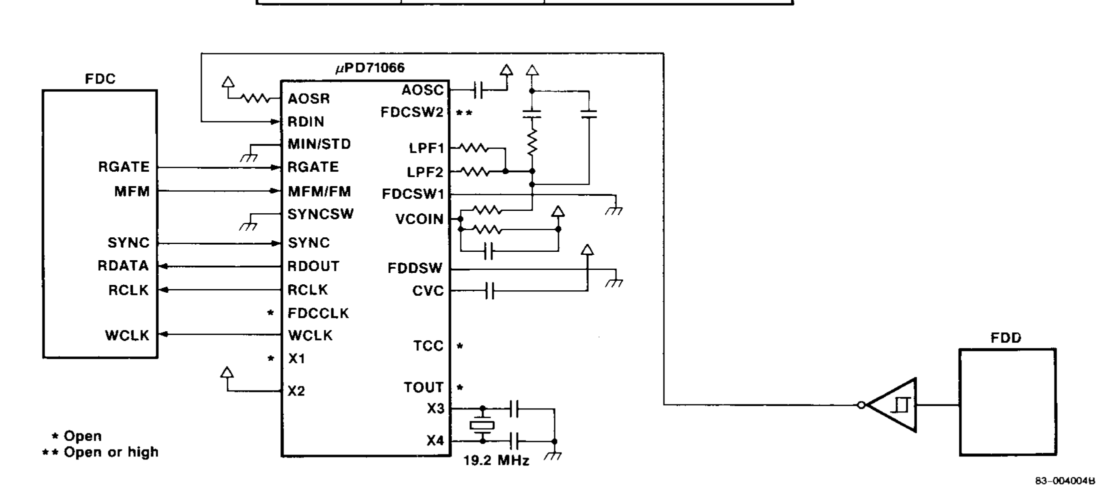

Figure 20. System Example 12: µPD71066 FDI and µPD7260 FDC

FDI	FDC	FDD
µPD71066	µPD7260	Data transfer rates are both 500/250/125 kb/s & 300/150 kb/s

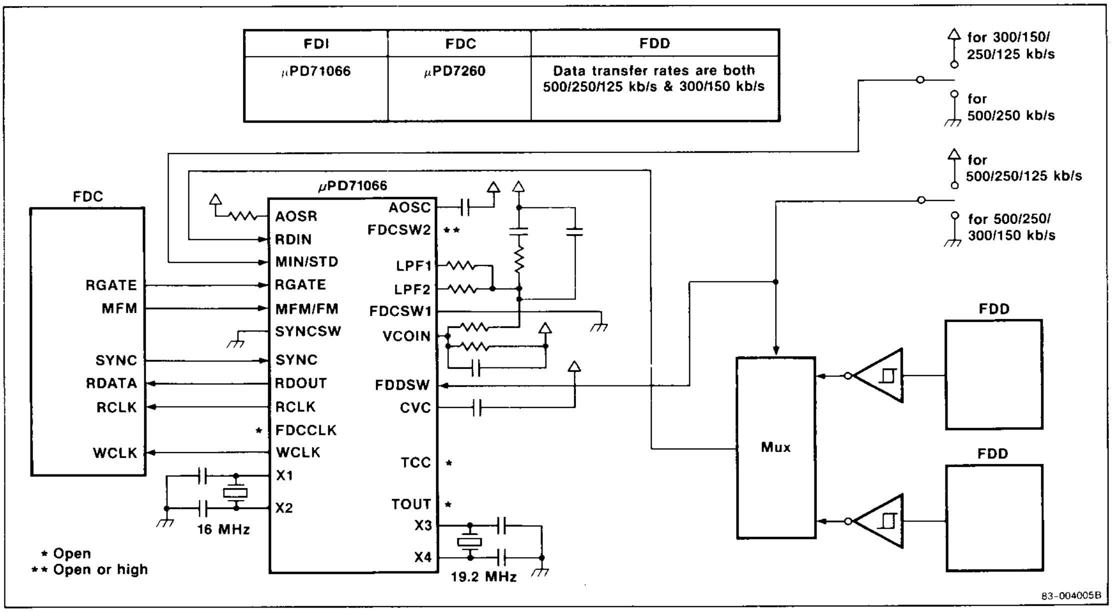

Figure 21. System Example 13: µPD71066 FDI and FD179X FDC

FDI	FDC	FDD
µPD71066	FD179X series	Data transfer rate is 500/250/125 kb/s

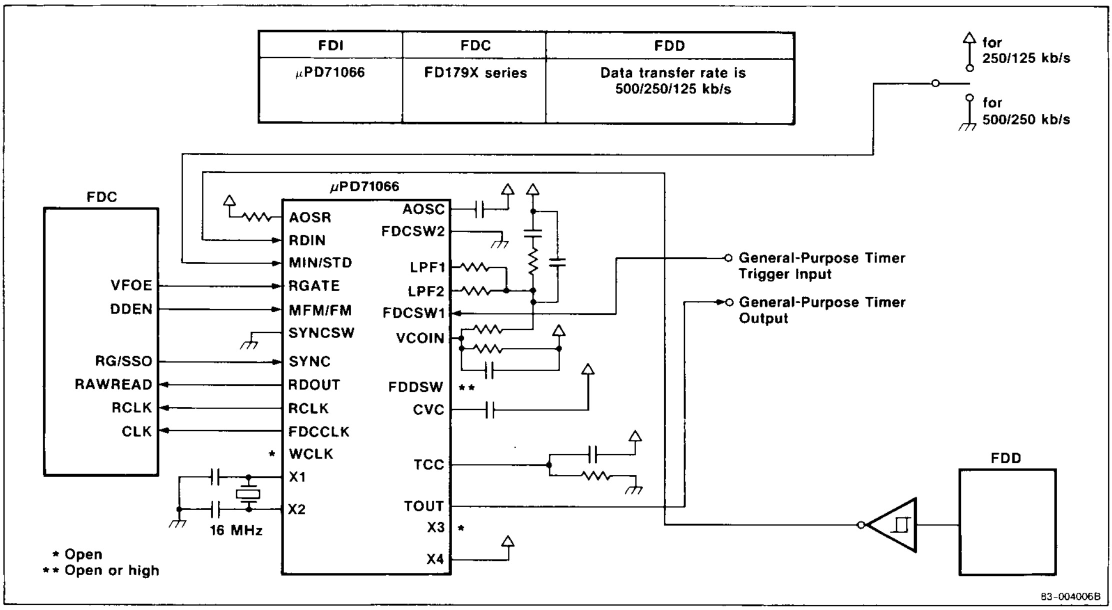

Figure 22. System Example 14: μPD71066 FDI and FD179X FDC

FDI	FDC	FDD
μPD71066	FD179X series	Data transfer rate is 300/150 kb/s

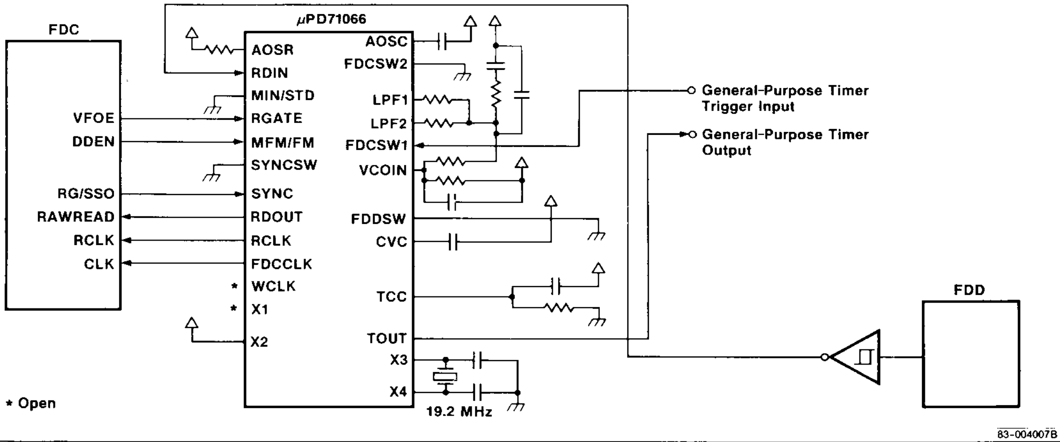

Figure 23. System Example 15: μPD71066 FDI and FD179X FDC

FDI	FDC	FDD
μPD71066	FD179X series	Data transfer rates are both 500/250/125 kb/s & 300/150 kb/s