M51994P,FP

2-OUTPUT TYPE SWITCHING REGULATOR CONTROL

DESCRIPTION

M51994 is a semiconductor integrated circuit designed for controlling primary-control two-output switching regulators and it is best suitable for obtaining DC stabilized voltage from the commercial power supply.

This provides fast rise/fall time of the output voltage as well as output current, allowing the direct driving of the MOSFET.

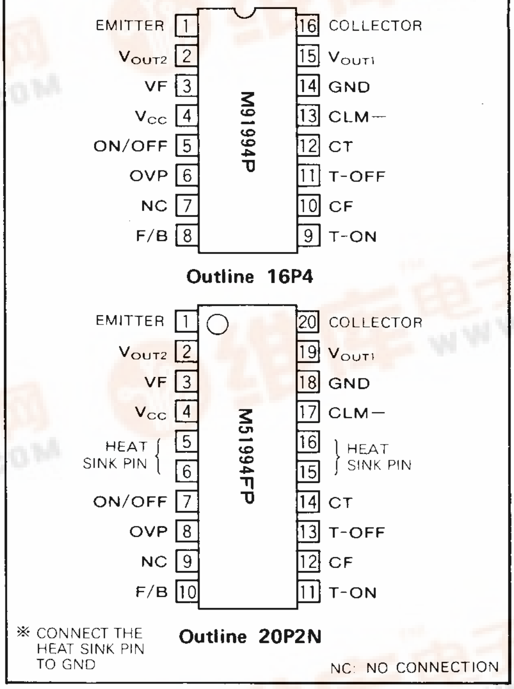
This also provides fast rise/fall time on output pulses and it equips a high-speed and highly-sensitive current limit circuit, therefore, you can create really high-speed switching regulators using the device.

Since it contains a timer type protection circuit, the protection in case of any excess output current (i.e. due to a short-circuit) can be done easily only by adding few parts to the primary side.

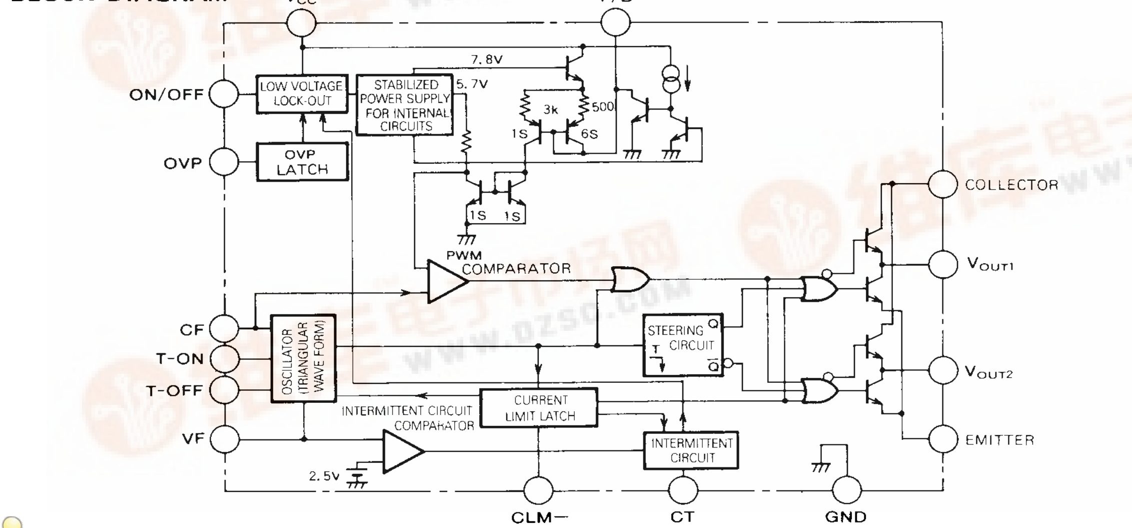
FEATURES

- Output current . . . . ±2A
- Output rise time = 60ns, Output fall time = 40ns
- Small pre-operation current . . . . 110μA (Standard)
- Uses a pulse-by-pulse current limiting method (CLM-pin) which minimizes required peripheral circuits.
- Supports the protection for excess output current . . . . Timer-type protection circuit
- Uses a deforming totempole output method which require small through current.
- Supports 2-output drive functions using a steering circuit. (Applicable for push-pull, half-bridge, and full-bridge circuits)
- Supports the OVP function which keeps the power OFF status once a signal is input.

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



MITSUBISHI ELECTRIC

2-OUTPUT TYPE SWITCHING REGULATOR CONTROL

- Because of the large voltage difference between the start and stop voltages, the smoothing capacity for the input power supply can be minimized.
  .... Start voltage = 16V, Stop voltage = 10V
- Uses a package with the large permissible loss to endure the heat being generated by the gate drive current of the MOS FET ...... 16-pin DIP, 20-pin SOP 1.5W (at 25°C)

APPLICATION

Switching regulators of push-pull, half-bridge, and full-bridge types

RECOMMENDED OPERATING CONDITIONS

Supply voltage range .... 12V to 30V
Operating frequency .... Less than 500kHz

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		31	V
V_{CC}	Collector pin applied voltage		31	V
I_O	Output current	Peak	±2	A
		Continuous	±0.15	
V_{VF}	VF pin supplied voltage		V_{CC}	V
$V_{ON/OFF}$	ON/OFF pin supplied voltage		V_{CC}	V
V_{CLM-}	CLM-pin applied voltage		−4.0～+4.0	V
V_{OVP}	OVP-pin applied voltage		V_{CC}	V
V_{FB}	F/B pin applied voltage		0	V
I_{TON}	T-ON pin output current		−0.5	mA
I_{TOFF}	T-OFF pin output current		−0.5	mA
Pd	Power dissipation	Ta=25℃	1.5	W
K_θ	Thermal derating	Ta≧25℃	12	mW/℃
Topr	Operating temperature		−30～+85	℃
Tstg	Storage temperature		−40～+125	℃
T_j	Junction temperature		150	℃

Note 1: The "+" and "−" signs indicate the direction of the current flow-into and flow-out from the IC lead, respectively.

ELECTRICAL CHARACTERISTICS (Ta=25℃, V_{CC}= 18V, unless otherwise noted)

Symbol		Parameter	Test conditions	Limits Min	Typ	Max	Unit
V_{CC}	Source voltage and circuit current	Supply voltage range				30	V
$V_{CC(START)}$		Start voltage		15.2	16.2	17.2	V
$V_{CC(STOP)}$		Stop voltage		9.0	9.9	10.9	V
$\triangle V_{CC}$		Voltage difference between start and stop voltage	$\triangle V_{CC}=V_{CC(START)}-V_{CC(STOP)}$	5.0	6.3	7.6	V
I_{CCL}		Pre-operation circuit current	V_{CC}=14.5V, Ta=25℃	70	110	165	μA
			V_{CC}=14.5V, −30℃≦Ta≦85℃	55	110	220	μA
I_{CCO}		Operating circuit current	V_{CC}=30V	12.0	18.5	27.0	mA
$I_{CC\ OFF}$		OFF time circuit current	V_{CC}=25V	0.95	1.31	1.9	mA
			V_{CC}=14V	55	110	220	μA
$I_{CC\ CT}$		Circuit current during the Timer OFF	V_{CC}=25V	1.0	1.41	2.1	mA
			V_{CC}=14V	145	230	345	μA
$I_{CC\ OVP}$		Circuit current during OVP operatins	V_{CC}=25V	1.3	2.0	3.0	mA
			V_{CC}=9.5V	125	190	290	μA
$V_{THH\ ON/OFF}$	ON/OFF	ON/OFF pin high threshold voltage		2.1	2.6	3.1	V
$V_{THL\ ON/OFF}$		ON/OFF pin low threshold voltage		1.9	2.4	2.9	V
$\triangle V_{TH\ ON/OFF}$		ON/OFF pin hysterisis voltage		0.1	0.2	0.3	V

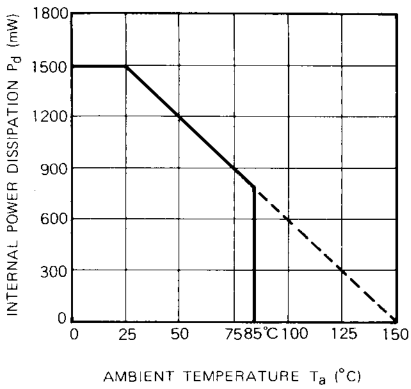
ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{FBMIND}	F/B	Current at 0% duty cycle		−2.1	−1.54	−1.0	mA
I_{FBMAXD}	F/B	Current at maximum duty cycle		−0.90	−0.55	−0.40	mA
$\triangle I_{FB}$	F/B	Current difference between the maximum and 0% duty	$\triangle I_{FB} = I_{FRMIND} - I_{FBMAXD}$	−1.35	−0.99	−0.70	mA
V_{FB}	F/B	F/B pin voltage	F/B pin current = −0.95mA	4.9	5.9	7.1	V
R_{FB}	F/B	F/B pin resistance			600		Ω
I_{FBDIS}	F/B	F/B pin discharge current	$V_{CC}=5V$, $V_{F/B}=1V$	1	3		mA
V_{THOVP}	OVP	OVP pin threshold voltage		1.00	1.40	1.80	V
I_{INOVP}	OVP	OVP pin input voltage			1.2	3.6	μA
V_{CCOVPC}	OVP	OVP cancel source voltage		7.6	8.6	9.6	V
$V_{CC(STOP)} - V_{CCOVPC}$	OVP	Voltage difference between the stop voltage and the OVP cancel source voltage		0.65	1.30		V
I_{TIMER}	Timer	Timer frequency		0.47	0.71	1.07	Hz
I_{TIMECH}	Timer	Timer charge current	$V_{CT}=3.3V$, $Ta=-5℃$	−382	−273	−202	μA
			$V_{CT}=3.3V$, $Ta=25℃$	−358	−256	−190	μA
			$V_{CT}=3.3V$, $Ta=85℃$	−311	−222	−164	μA
$TIME_{OFF/ON}$	Timer	Ratio between ON and OFF times		7.63	9.54	11.9	—
V_{THCLM-}	CLM−	CLM pin threshold voltage	$-5℃ \leqq Ta \leqq 85℃$	−220	−200	−180	mV
I_{INCLM-}	CLM−	CLM pin output current	$V_{CLM}=-0.1V$	−205	−150	−110	μA
T_{DDCLM-}	CLM−	CLM pin delay time			170		ns
f_{OSC}	Oscillator	Oscillation frequency	$R_{ON}=36k\Omega$, $R_{OFF}=12k\Omega$	173	191	210	kHz
T_{DUTY}	Oscillator	Maximum ON duty	$C_F=220pF$, $-5℃ \leqq Ta \leqq 85℃$	85.0	89.0	93.0	%
V_{OSCH}	Oscillator	Upper limit voltage for oscillation wave forms		3.97	4.37	4.77	V
V_{OSCL}	Oscillator	Lower limit voltage for oscillation wave forms		1.76	1.96	2.16	V
$\triangle V_{OSC}$	Oscillator	Voltage difference between upper and lower oscillation wave forms		2.11	2.41	2.71	V
f_{OSCVF}	VF	Oscillation frequency during CLM operations, $V_F=4.5V$	$R_{ON}=36k\Omega$, $R_{OFF}=12k\Omega$	173	191	210	kHz
		Oscillation frequency during CLM operations, $V_F=1.5V$	$C_F=220pF$	144	166	191	kHz
T_{VFDUTY}	VF	Duty ratio during CLM operations, $V_F=0.2V$	Maximum ON duty/Minimum OFF duty	5.8	6.25	8.0	—
V_{THTIME}	VF	VF voltage for starting timer operation		2.25	2.5	2.75	V
I_{VF}	VF	VF pin input current	Output current		2	6	μA
V_{OL1}	Output	Output low voltage	$V_{CC}=18V$, $I_O=10mA$		0.05	0.4	V
V_{OL2}	Output	Output low voltage	$V_{CC}=18V$, $I_O=100mA$		0.7	1.4	V
V_{OL3}	Output	Output low voltage	$V_{CC}=5V$, $I_O=1mA$		0.69	1.0	V
V_{OL4}	Output	Output low voltage	$V_{CC}=5V$, $I_O=100mA$		1.3	2.0	V
V_{OH1}	Output	Output high voltage	$V_{CC}=18V$, $I_O=-10mA$	16.0	16.5		V
V_{OH2}	Output	Output high voltage	$V_{CC}=18V$, $I_O=-100mA$	15.5	16.0		V
T_{RISE}	Output	Output voltage rise time	Without load		50		ns
T_{FALL}	Output	Output voltage fall time	Without load		35		ns

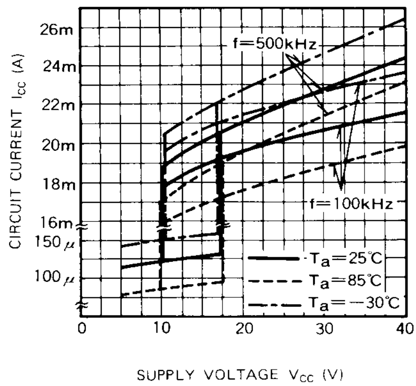
* :Output 1 and 2 will become HIGH at a duty specified per cycle. (They never become HIGH at the same time.)

TYPICAL CHARACTERISTICS

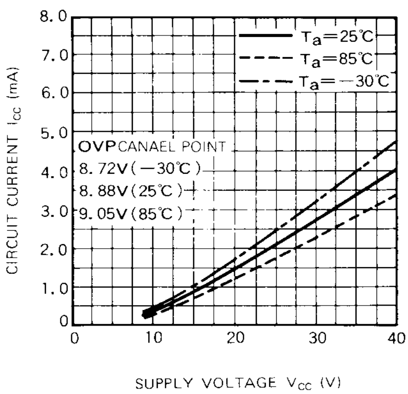
THERMAL DERATING (MAXIMUM RATING)



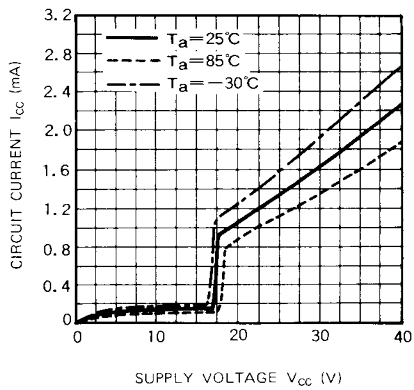
CIRCUIT CURRENT VS. SUPPLY VOLTAGE (NORMAL OPERATION)



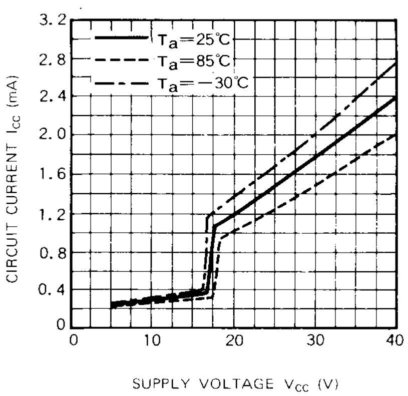
CIRCUIT CURRENT VS. SUPPLY VOLTAGE (OVP STATE)



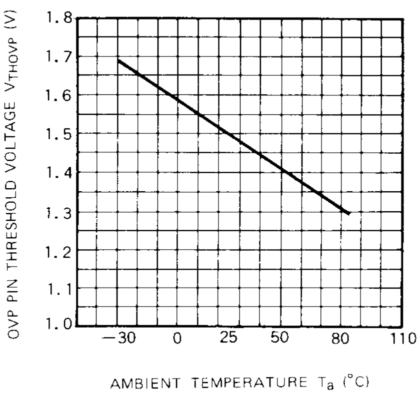
CIRCUIT CURRENT VS. SUPPLY VOLTAGE (OFF STATE)



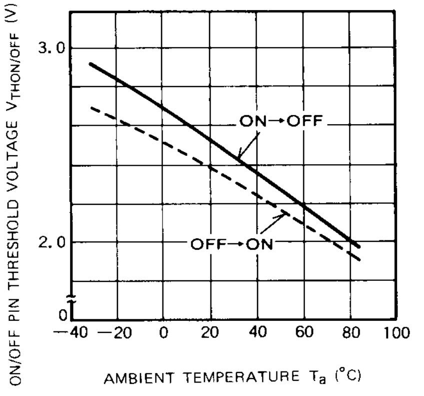
CIRCUIT CURRENT VS. SUPPLY VOLTAGE (TIMER OFF STATE)



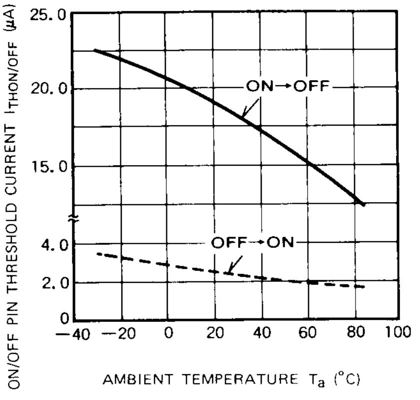
OVP PIN THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE



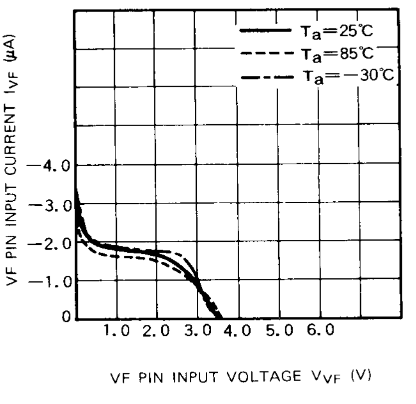
ON/OFF PIN THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE



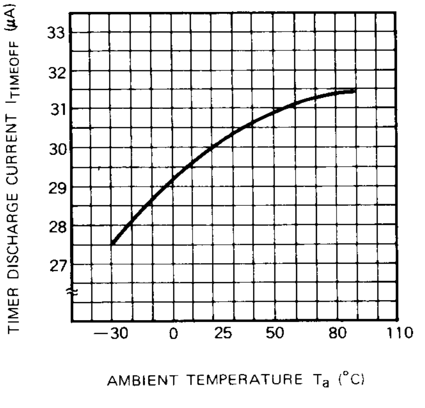
ON/OFF PIN THRESHOLD CURRENT VS. AMBIENT TEMPERATURE



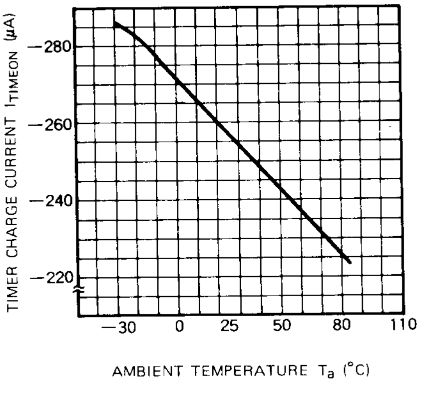
VF PIN INPUT CURRENT VS. INPUT VOLTAGE



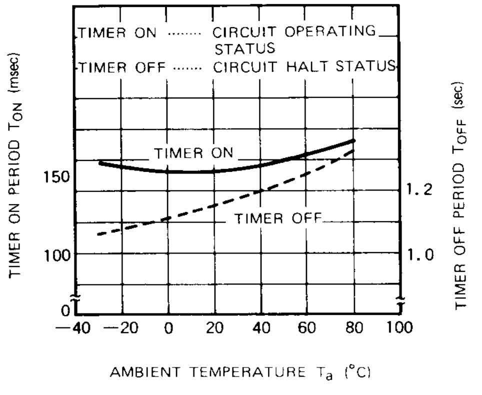
TIMER DISCHARGE CURRENT VS. AMBIENT TEMPERATURE



TIMER CHARGE CURRENT VS. AMBIENT TEMPERATURE

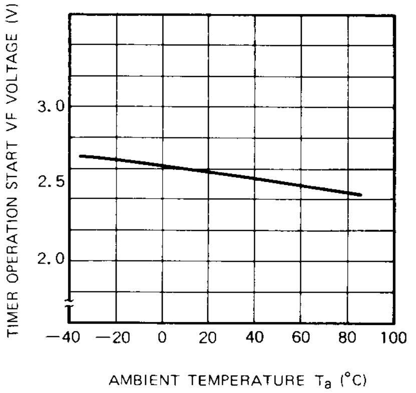


TIMER ON (OFF) PERIOD VS. AMBIENT TEMPERATURE

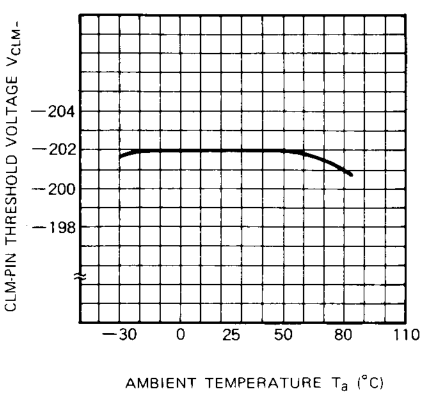


2-OUTPUT TYPE SWITCHING REGULATOR CONTROL

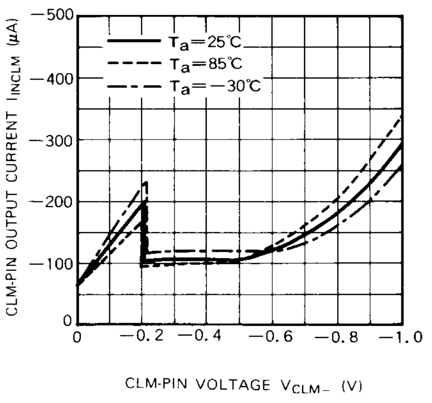
TIMER OPERATION START VF VOLTAGE VS. AMBIENT TEMPERATURE



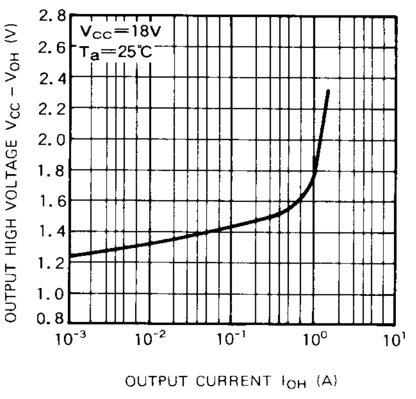
CLM-PIN THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE



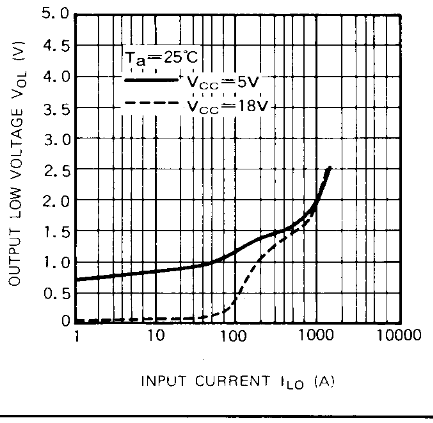
CLM-PIN OUTPUT CURRENT VS. CLM-PIN VOLTAGE



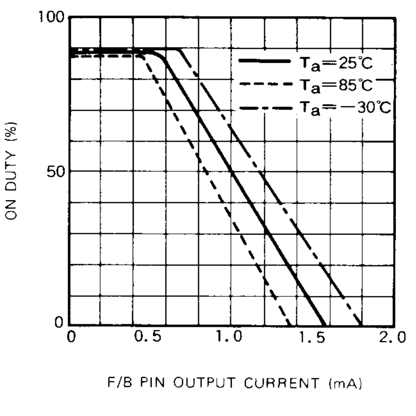
OUTPUT HIGH VOLTAGE VS. OUTPUT CURRENT



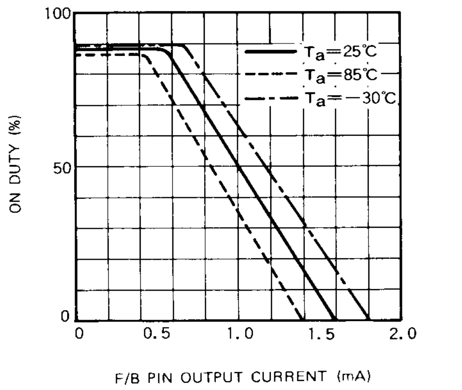
OUTPUT LOW VOLTAGE VS. INPUT CURRENT



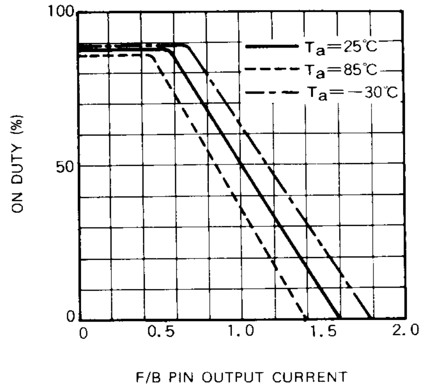
F/B PIN OUTPUT CURRENT VS. ON DUTY (f_{OSC} = 100kHz)



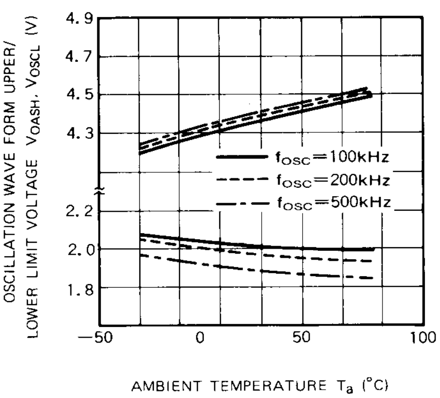
F/B PIN OUTPUT CURRENT VS. ON DUTY (f_{OSC} = 200kHz)



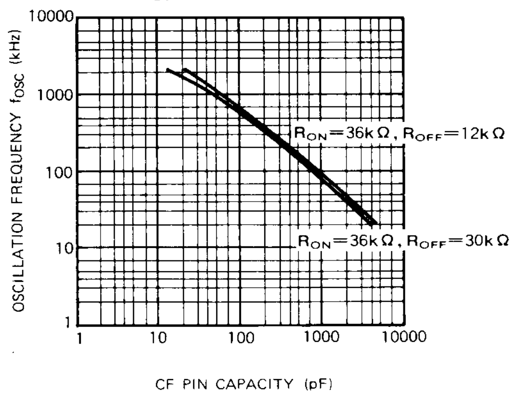
F/B PIN OUTPUT CURRENT VS. ON DUTY (f_{OSC} = 500kHz)



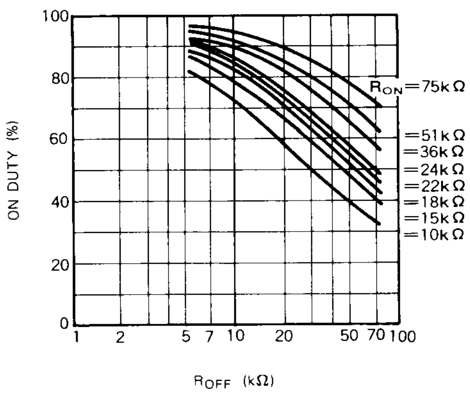
OSCILLATION WAVE FORM UPPER/LOWER LIMIT VOLTAGE VS. AMBIENT TEMPERATURE



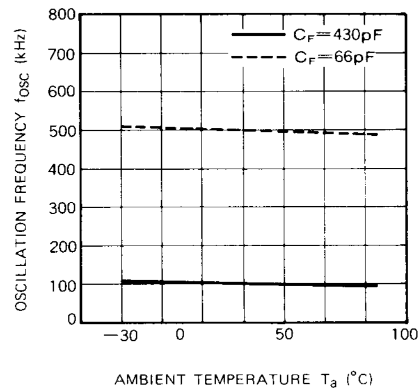
OSCILLATION FREQUENCY VS. CF PIN CAPACITY



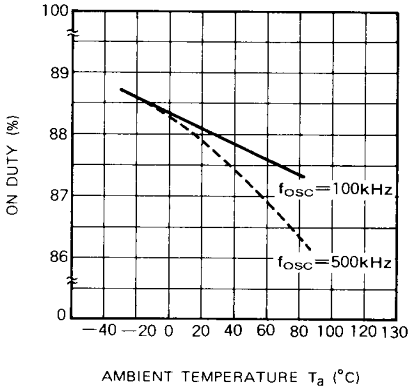
ON DUTY VS. R_{OFF}



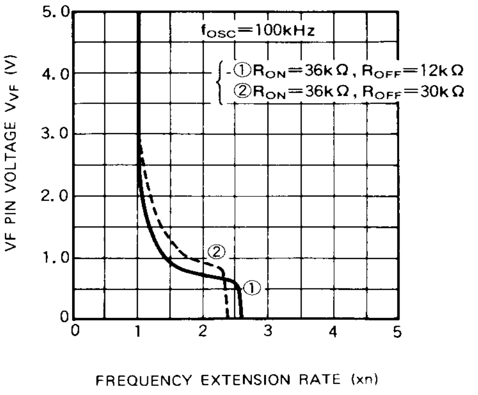
OSCILLATION FREQUENCY VS. AMBIENT TEMPERATURE



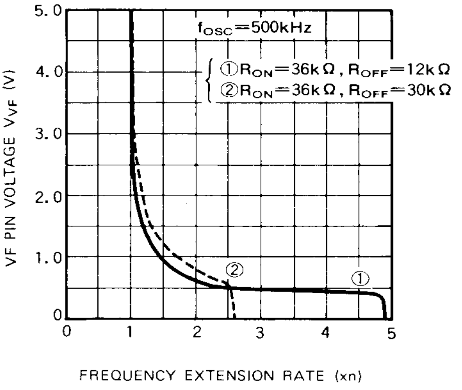
ON DUTY VS. AMBIENT TEMPERATURE



VF PIN VOLTAGE VS. FREQUENCY



VF PIN VOLTAGE VS. FREQUENCY



DESCRIPTIONS OF OPERATIONS

1. Oscillation Circuit

The oscillation wave form of M51994 is triangular. The output is enabled (disabled = dead time) on the leading (trailing) edges. The slope of the leading edge is determined by multiplying the register R_{ON} connected to the T-ON pin and the capacity of C_F connected to the C_F pin. The slope of the trailing edge is determined by multiplying the registers R_{OFF} and C_F connected to the T-OFF pin.

(1) The operation of the oscillation circuit when the SOFT circuit is not working

The figure below shows the charge/discharge control circuit section of the oscillation capacitor C_F.

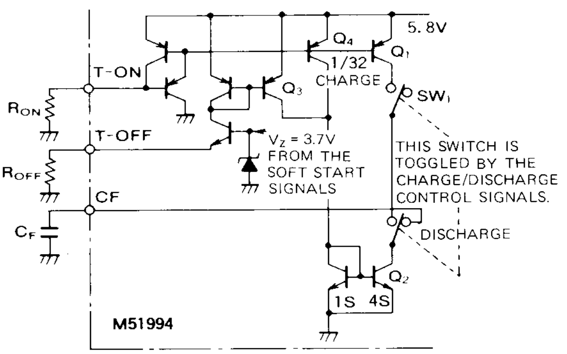


Figure 1 Charge/discharge control circuit of the oscillation capacitor C_F

In the charge status SW_1 and SW_2 become ON and OFF, respectively. In the discharge status SW_1 and SW_2 become OFF and ON, respectively.

When SW_1 is ON and SW_2 is OFF, charge current flows from Q_1 to C_F.

The voltage build-up rate (the rising slope of the oscillation wave form) of C_F is given by the following equation:

$$\simeq \frac{V_{T\text{-}ON}}{R_{ON} \cdot C_F} \text{ (V/sec)} \quad \cdots\cdots (1)$$

Here, $V_{T\text{-}ON}$ (voltage at T-ON pin) is about 4.5V.

Therefore, the rising slope period (that is, the maximum ON period) will be as follows:

$$\frac{(V_{OSCH} - V_{OSCL}) \cdot R_{ON} \cdot C_F}{V_{T\text{-}ON}} \text{ (sec)} \quad \cdots\cdots (2)$$

Here, V_{OSCH} (upper limit voltage of the oscillation wave form) is about 4.4V and V_{OSCL} (lower limit voltage of the oscillation wave form) is about 2.0V.

When SW_1 is OFF and SW_2 is ON, the discharge current flows from C_F to Q_2. The value of this discharge current is calculated by multiplying 4 to the sum of the current through R_{OFF} and 1/32nd of the current through R_{ON}.

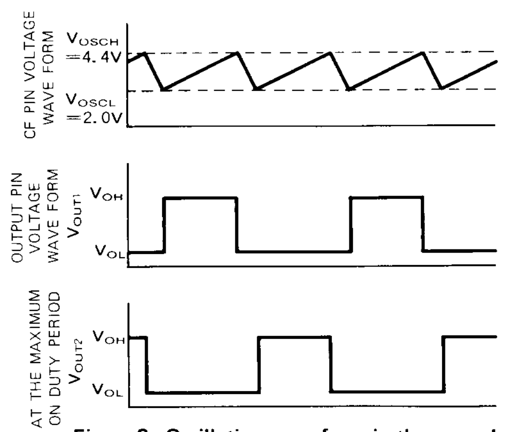


Figure 2 Oscillation wave form in the normal status (when the intermittent action and the oscillation control circuit are not working)

This is given by the following equations:

Falling slope of the oscillation wave form

$$\cong 4\left(\frac{V_{T\text{-}OFF}}{R_{OFF} \cdot C_F} + \frac{V_{T\text{-}ON}}{32 \cdot R_{ON} \cdot C_F}\right) \text{ (V/sec)} \quad \cdots (3)$$

The minimum OFF period

$$\simeq \frac{(V_{OSCH} - V_{OSCL}) \cdot C_F}{4\left(\frac{V_{T\text{-}OFF}}{R_{OFF}} + \frac{}{32 \cdot R_{ON}}\right)} \text{ (sec)} \quad \cdots\cdots (4)$$

Here, $V_{T\text{-}OFF}$ (voltage at T-OFF pin) is about 3.0V. The period of the oscillation wave form is the sum of equations (2) and (4). The oscillation wave form becomes triangular as shown in Figure 2.

(2) The operation of the osicllation circuit when the intermittent action and the control circuit are working

The intermittent action and the oscillation control circuit will be enabled when the current limit circuit (CLM−) works. (See the Intermittent Action and the Oscillation Control Circuit sections.) At the time, the voltage at the T-OFF pin is affected by the voltage applied to the VF pin.

Therefore, under this status, the falling slope of the oscillation wave form is affected by the voltage applied to the VF pin and the dead time will be extended.

The equations below are applied under the above conditions:

The rising slope of the oscillation wave form

$$\frac{V_{T\text{-}ON}}{R_{ON} \cdot C_F} \text{ (V/sec)} \quad \cdots\cdots (5)$$

The falling slope of the oscillation wave form

$$4 \cdot \left(\frac{V_{VF} - V_{VFO}}{R_{OFF} \times C_F} + \frac{V_{T\text{-}ON}}{32 \times R_{ON} \times C_F}\right) \text{ (V/sec)} \quad \cdots\cdots (6)$$

Note V_{VF}: applied voltage at VF pin

$V_{VFO} \simeq 0.4V$

when $V_{VF} - V_{VFO} < 0$, $V_{VF} - V_{VFO} = 0$

when $V_{VF} - V_{VFO} > V_{T\text{-}OFF}, \simeq 3.0V$

$$V_{VF} - V_{VFO} = V_{T\text{-}OFF}$$

(That is, when $V_{VF} > 3.4V$, the status be the same as that when the intermittent action and the oscillation control circuit as not working.)

Therefore, the maximum ON period is the same as that when the intermittent action and the oscillation control circuit are not working and the equation is given as follows:

$$\frac{(V_{OSCH} - V_{OSCL}) \times R_{ON} \times C_F}{V_{T\text{-}ON}} \text{ (sec)} \quad \ldots\ldots\ldots (2)$$

The minimum OFF period is given by the following equation:

$$\frac{(V_{OSCH} - V_{OSCL})}{4\left(\dfrac{V_F - V_{VFO}}{R_{OFF} \times C_F} + \dfrac{V_{T\text{-}ON}}{32 \times R_{ON} \times C_F}\right)} \text{ (sec)} \quad \ldots\ldots (7)$$

Thus, the cycle of the oscillation wave form is given by the sum of equations (2) and (7).

Figure 3 shows the wave form at the time. As shown in Figure 4, the output pulse will not be generated at the first cycle on the output pulse wave form upon the activation. It will be generated from the second cycle. This is because the first C_F pin wave form rises at 0V and the maximum ON time is extended.

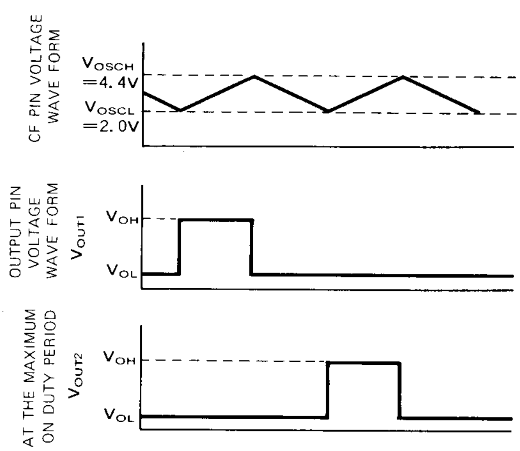
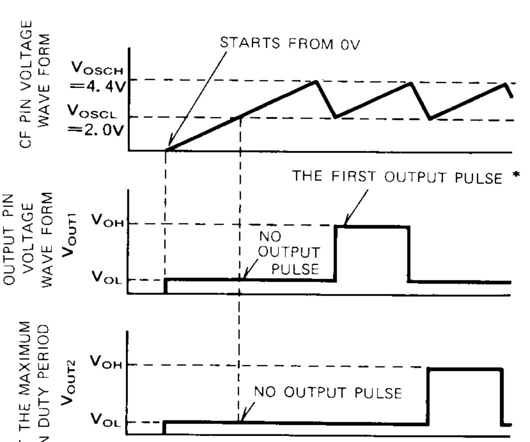


Figure 3 Oscillation wave form when the intermittent action and the oscillation control circuit are working



* IT IS UNSURE THAT THE FIRST OUTPUT PULSE WILL BE SENT TO V_{OUT1} OR V_{OUT2}.

Figure 4 Relation between the oscillation wave form upon the activation and the output wave form

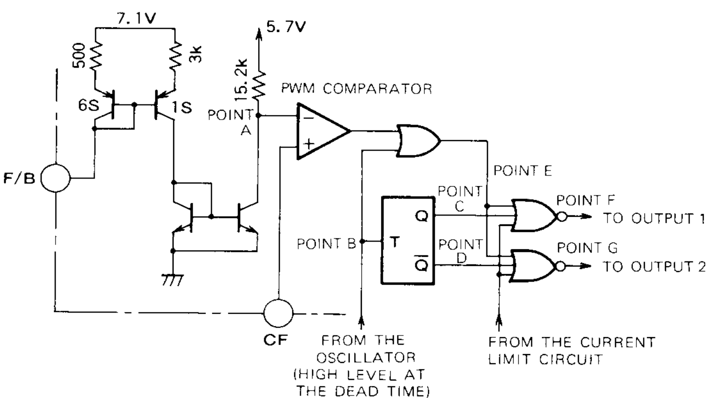


Figure 5 PWM comparator and steering circuit sections

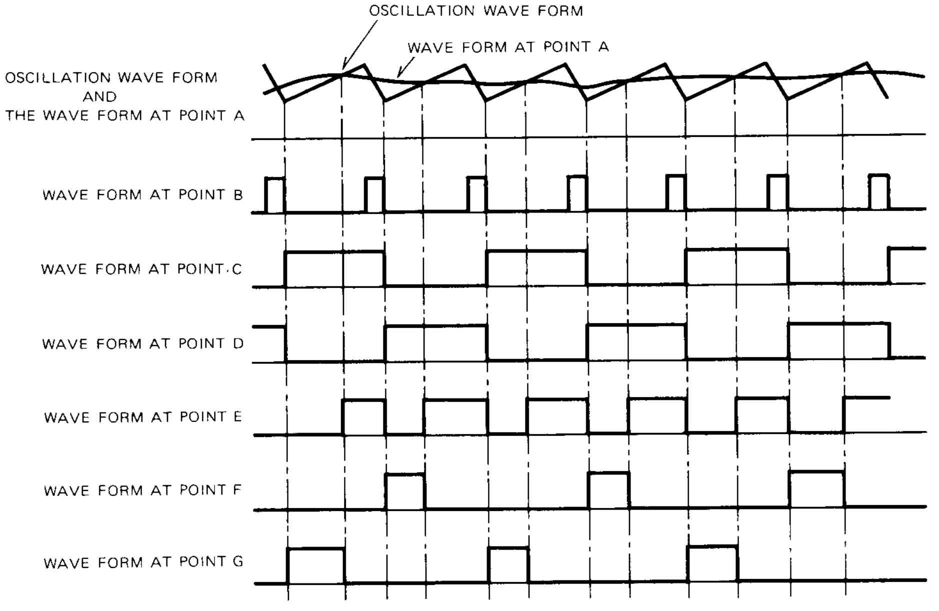


Figure 6 Wave forms at each point of the PWM comparator and the steering circuit

2. PWM comparator and steering circuit sections

Figure 5 shows the circuit diagram of the PWM comparator and the steering circuit in this IC. If there is no output current from the F/B pin, the output pulse width will agree with the voltage build-up period of the CF pin oscillation wave form.

If the value of the resistance for the F/B pin connection (F/B pin output current) is finite and any current is output from the F/B pin, the electric potential at the point A in Figure 5 will change depending on the current. The current becomes higher, the electric potential at point A is compared with the oscillation wave form of the CF pin by the PWM comparator. If the level of the oscillation wave form is higher than the electric potential at point A, the output of the PWM comparator becomes the HIGH level. The final output drive wave form (point F and point G) is obtained by calculating the logical OR of the ORed signals (point E) of dead time signals from the oscillator and the steering circuit output signals (points C and D). (See Figure 6)

3. Current limit circuit

If the current limit signal is input before the voltage at point A in Figure 5 and the CF pin oscillation wave form crosses, the output will be disabled from that time to the next cycle. Figure 7 shows this status.

Even if the current limit circuit is set and no wave form is generated for the output, this status will be reset during the next dead time period.

Therefore, the current limit circuit works in each cycle. This circuit operation is called as the pulse-by-pulse current limit.

Note the current limit detection sensitivity is supported by the temperature compensation.

If you desire the detection is to be done with the voltage less than -200mV, enter the voltage to this pin using the resistance division.

In the example the current is detected using a resistance, you may use a current transformer.

Noise voltage may be generated at R_{CLM} when the transistor is set to ON due to the snubber circuit or the capacity between coils of a transformer. The CLM may malfunctions because of this noise voltage so that noise-cut filters R_{NF} and C_{NF} are connected in the figure.

Set the R_{NF} to any value between 10 to 100Ω where it is not severaly affected by the output current from the CLM-pin (about 200μA). Also, set the C_{NF} to any value where noise can be removed.

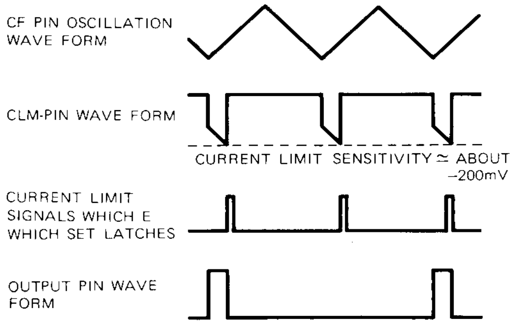


Figure 7 Wave forms of the current limit circuit which describe operations

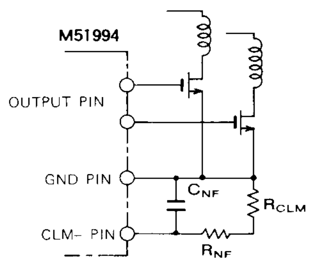


Figure 8 Current limit circuit connection diagram

4. Intermittent Action and Oscillation Control Circuit

When the current limit circuit is activated and the VF voltage becomes below some level, the dead time is extended and the intermittent action circuit (timer type protection circuit) starts working. The intermittent action and oscillation control circuit generates signals for controlling oscillators and intermittent action circuits using current limit signals.

Figure 9 shows the operation time chart for the circuit.

When the output from the intermittent action and oscillation control circuit in the time chart is HIGH level, the oscillation wave form depends on the VF pin voltage and the intermittent action circuit works.

5. Intermittent operation circuit section

Intermittent circuit will start to operate when the output signal from the intermittent and oscillation control circuit are "high" and also V_F terminal voltage is lower than $V_{TH\text{-}TIME}$ of 2.5V. In the application circuit where there is the feed back loop from output terminal to V_F terminal, the circuit will operate in a short time from the instance of output "on".

Fig.10 shows the block diagram of intermittent operation circuit. Transistor Q is onstate when V_F terminal voltage is higher than $V_{TH\text{-}TIME}$ of 2.5V, so the C_T terminal voltage is near to GND potential.

When V_F terminal voltage is lower than $V_{TH\text{-}TIME}$, Q becomes "off" and the C_T has the possibility to be charged up.

Under this condition, if the intermittent and oscillation control signal become "high", the switch SWA will close only in this "high" duration and C_T is charged up by the current of 250μA through SWA (SWB)is open) and C_T terminal potential will rise. The output pulse can be generated only in this duration.

When the C_T terminal voltage reaches to 8V, the control logic circuit makes the SWA "off" and SWB "on", in order to flowout the $I_{TIME\text{-}DIs}$ of 30μA from C_T terminal.

The IC operation will be ceased in the falling duration.

On the other hand, when C_T terminal voltage decreasea to lower than 2V, the IC operation will be reset to original state, as the control logic circuit makes the SWA "on" and SWB "off".

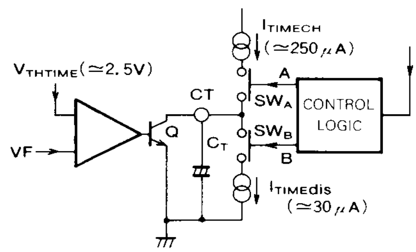
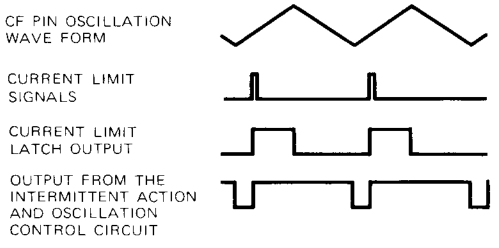
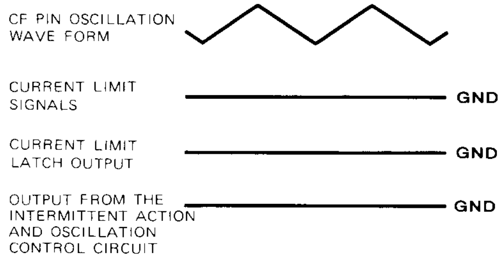


Fig.10 Block diagram of intermittent circuit



(a) When current limit signals are present



(b) When current limit signals are not present

Figure 9 Time chart for the intermittent action and oscillation control circuit

Figure 11 shows the characteristics of the circuit current versus the source voltage. Under this status no current can be obtained from the secondary winding of the transformer so that the circuit current is supplied only from the resistance R_1 connected to the V_{CC} pin of the IC. However, since the circuit current has such characteristics as that shown in Figure 11, if you set the resistance R_1 connected to the V_{CC} (shown in Figure 16) to some proper value, appropriate source voltage will be retained.

Figure 13 shows an application circuit which maintains the non-operating status when excess output loading status has lasted for a specific time.

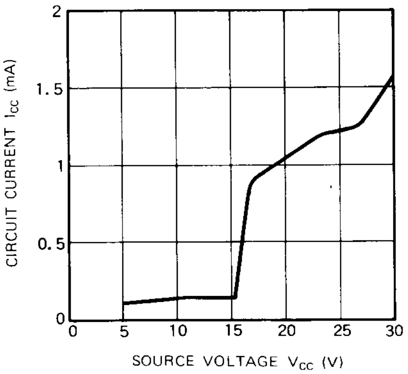


Figure 11 Characteristics of the circuit current versus the source voltage when the intermittent action circuit is not working

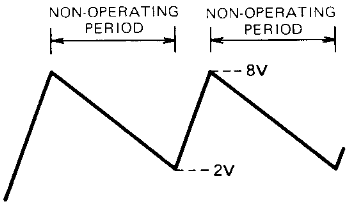


Figure 12 CT pin wave form

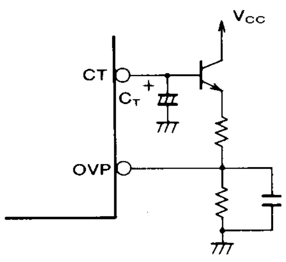


Figure 13 Application circuit which maintains the non-operating status when the excess output loading status has lasted for a specific time

REFERENCE DATA

MOS FET Gate Drive Loss

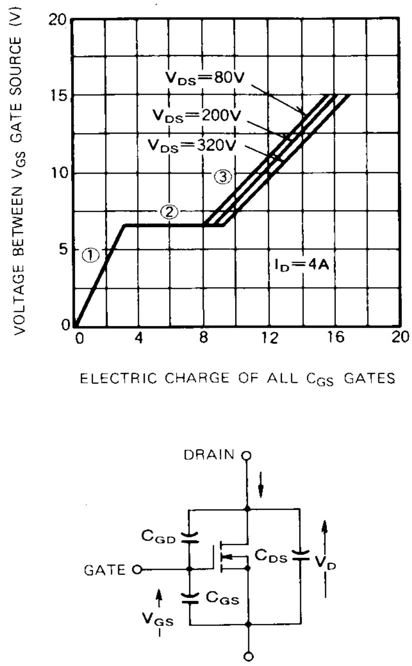


Figure 14 Relations between the voltage to be applied between gate sources and the charge to be accumulated at the time

Figure 14 shows the relation between the voltage to be applied to gates and the electric charge to be accumulated in the gates at the time.

In area ① the transistor is turned off and the drain voltage is high, therefore, the depletion layer is spread out to the drain side and the value of C_{GS} is small so that the charge will be accumulated only in C_{GS}.

In area ② the transistor moves from its OFF status to the ON status and the C_{GD} works as mirror capacity.

In area ③ the transistor turns on, the drain voltage goes low, and both C_{GD} and C_{GS} will be involved.

The current which charges or discharges the gate's electric charge will be the gate drive loss. If the gate drive current is I_d and the charge of all gates (when gate voltage is HIGH) is Q_{GSH}, the following equation is valid:

$$I_d = Q_{GSH} \cdot f_{OSC} \quad \cdots\cdots (8)$$

Here, f_{OSC} is the switching frequency (oscillation frequency)

Depending on the size of the MOS FET, the gate drive current may reach up to one hundred mA in 500kHz so that the heat generation of the IC becomes fairly large. In this case, any one of the following action should be taken:

① Attach a radiation fan to the IC.
② Use a board with good radiation characteristics.
③ Use an output buffer circuit described below.

Output Buffer Circuit

For example, use the following output buffer circuit as shown in Figure 15 when the device drives a large electric charge or bipolar transistors.

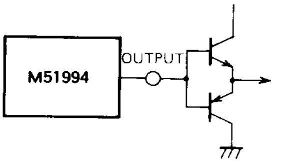
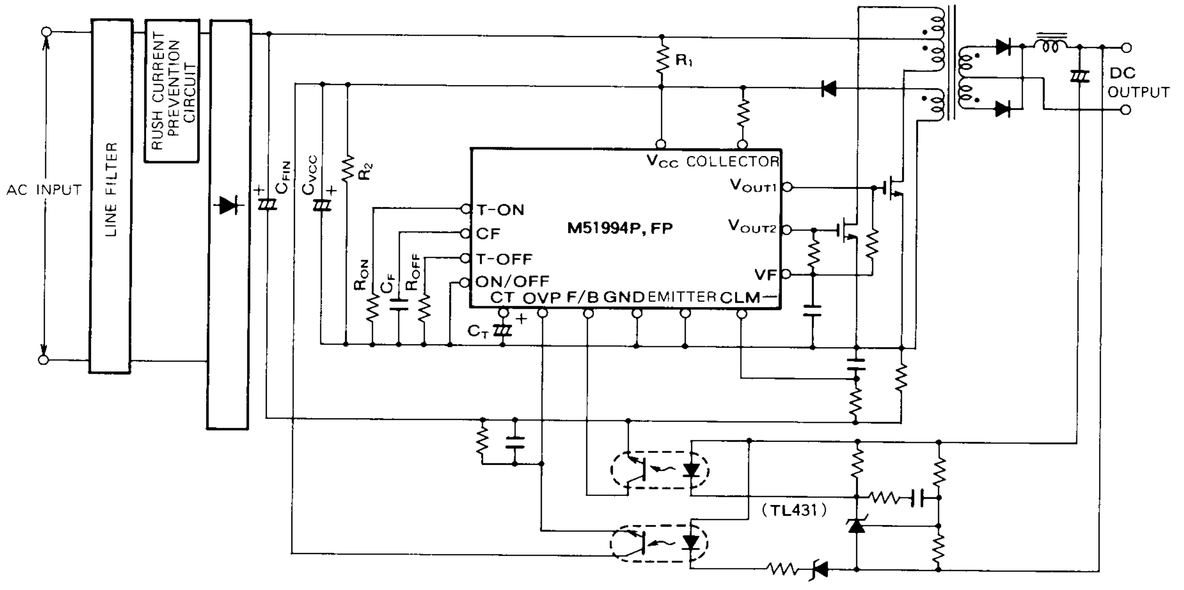


Figure 15 A buffer circuit is added to the output

EXAMPLE OF AN APPLICATION CIRCUIT



• WHEN THE CLM-PIN IS SMALL THE CONSTANT CR IS USED FOR CUTTING NOISES WHILE THE MOS FET IS SET TO ON.

Figure 16 Application circuit for a push-pull regulator