T-79-05-40

LA6324M

3034A

Monolithic Linear IC

Ⓔ1126C

High-Performance Quad Operational Amplifier

The LA6324M consists of four independent, high-performance, internally phase compensated operational amplifiers that are designed to operate from a single power supply over a wide range of voltages. These four operational amplifiers are packaged in a single package. As in case of conventional general-purpose operational amplifiers, operation from dual power supplies is also possible and the power dissipation is low.
It can be applied to various uses in commercial and industrial equipment including all types of transducer amplifiers, DC amplifiers.

Features

- No phase compensation required
- Wide operating voltage range: 3.0 to 30.0V (single supply)
  ±1.5 to ±15.0V (dual supplies)
- Input voltage range includes the neighborhood of GND level and output voltage range V_{OUT} is from 0 to V_{CC} −1.5V.
- Small current dissipation: I_{CC}=0.6mA typ/V_{CC}=+5V, R_L=∞
- Mini flat package enabling compactness of sets

Maximum Ratings/T_a=25°C

			unit
Maximum supply voltage	V_{CC} max	32	V
Differential input voltage	V_{ID}	32	V
Maximum input voltage	V_{IN} max	−0.3~+32	V
Allowable power dissipation	P_d max	330	mW
Operating temperature	T_{opg}	−30~+85	°C
Storage temperature	T_{stg}	−55~+125	°C

Operating Characteristics/T_a=25°C, V_{CC}=+5V

			Test circuit	min	typ	max	unit
Input offset voltage	V_{IO}		1		±2	±7	mV
Input offset current	I_{IO}	$I_{IN}(+)$ / $I_{IN}(-)$	2		±5	±50	nA
Input bias current	I_B	$I_{IN}(+)$ / $I_{IN}(-)$	3		45	250	nA
Common-mode input voltage range	V_{ICM}		4	0		V_{CC}−1.5	V
Common-mode rejection ratio	CMR		4	65	80		dB
Large amplitude voltage gain	V_G	V_{CC}=15V, R_L≧2kΩ	5	25	100		V/mV
Output voltage range	V_{OUT}			0		V_{CC}−1.5	V
Power supply voltage rejection	SVR			65	100		dB
Channel separation		f=1k to 20kHz			120		dB
Current dissipation	I_{CC}		8		0.6	2	mA
	I_{CC}	V_{CC}=30V	8		1.5	3	mA

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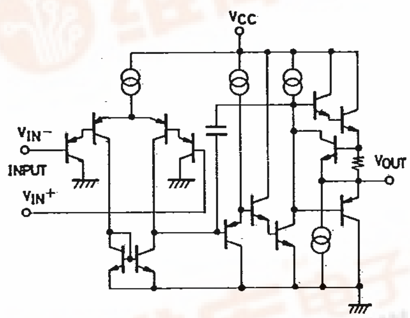
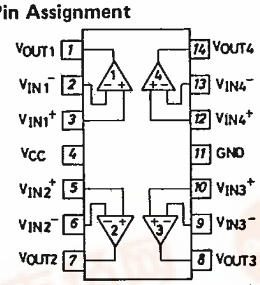
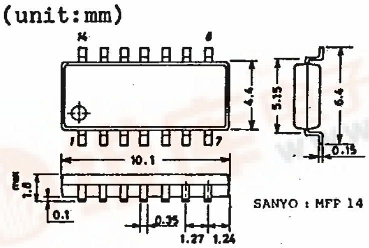
Equivalent Circuit (1 unit)



Pin Assignment



Case Outline 3034A-M14IC
(unit:mm)



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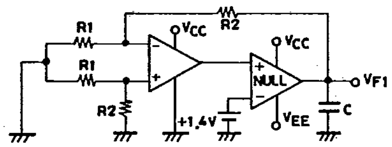
			Test circuit	min	typ	max	unit
Output current (source)	I_O source	$V_{IN}+=1V, V_{IN}-=0V$	9	20	40		mA
Output current (sink)	I_O sink	$V_{IN}+=0V, V_{IN}-=1V$	10	10	20		mA

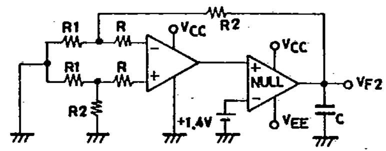
Test Circuits

1 Input offset voltage V_{IO}



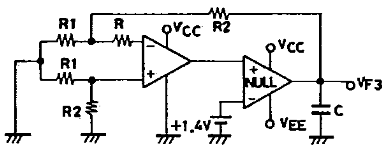
$$V_{IO} = \frac{V_{F1}}{1 + R2/R1}$$

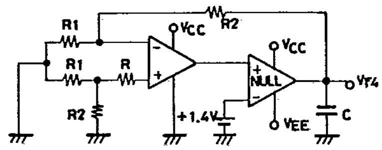
2 Input offset current I_{IO}



$$I_{IO} = \frac{V_{F2} - V_{F1}}{R(1 + R2/R1)}$$

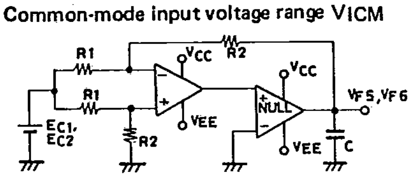
3 Input bias current I_B





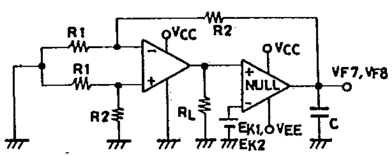
$$I_B = \frac{V_{F4} - V_{F3}}{2R(1 + R2/R1)}$$

4 Common-mode rejection ratio CMR
Common-mode input voltage range V_{ICM}



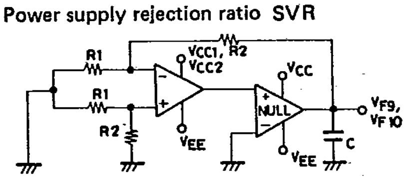
$$CMR = 20 \log \left| \frac{(E_{C1} - E_{C2})(1 + R2/R1)}{V_{F5} - V_{F6}} \right|$$

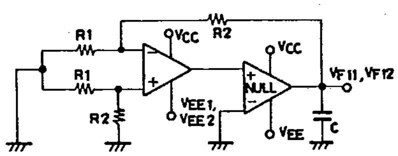
5 Voltage gain VG



$$VG = \frac{(E_{K1} - E_{K2})(1 + R2/R1)}{V_{F8} - V_{F7}}$$

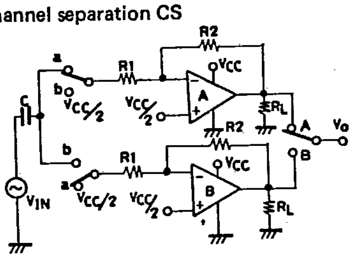
6 Power supply rejection ratio SVR





$$SVR(+) = 20 \log \left| \frac{(1 + R2/R1)(V_{CC1} - V_{CC2})}{V_{F9} - V_{F10}} \right| \quad SVR(-) = 20 \log \left| \frac{(1 + R2/R1)(V_{EE1} - V_{EE2})}{V_{F11} - V_{F12}} \right|$$

7 Channel separation CS



SW: a

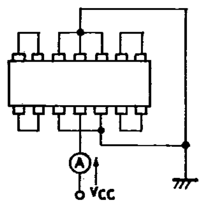
$$CS\ (A \to B) = 20 \log \frac{R_2}{R_1} \frac{V_{OA}}{V_{OB}}$$

SW: b

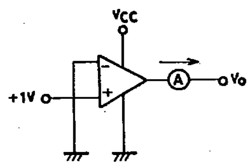
$$CS\ (B \to A) = 20 \log \frac{R_2}{R_1} \frac{V_{OB}}{V_{OA}}$$

These apply also to other channels.

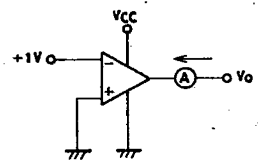
8 Current dissipation ICC



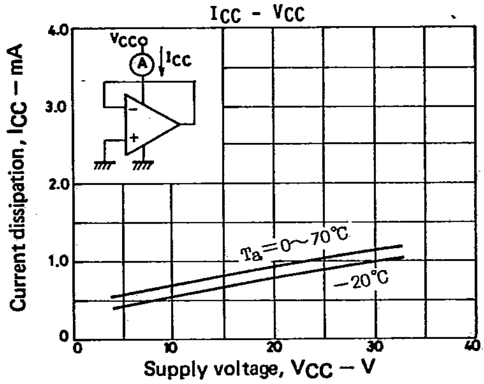
9 Output current IO source



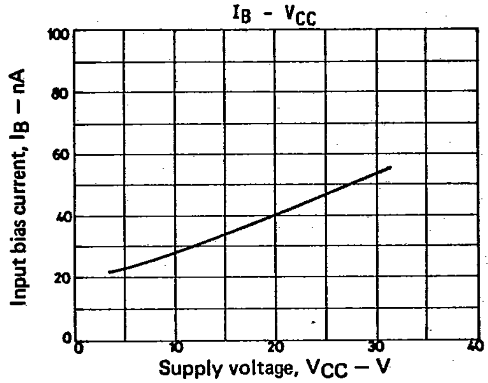
10 Output current IO sink



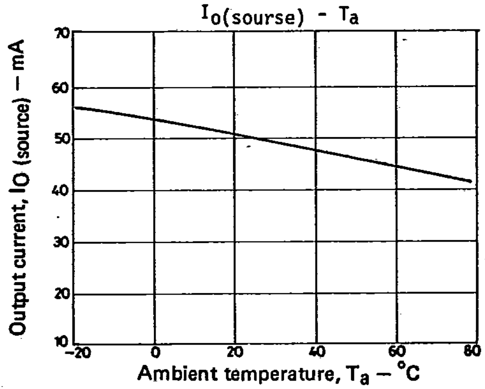
ICC - VCC



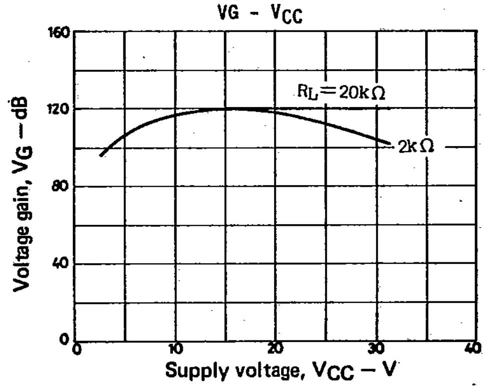
IB - VCC



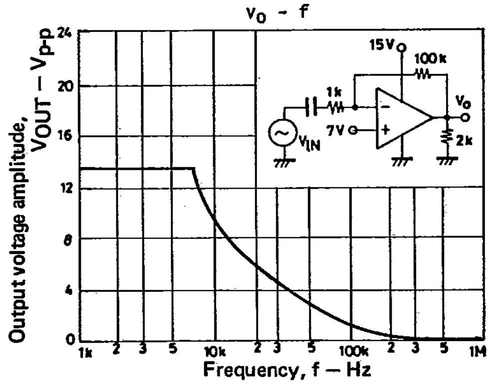
Io(sourse) - Ta



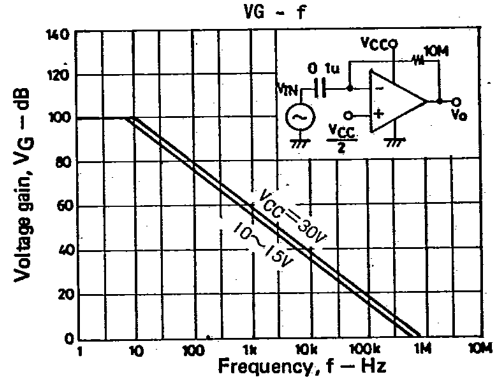
VG - VCC

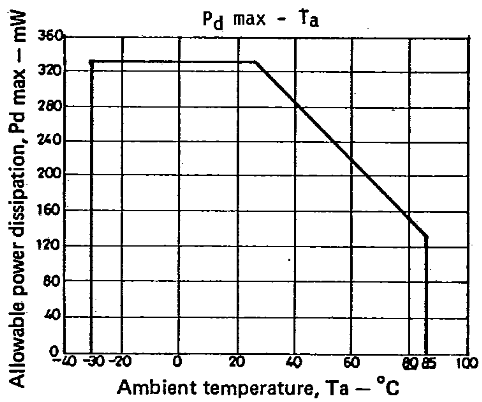


Vo - f



VG - f





■ Sample Application Circuits