TEMIC

Siliconix

SMP50N06-25

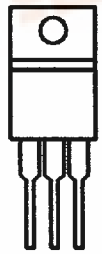
N-Channel Enhancement-Mode MOSFET, 25-mΩ $r_{DS(on)}$

175°C Maximum Junction Temperature

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.025	50

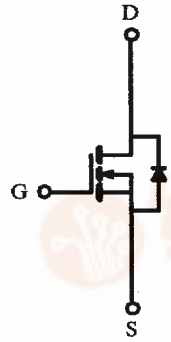
TO-220AB



DRAIN connected to TAB

G D S

Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 175°C)	T_C = 25°C	I_D	50	A
	T_C = 100°C		35	
Pulsed Drain Current		I_{DM}	130	
Continuous Source Current (Diode Conduction)		I_S	50	
Avalanche Current		I_{AR}	50	
Avalanche Energy	L = 0.1 mH	E_{AS}	125	mJ
Repetitive Avalanche Energy[a]	L = 0.05 mH	E_{AR}	62.5	
Maximum Power Dissipation	T_C = 25°C	P_D	131	W
	T_C = 100°C		65	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		80	°C/W
Maximum Junction-to-Case	R_{thJC}		1.14	
Case-to-Sink	R_{thCS}	1.0		

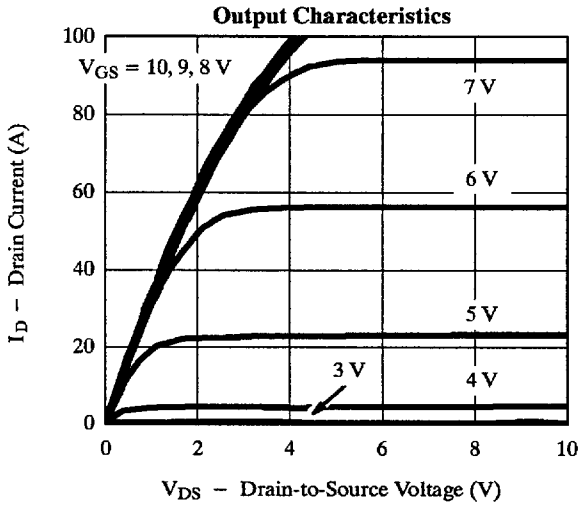
Notes:
a. Duty cycle ≤ 1%

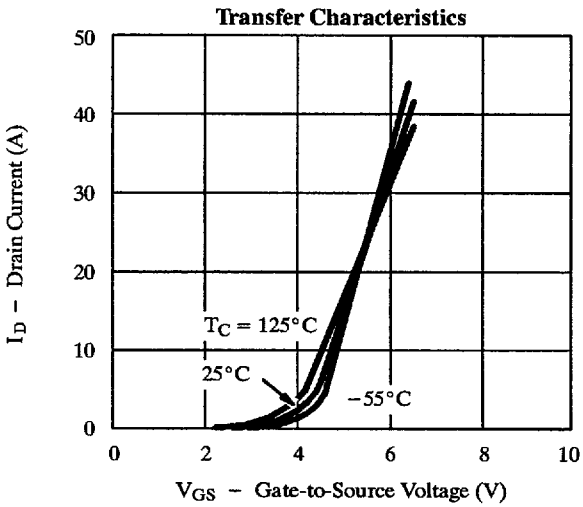
Specifications (T_J = 25°C Unless Otherwise Noted)

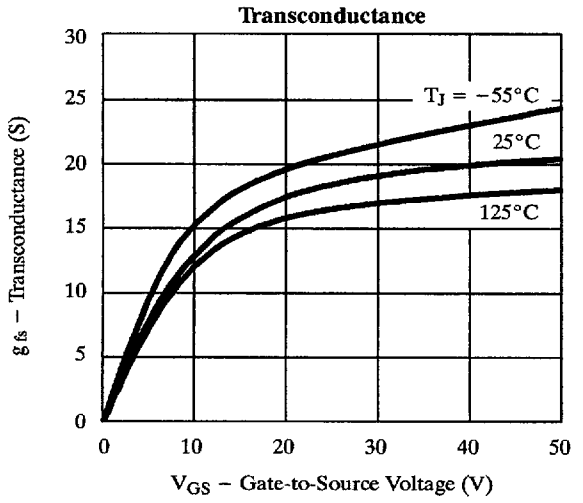
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2		4	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C			250	
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	50			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 25 A		0.020	0.025	Ω
		V_{GS} = 10 V, I_D = 25 A, T_J = 125°C		0.033	0.042	
		V_{GS} = 10 V, I_D = 25 A, T_J = 175°C		0.043	0.0525	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 25 A		20		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2000		nC
Output Capacitance	C_{oss}			570		
Reverse Transfer Capacitance	C_{rss}			120		
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 50 A		55	80	
Gate-Source Charge	Q_{gs}			9	15	
Gate-Drain Charge	Q_{gd}			24	40	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.6 Ω I_D ≅ 50 A, V_{GEN} = 10 V, R_G = 2.5 Ω		15	30	ns
Rise Time	t_r			20	35	
Turn-Off Delay Time	$t_{d(off)}$			40	65	
Fall Time	t_f			15	30	
Source-Drain Diode Ratings and Characteristics						
Diode Forward Voltage[b]	V_{SD}	I_F = 50 A, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = 50 A, di/dt = 100 A/µs		130		ns
Peak Reverse Recovery Current	$I_{RM(rec)}$			10		A
Reverse Recovery Charge	Q_{rr}			0.7		µC

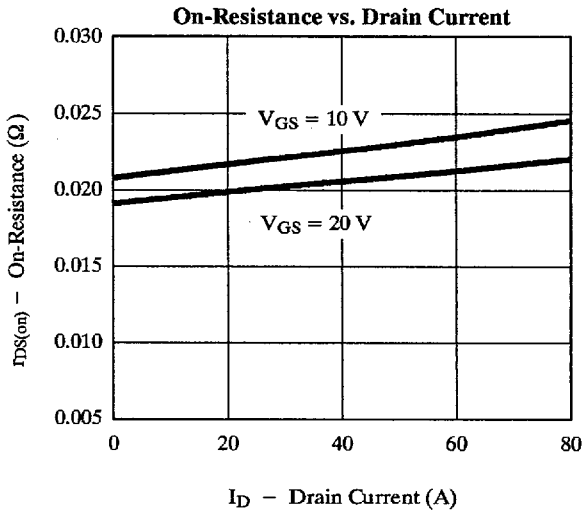
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

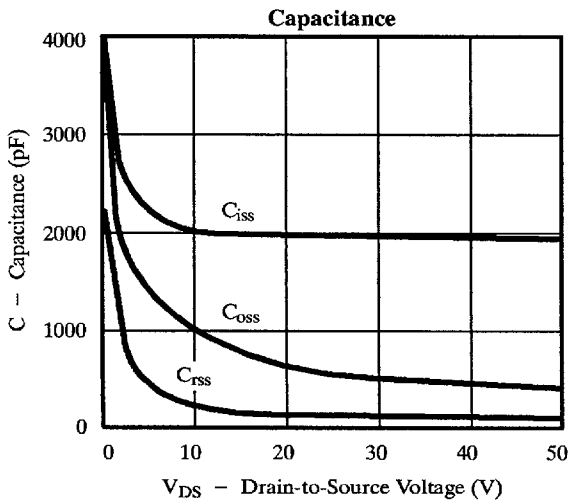
Typical Characteristics (25°C Unless Otherwise Noted)

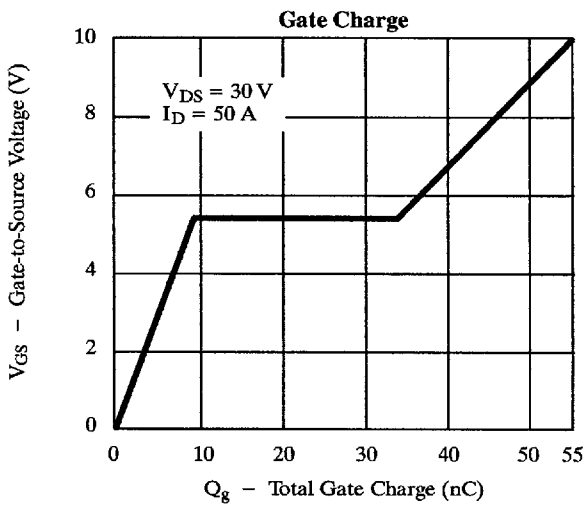








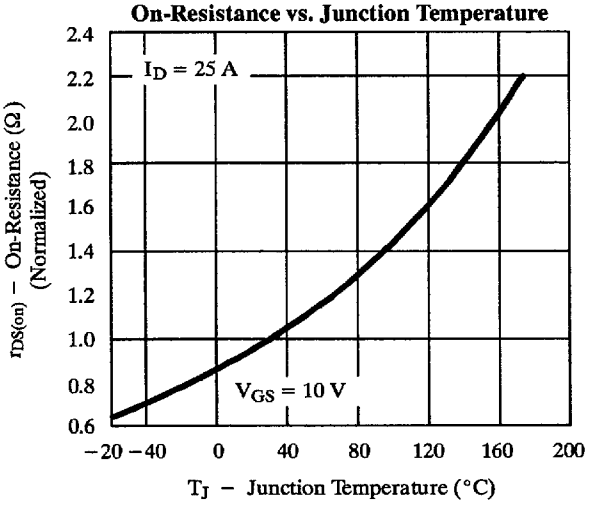




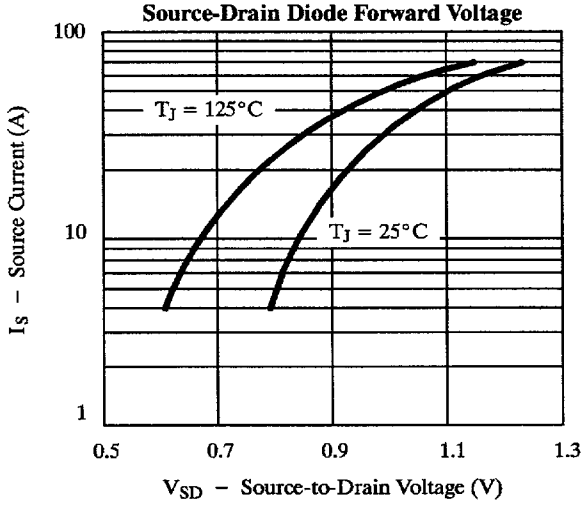
SMP50N06-25

Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

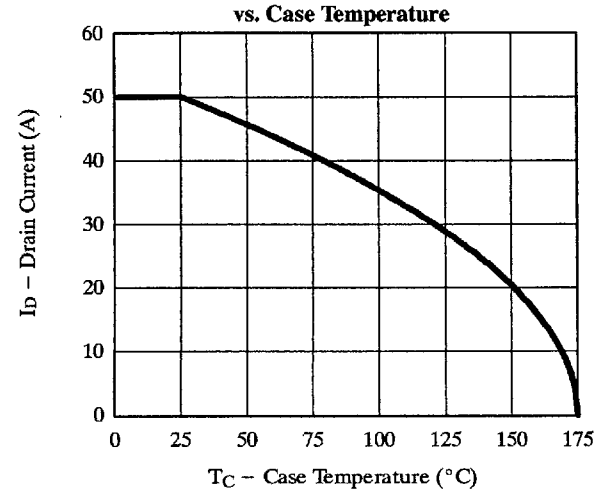


Source-Drain Diode Forward Voltage

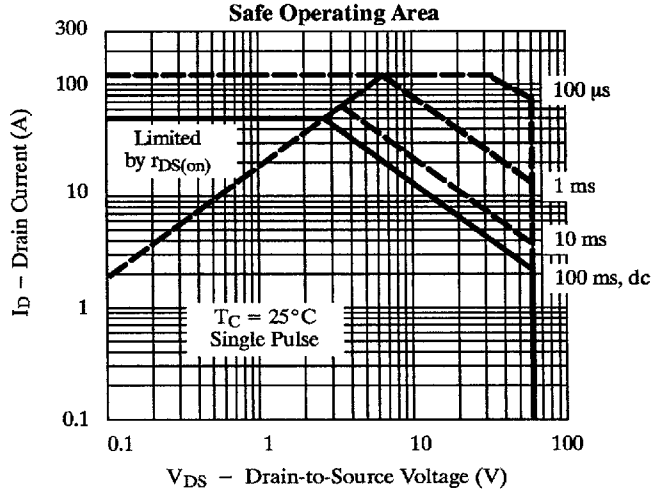


Thermal Ratings

Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case