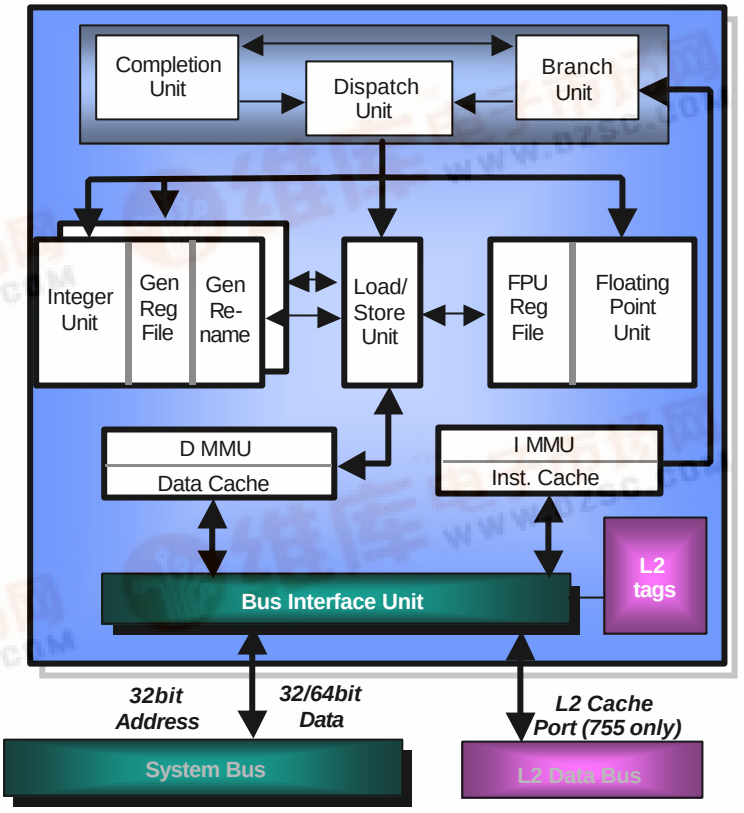
PC745B/PC755BFS - Rev.1 – 01/11

PC745B AND PC755B PowerPC™ Microprocessors Fact Sheet

PC745B and PC755B PowerPC microprocessors are high-performance, low-power, 32-bit implementations of the PowerPC Reduced Instruction Set Computer (RISC) architecture, specially enhanced for embedded applications. The PC755B and PC745B microprocessors differ only in that the PC755B features an enhanced, dedicated L2-cache interface with on-chip L2-tags. Both are software compatible with the PowerPC603e microprocessor family and the PC745B is pin-compatible as well. Both PC745B and PC755B are fully JTAG compliant.

PC745B and PC755B Main Features

- **Six independent execution units**
  - 2 Integer Units sharing 32 General Purpose Registers
  - Floating Point Unit using a 32-entry FPR file
  - Branch Processing Unit : 4 instructions fetched per clock
  - Load/Store Unit
  - System Register Unit
- **Cache and MMU support**
  - 32-Kbytes, physically addressed, Instruction and Data caches
  - 8-way set associative Instruction and Data caches
  - Dedicated L2-cache with on-chip L2 tags (PC755B only)
  - Separate Instruction and Data MMUs
  - Virtual memory support up to 4 Petabytes (2^{52})
  - Real memory support up to 4 Gigabytes (2^{32})
  - 128-entry instruction and data TLBs



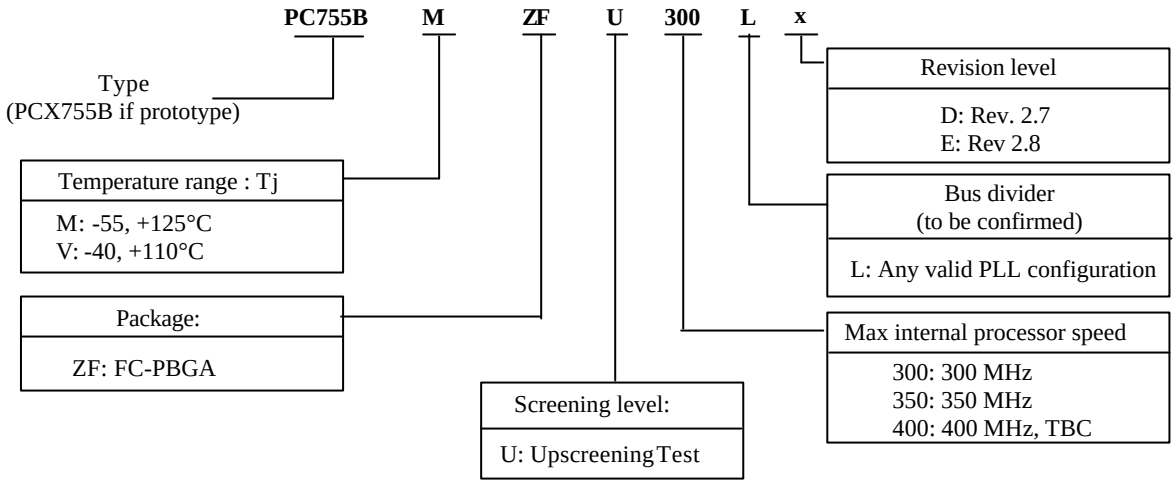
- **Bus Interface**
  - Compatible with 60x processor interface
  - 32-bit address bus
  - 64-bit data bus, 32-bit mode selectable
  - 13 Bus-to-Core frequency multipliers
  - Selectable interface voltages

- **Power Management**
  - Low-power design
  - Selectable 1.8V/2.0V interface voltage
  - 3 static power saving modes : doze, nap and sleep
  - Dynamic power management
  - Integrated thermal management unit

- **Packaging**
  - 255 Flip-Chip PBGA (PC745B)
  - 360 Flip-Chip PBGA (PC755B)
  - 255 and 360 CBGA available upon request

- **Screening**
  - FC-PBGA upscreening based upon ATMEL-Grenoble standards
  - Full Military temperature range (Tj = -55°C, + 125°C)
  - Industrial temperature range (Tj = -40°C, +110°C)

CPU Summary	PC745B 300 - 350 MHz	PC755B 300 - 400 MHz
Die Revision	2.7 = D	2.7 = D
CPU Speeds - Internal	300 MHz	300 MHz
	350 MHz	350 MHz
		400 MHz
CPU Bus Dividers	2x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 10x	2x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 10x
Bus Interface	32-bit address, 32/64-bit data	32-bit address, 32/64-bit data
Instructions per Clock	3 (2+Branch)	3 (2+Branch)
L1 Cache	32-KB Instruction and Data	32-KB Instruction and Data
L2 Cache	-	256KB, 512KB, 1MB
Core-to-L2 Frequency Divisions	-	1:1, 1.5:1, 2:1, 2.5:1, 3:1
Typ/Max Power Dissipation	4.0W/5.7W @ 350 MHz	4.4W/6.4W @ 400 MHz
Die Size	51 mm^2	51 mm^2
Package	255-pin Flip-Chip PBGA	360-pin Flip-Chip PBGA
	Ceramic Package if Identifications	Ceramic Package if Identifications
Process	0.22µ CMOS, 5LM	0.22µ CMOS, 5LM
Voltage	1.8/2.0 or 3.3V I/O	1.8/2.0 or 3.3V I/O
	2.0V internal	2.0V internal
SPECint95 (estimated)	15.7 @ 350 MHz	18.1 @ 400MHz
SPECfp95 (estimated)	11.6 @ 350 MHz	12.3 @ 400MHz
Other Performance	641 MIPS @ 350 MHz	733 MIPS @ 400MHz
Status	Active	Active
Samples	Now	Now
Production	Now	Now
Execution Units	Integer (2)	Integer (2)
	Floating Point Unit	Floating Point Unit
	Branch Unit	Branch Unit
	Load/Store Unit	Load/Store Unit
	System Register	System Register



For additional information:
contact your local ATMEL-Grenoble representative
or visit our web site at http://www.atmel-grenoble.com

You may also contact the PowerPC technical hotline at std.hotline@atmel-grenoble.com

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