

# OKI Semiconductor

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## MSM7532

### Single Chip MSK Modem with Compandor for Cordless Telephone

#### GENERAL DESCRIPTION

The MSM7532 is a baseband device with a modem function and a baseband voice signal processing function for analog cordless telephone. The voice signal transmitter in this IC consists of a high-pass filter, compressor, scrambler, pre-emphasis, limiter, and splatter filter.

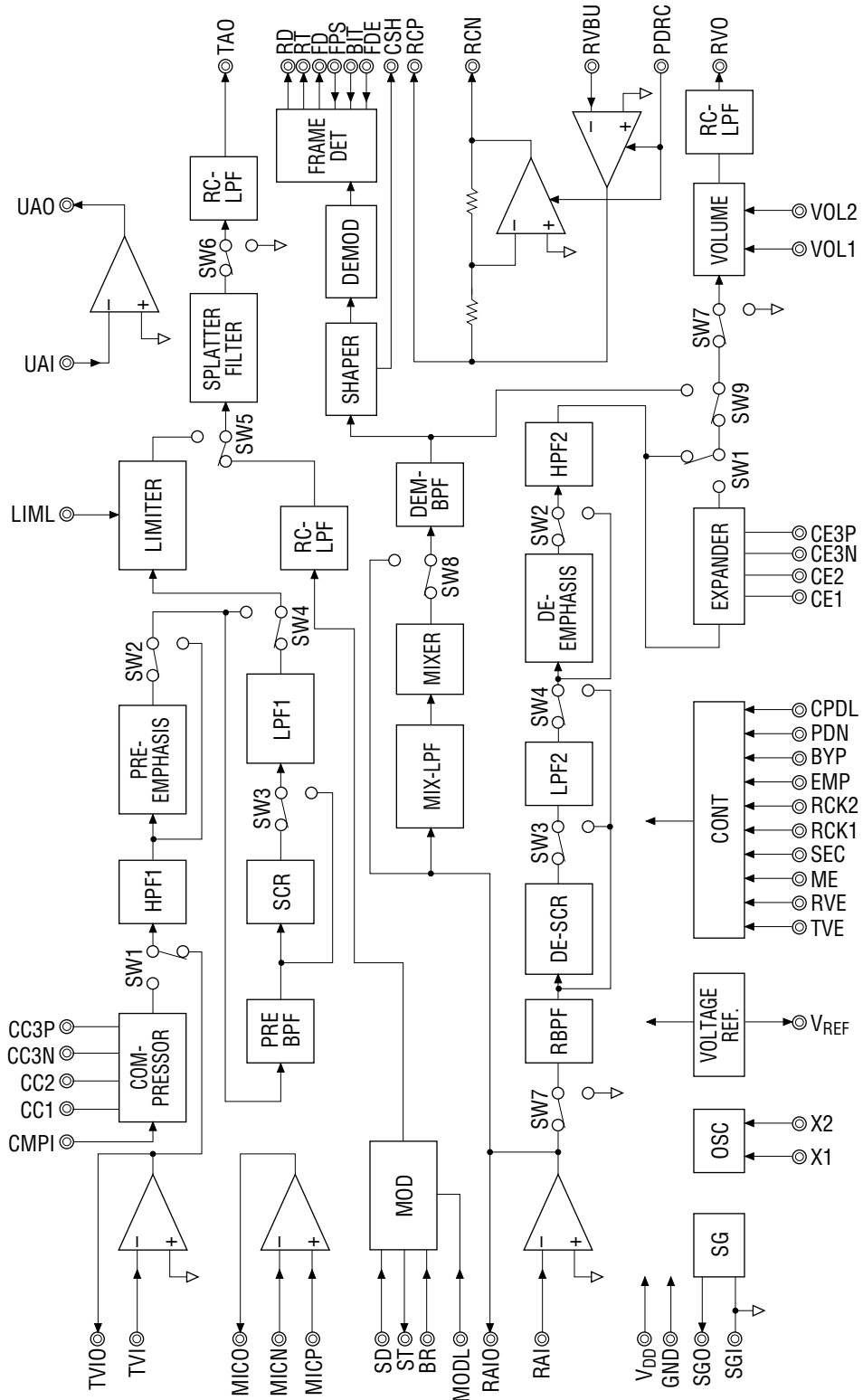
The voice signal receiver consists of a bandpass filter, a de-scrambler, a de-emphasis, an expander, an electronic volume, and a ceramic receiver driving circuit.

The MODEM in this IC transmits and receives MSK (Minimum Shift Keying) modem signals.

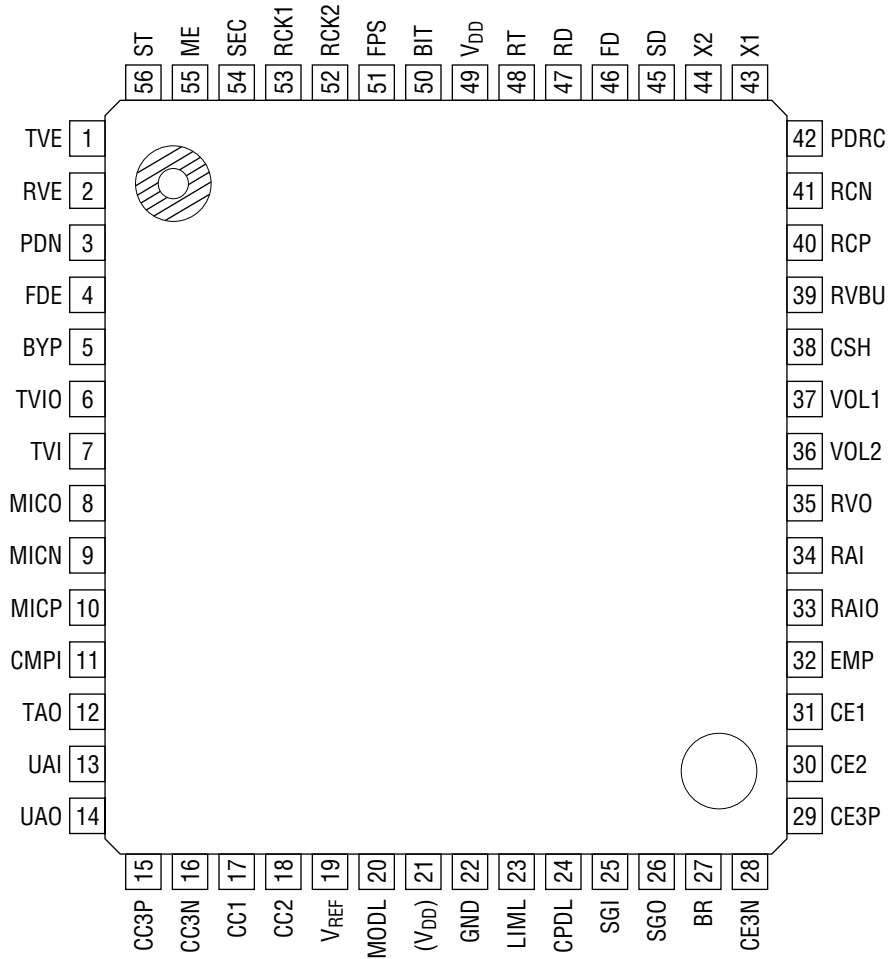
#### FEATURES

- Built-in ceramic receiver drive amplifiers
- The compander input reference level, limiter level, and modem transmit level are easy to be externally adjusted.
- Built-in 2-bit electronic volume
- A microphone amplifier and an amplifier available for users are built in.
- Mode settings using parallel interfaces
- Built-in compander dynamic range: 70 dB
- Built-in maximum gain limit circuit for expander
- The bit rate of MSK modem is switchable between 2400 bps and 1200 bps.
- Scrambler and emphasis can be used by serially connecting them or can be used separately with each other.
- Three kinds of the reverse frequency of the scrambler are selectable.
- The modem receiver functions detect bit synchronous signals and frame synchronous signals.
- Four-step power down modes
- Built-in crystal oscillation circuit
- Wide range of power supply (1.8 V to 5.5 V)
- Package:  
56-pin plastic QFP (QFP56-P-910-0.65-2K) (Product name : MSM7532GS-2K)

BLOCK DIAGRAM



**PIN CONFIGURATION (TOP VIEW)**



**56-Pin Plastic QFP**

Notes: The pin 49 should be used for  $V_{DD}$ .  
 The pin 21 should be connected to  $V_{DD}$  or opened.

## PIN AND FUNCTIONAL DESCRIPTIONS

### TVE

Transmit voice signal output control pin.  
Refer to the TAO pin description.

### RVE

Receive voice signal output control pin.  
Refer to the RVO pin description.

### PDN

Power down control pin.  
The four-step power down modes are controlled by the PDN, ME, RVE, and TVE pins.

|               | PDN              | RVE | TVE | ME | Voice signal<br>Processing Section | Transmit Modem | Receive Modem | Crystal<br>Oscillation Circuit |
|---------------|------------------|-----|-----|----|------------------------------------|----------------|---------------|--------------------------------|
| <b>Mode 1</b> | 1                | 0   | 1   | X  | OFF                                | OFF            | OFF           | OFF                            |
| <b>Mode 2</b> | 1                | 0   | 0   | X  | OFF                                | OFF            | OFF           | ON                             |
| <b>Mode 3</b> | 1                | 1   | X   | X  | OFF                                | OFF            | ON            | ON                             |
| <b>Mode 4</b> | 0                | 0   | 0   | 1  | OFF                                | ON             | ON            | ON                             |
| <b>Mode 5</b> | Other than above |     |     |    | ON                                 | ON             | ON            | ON                             |

X: Don't care

In Mode 5, all the circuits are ON.

The MODEM demodulation circuit and FD pin are reset to zero by setting to Mode 1 or Mode 2 (PDN = "1", RVE = "0").

After turning the power ON, set the LSI into one of these modes, then reset it before using. To hold the voice signal processing section ON during transmission of MSK signals, set the ME and TVE pins to "1". In this case, the input from TVI is not output to TAO. Refer to the TAO pin description.

### FDE

Pin used to control the function of frame synchronous signal detection circuit.

If digital "0" is entered in this pin, the FD pin remains reset at "0" level. The RT and RD pins are always active.

If digital "1" is entered in this pin, the frame synchronous signal detection circuit becomes active. And the RT and RD pins are fixed at "1" level until the FD pin goes to "1" level by detecting the frame synchronous signals.

Refer to Figure 3 "Receive Signal Timing".

### BYP

Compannder path selection pin.

| BYP | Transmit side                        | Receive side                       | Note |
|-----|--------------------------------------|------------------------------------|------|
| 0   | Compressor is connected to the path. | Expander is connected to the path. | SW1  |
| 1   | Compressor is bypassed to the path.  | Expander is bypassed to the path.  |      |

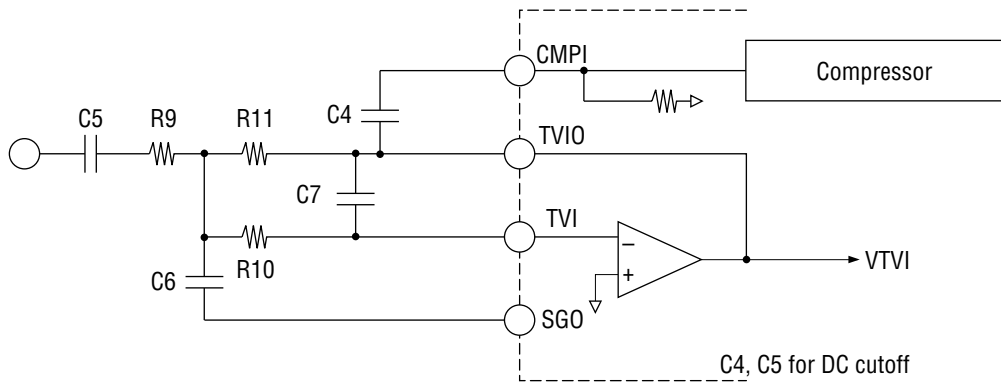
When the expander is used, the maximum gain of expander is limited to approximately +12 dB. This tendency will appear as the input signal level is increased when  $V_{DD}$  is larger (e. g., 5 V) and  $V_{CPDL}$  is smaller (e.g., 0.1 V); the input/output characteristics then change automatically from expander characteristics to linear characteristics with constant gain.

**TVI, TVIO**

Pins used to constitute an RC-active filter on the transmit input side.

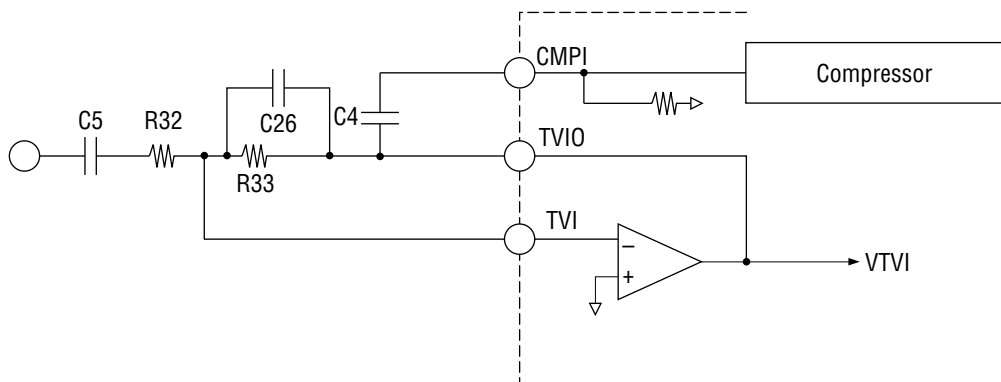
If input signals have frequency components over 50 kHz, these components are output as aliasing noises from the built-in SCF circuit. In order to remove these noises, insert the first or second order RC-active filter with about 10 kHz cut-off frequency, as shown below.

<Second order RC-active filter configuration>



In the case of  $f_c = 10 \text{ kHz}$ , gain : 0 dB  $\left( \begin{array}{l} R9 = R10 = R11 = 68 \text{ k}\Omega \\ C5 = 0.22 \text{ }\mu\text{F}, C6 = 510 \text{ pF}, C7 = 110 \text{ pF} \end{array} \right)$

<First order RC-active filter configuration>

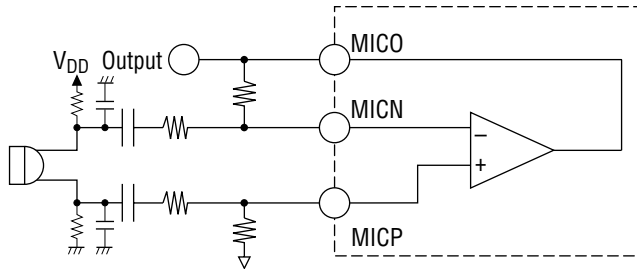


In the case of  $f_c = 10 \text{ kHz}$ , gain : 0 dB  $\left( \begin{array}{l} R32 = R33 = 51 \text{ k}\Omega \\ C5 = 0.22 \text{ }\mu\text{F}, C26 = 300 \text{ pF} \end{array} \right)$

**MICO, MICN, MICP**

MICN is the microphone amplifier inverting input pin, MICP is the non-inverting input pin, and MICO is the output pin. Only during power down mode 1 or 2, the amplifier is powered down and the MICO potential is undefined.

These pins can also be used for applications other than microphone amplifier.



**CMPI**

Input pin to the compressor.

Connect this pin to the TVIO pin with a 0.1 μF capacitor in order to prevent the malfunction of the compressor which may occur if DC input offset exists.

**TAO**

Transmit analog signal output pin.

According to control data on ME and TVE, TAO is set as shown below.

| ME | TVE | TAO   | Note |
|----|-----|---|------|
| 0  | 0   | No signal output (potential = V <sub>SG</sub> ) | SW6  |
| 0  | 1   | Voice signal output (signal from TVI, TVIO)     | SW5  |
| 1  | X   | MSK modulator output                            |      |

X: Don't care

**UAI, UAO**

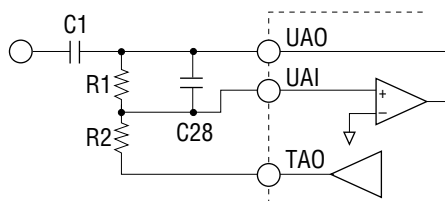
Inverting input pin (UAI) and output pin (UAO) for the amplifier available for users.

These pins are used as a gain control amplifier that can match the internal signal level of the LSI with the input level of the radio circuit.

The amplifier can drive a resistance over 2 kΩ.

In the power down mode 1 and 2, the amplifier enters power down mode.

Since the amplifier uses the power supply for the built-in transmitter, the amplifier should be used to control signals for the transmitter. C28 is a capacitor for oscillation prevention. Be sure to use a capacitor of 20 pF or more. If this amplifier is not used, connect UAI to UAO directly and remove R1, R2, C1, and C28.



**CC3P, CC3N**

Pins used to connect a capacitor for defining a time constant of output transient response for the compressor.

Insert a 0.22 μF capacitor between CC3N and CC3P.

**CC2, CC1**

Pins used to connect capacitors for removing DC offset in the compressor.

Insert a 0.22 μF capacitor between CC2 and SGO, and between CC1 and SGO.

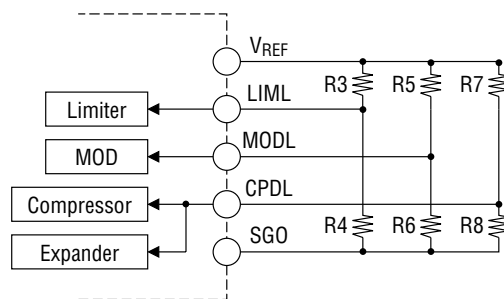
**V<sub>REF</sub>**

Output pin for internal reference voltage source.

The V<sub>REF</sub> output voltage is V<sub>SG</sub> + 0.5 V.

The voltages into which the voltage between V<sub>REF</sub> pin and SGO pin is divided by the resistors should be supplied to the LIML, MODL, and CPDL pin, respectively.

The V<sub>REF</sub> pin can be directly connected to the LIML pin, MODL pin, or CPDL pin.



**MODL**

DC voltage input pin used to define a transmit output level for MODEM.

One of the voltages into which the voltage between V<sub>REF</sub> pin and SGO pin is divided by the resistors should be supplied to this pin.

Refer to the V<sub>REF</sub> description for voltage division by the resistors.

If the potential difference between this pin and the SGO pin is V<sub>MODL</sub> (V), the TAO output level is expressed as follows.

$$V_{OX} = 20 \cdot \log (V_{MODL}) + 0.5 \text{ (dBV)}$$

**GND**

Ground pin (0V).

**LIML**

Clamp voltage input pin for deviation limiter.

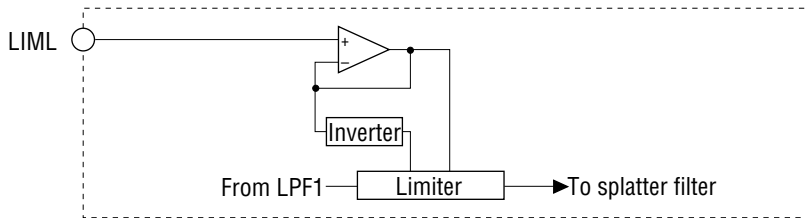
The voice signal maximum RF modulation can be controlled by supplying, to this pin, one of the voltages into which the voltage between V<sub>REF</sub> pin and SGO pin is divided by the resistors.

Refer to the V<sub>REF</sub> description for voltage division by the resistors.

If the potential difference between this pin and the SGO pin is V<sub>LIML</sub> (V), the limiter level is expressed as follows.

$$V_{LIML} = 20 \cdot \log (V_{LIML}) - 3.0 \text{ (dBV)}$$

The DC clamp level is  $V_{SG} \pm V_{LIML}$ .



**CPDL**

Input DC voltage reference level definition pin for compander.

One of the voltages into which the voltage between  $V_{REF}$  pin and SGO pin is divided by the resistors should be supplied to this pin. Refer to the  $V_{REF}$  description for voltage division by the resistors. If the potential difference between this pin and the SGO pin is  $V_{CPDL}$ , the compressor and expander input reference levels are expressed as follows.

$$V_{ICS} = V_{IES} = 20 \cdot \log(V_{CPDL}) - 5.8 \text{ (dBV)}$$

The compressor input reference level and expander input reference level change simultaneously.

**SGI**

Built-in signal ground that is reference voltage to be supplied to analog circuit.

The DC voltage is one half of the supply voltage.

When the power has fewer noises and fewer ripples, the idle noise can be improved by inserting a bypass capacitor over  $1 \mu\text{F}$  between SGI and GND, and between SGI and  $V_{DD}$ . If the power has a lot of noises, do not insert a bypass capacitor between SGI and  $V_{DD}$  to reduce supply noises.

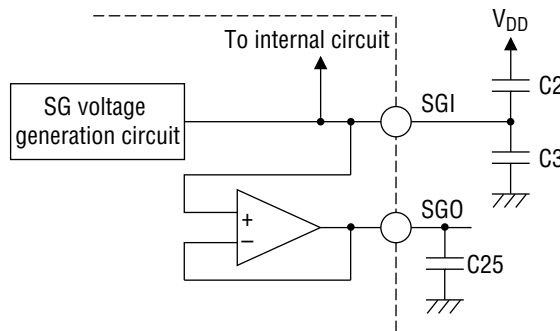
Other capacitors and resistors should be connected to the SGO pin.

**SGO**

Signal ground voltage output pin for LSI external circuits.

The DC voltage is one half of the supply voltage.

Insert a  $1 \mu\text{F}$  capacitor between SGO and GND.



**BR**

MODEM data signaling rate switching input.

| BR | Data Signaling Rate | Note |
|----|---------------------|------|
| 0  | 1200 bps            | SW8  |
| 1  | 2400 bps            |      |

**CE3P, CE3N**

Pins used to connect a capacitor for defining a time constant of output transient response for the expander.

Insert a  $0.22 \mu\text{F}$  capacitor between CE3N and CE3P



**CE1, CE2**

Pins used to connect a capacitor for removing DC offset in the expander.  
 Insert a 0.22  $\mu$ F capacitor between CE1 and SGO, an 1  $\mu$ F capacitor between CE2 and SGO.

**EMP**

Emphasis path selection pin.

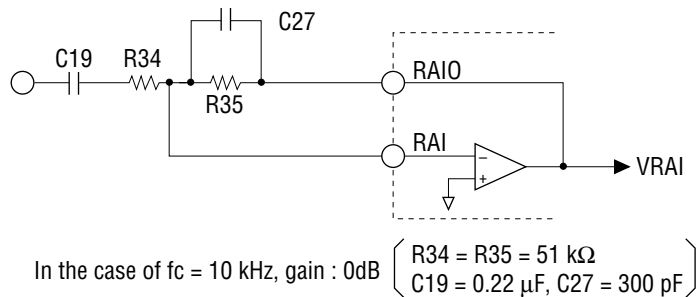
| EMP | Transmit side                                 | Receive side                                 | Note |
|-----|---|--|------|
| 0   | Pre-emphasis circuit is bypassed to the path  | De-emphasis circuit is bypassed to the path  | SW2  |
| 1   | Pre-emphasis circuit is connected to the path | De-emphasis circuit is connected to the path |      |

**RAIO, RAI**

Pins used to constitute RC-active filter on the receive signal input side.  
 Refer to the TVIO and TVI description.

If the Scrambler circuit is used, using the first order RC-active filter is recommended. In this case, configure the filter so that either R34 or R35, or both of them, is 60 k $\Omega$  or less.

<First order RC-active filter configuration>



**RVO**

Receive voice signal output pin.

The RVO state is controlled depending on the digital data set to RVE.

| RVE | RVO                                     | Note |
|-----|---|------|
| 0   | No signal output (voltage = $V_{SG}$ )  | SW7  |
| 1   | Output of signals input to RAI and RAIO |      |

**VOL1, VOL2**

Pins used to set up a gain for the electronic volume.

The volume at the stage next to expander is controlled by the pins.

| VOL2 | VOL1 | Gain   |
|------|------|--------|
| 0    | 1    | +6 dB  |
| 0    | 0    | 0 dB   |
| 1    | 1    | -6 dB  |
| 1    | 0    | -12 dB |

**CSH**

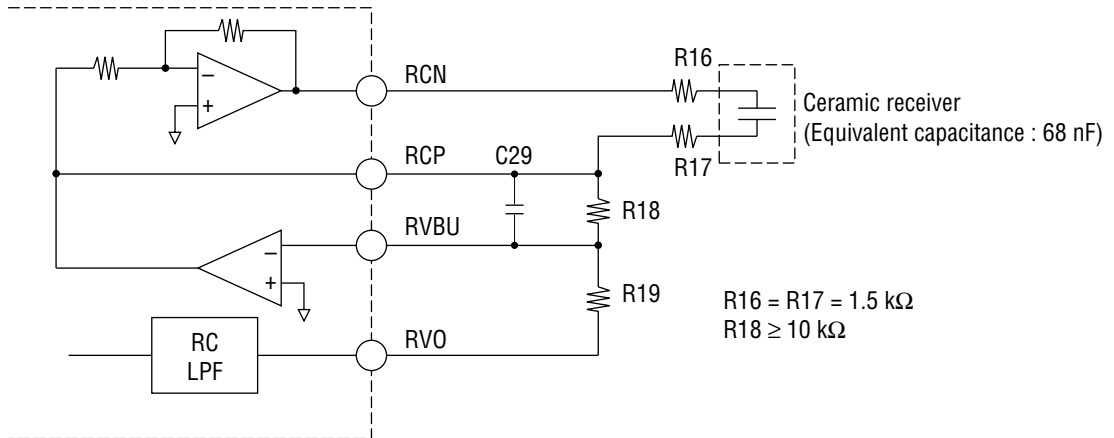
Pin used to connect a capacitor for removing DC offset in shaper of modem receiver.  
 Insert a 1  $\mu$ F capacitor between this pin and GND.

**RVBU**

Ceramic receiver amplifier input pin.  
Refer to the RCN, RCP description.

**RCP, RCN**

Ceramic receiver amplifier output pins.



C29 is a capacitor for oscillation prevention. Be sure to use a capacitor of 20 pF or more.

If no ceramic receiver amplifier is used, RVBU should be directly connected to RCP, RCN be open, and R16 to R19, and C29 be removed.

**PDRC**

Pin used to control power down of the ceramic receiver amplifier.

If digital "1" is input in this pin, the two ceramic receiver amplifiers are powered down. If the LSI is in power-down mode 1 or 2 (PDN = "1", RVE = "0"), the ceramic receiver amplifiers are powered down even when the PDRC is at "0".

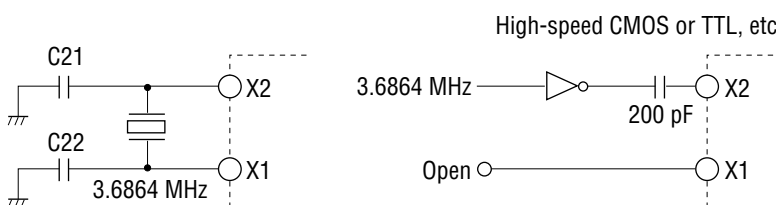
**X1, X2**

Crystal oscillator connection pins.

3.6864 MHz crystal oscillator should be connected.

If the load capacitance of the crystal oscillator is 16 pF, insert a 12 pF capacitor between X1 and GND and between X2 and GND.

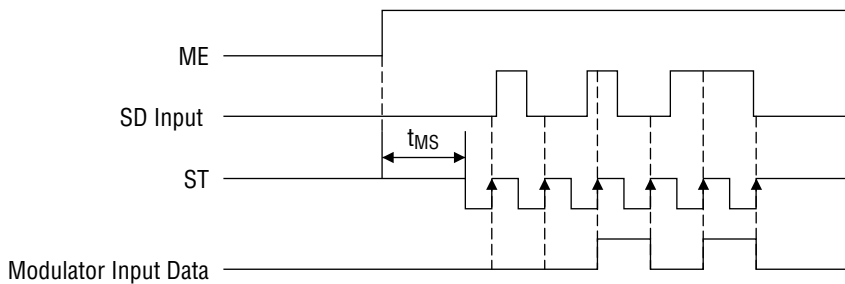
If an external clock is used, with X1 opened, the clock should be input from X2 through a 200 pF capacitor.



**SD**

Transmit data input pin.

The data on the SD pin is accepted as the modulator input signals in synchronization with the rising edges of ST.



At the start of data transmission, the synchronization with the receive modem is required. Therefore bit synchronous signals (the alternating patterns of "1" and "0") more than 18 bits should be input in SD.

If a radio transmission path is better in S/N ratio, the receive section can properly operate with bit synchronous signals more than 11 bits.

**FD**

Frame synchronous detection signal output pin.

If the contents of received data in the LSI matches the patterns defined by FPS and BIT in a state where FDE is at "1" level, FD holds "1" level. If FDE is at "0" level, FD is fixed at "0" level. FD is also fixed at "0" in power-down mode 1 or 2 (PDN = "1", RVE = "0").

Take the following procedure to detect frame synchronization:

- (1) Set the synchronous patterns to be detected at BIT and FPS.
- (2) Drive FDE at "0" level for 1 ms or more, and then at "1" level. FD is reset to "0" and RT and PD are fixed at "1" level.
- (3) When a frame synchronous signal has been detected, FD is driven at "1" level and RT and RD become active. To ensure detection of frame synchronous signals, lock in PLL of the receive modem. At the beginning of transmission, transmit synchronous patterns after synchronizing with the opposite modem using a bit synchronous signal of 18 bits or more. Refer to "Receiver Signal Timing" in Fig. 3.

**RD**

Receive data output pin.

Outputs demodulation serial data for receive signals.

Since the RD data is output in synchronization with the falling edges of re-generated timing clock pulse RT, it is recommended that the data be latched on the rising edge of RT.

If FDE is at "1" level and FD is at "0" level, RD remains set at "1" level.

**RT**

Receive data timing re-generation clock output pin.

Outputs synchronous clock re-generated by built-in PLL. The data from RD and signals from FD are output in synchronization with falling edges of signals from the RT pin. If FDE is at "1" level and FD is at "0" level, RD remains set at "1" level.

Refer to "Receive Signal Timing" in Fig. 3.

**V<sub>DD</sub>**

Power supply pin.

A bypass capacitor more than 10 μF should be inserted between this pin and GND.

**BIT**

Bit synchronous signal detector control input pin.

The FD pin goes to "1" level when the BIT pin and FDE pin are at "1" level, and a 4-bit synchronous signal and 16-bit frame synchronous signal are successively detected.

The FD pin goes to "1" level when the BIT pin is at "0" level and the FDE pin is at "1" level, and a 16-bit frame synchronous signal is detected.

Refer to the FPS description.

**FPS**

Frame synchronous pattern setup input pin.

| BIT | FPS | Detection Pattern                   | Receiver     |
|-----|-----|-------------------------------------|--------------|
| 0   | 0   | 1001 0011 0011 0110 (= 9336H)       | Handset      |
| 0   | 1   | 1100 0100 1101 0110 (= C4D6H)       | Base station |
| 1   | 0   | 1010 1001 0011 0011 0110 (= A9336H) | Handset      |
| 1   | 1   | 1010 1100 0100 1101 0110 (= AC4D6H) | Base station |

(These synchronous patterns are for Japanese cordless telephones.)

**RCK1, RCK2, SEC**

Reverse frequency selection pins of voice scrambler.

These pins are also used to select filter and scrambler bypass mode.

| SEC | PCK1 | PCK2 | Transmit side  | Receive side  | Note       |
|-----|------|------|--|---|------------|
| 0   | 0    | 0    | Pre-BPF, SCR and LPF1 are bypassed                                     | DE-SCR and LPF2 are bypassed                                    | SW4        |
| 0   | 0    | 1    | Pre-BPF and LPF1 are connected but Scrambler circuit (SCR) is bypassed | LPF2 is connected but De-scrambler (DE-SCR) is bypassed         | SW3<br>SW4 |
| 0   | 1    | 0    |  |   |            |
| 0   | 1    | 1    |  |   |            |
| 1   | 0    | 0    | Pre-BPF, SCR and LPF1 are bypassed                                     | DEM-BPF output is connected to RVO pin via RC-LPF (for IC test) | SW9        |
| 1   | 0    | 1    | Scrambler works  | De-scrambler circuit works                                      | SW3<br>SW4 |
| 1   | 1    | 0    |  |   |            |
| 1   | 1    | 1    |  |   |            |

| RCK1 | RCK2 | Reverse freq. |
|------|------|---------------|
| 0    | 1    | 3200 Hz       |
| 1    | 0    | 3291 Hz       |
| 1    | 1    | 3388 Hz       |

**ME**

Pin used to control MSK modulator output.

If digital "1" is entered to this pin, MSK modulator output is connected to splatter filter input. Refer to the TAO description.

If digital "1" is entered to the ME pin and digital "0" to the PDN, RVE and TVE pins, the voice signal processing system is powered down. Refer to the PDN pin description.

**ST**

Transmit data timing clock output pin.

Signals on the SD pin are accepted in synchronization with the leading edges of the signals from the ST pin. If ME is at "0" level, ST remains set at "1" level.

**ABSOLUTE MAXIMUM RATINGS**

| Parameter                | Symbol           | Condition                    | Rating                       | Unit |
|--------------------------|------------------|------------------------------|------------------------------|------|
| Power Supply Voltage     | V <sub>DD</sub>  | Ta = 25°C<br>Referred to GND | -0.3 to 7                    | V    |
| Analog Input Voltage *1  | V <sub>IA</sub>  |                              | -0.3 to V <sub>DD</sub> +0.3 |      |
| Digital Input Voltage *2 | V <sub>ID</sub>  |                              |                              |      |
| Operating Temperature    | T <sub>op</sub>  | —                            | -30 to +70                   | °C   |
| Storage Temperature      | T <sub>STG</sub> | —                            | -55 to +150                  |      |

\*1: TVI, MICN, MICP, CMPI, UAI, MODL, LIML, CPDL, RAI, RVBU

\*2: TVE, RVE, PDN, FDE, BYP, BR, EMP, VOL1, VOL2, PDRC, X2, SD, BIT, FPS, RCK1, RCK2, SEC, ME

**RECOMMENDED OPERATING CONDITIONS**

| Parameter  | Symbol                       | Condition  | Min         | Typ    | Max                     | Unit                        |     |
|--|------------------------------|--|-------------|--------|-------------------------|-----------------------------|-----|
| Power Supply Voltage                                 | V <sub>DD</sub>              | Referred to GND                                      | +1.8        | +2.4   | +5.5                    | V                           |     |
| Operating Temperature                                | T <sub>op</sub>              | —  | -30         | +25    | +70                     | °C                          |     |
| Data Signaling Rate                                  | T <sub>s</sub>               | BR = "0"   | —           | 1200   | —                       | bit/sec                     |     |
|  |                              | BR = "1"   | —           | 2400   | —                       |                             |     |
| Analog Signal Input Level                            | V <sub>IA</sub>              | TVIO, RAI0 level<br>V <sub>DD</sub> = 2.1 V to 5.5 V | —           | —      | -6                      | dBV                         |     |
|  |                              | V <sub>DD</sub> = 4.5 V to 5.5 V                     | —           | —      | 0                       |                             |     |
| DC Input Range                                       | V <sub>MODL</sub>            | Referred to V <sub>SG</sub>                          | MODL        | 0.05   | 0.25                    | $\frac{1}{3}V_{DD}$<br>-0.2 | V   |
|  | V <sub>LIML</sub>            |  | LIML        | 0.1    | 0.25                    | $\frac{1}{2}V_{DD}$<br>-0.3 |     |
|  | V <sub>CPDL</sub>            |  | CPDL        | 0.1    | 0.25                    | 0.5                         |     |
| Microphone Amplifier Common Mode Input Voltage Range | V <sub>IM</sub>              | MICN, MICP   | 0.85        | —      | V <sub>DD</sub><br>-0.8 |                             |     |
| C2, C3, C13, C15, C25                                | —                            | —  | —           | 1.0    | —                       | μF                          |     |
| C10, C11, C12, C14, C16                              | —                            | —  | —           | 0.22   | —                       |                             |     |
| C4   | —                            | —  | —           | 0.1    | —                       |                             |     |
| C20  | —                            | —  | —           | 10     | —                       |                             |     |
| C21, C22   | —                            | —  | —           | 12     | —                       | pF                          |     |
| C28, C29   | —                            | —  | 20          | —      | —                       |                             |     |
| Crystal Resonator                                    | Frequency                    | —  | —           | 3.6864 | —                       | MHz                         |     |
|  | Freq, Tolerance              | —  | 25 ±5°C     | -100   | —                       | 100                         | ppm |
|  | Temp, Coefficient            | —  | -30 to 70°C | -100   | —                       | 100                         |     |
|  | Equivalent Series Resistance | —  | —           | —      | —                       | 100                         | Ω   |
|  | Load Capacitance             | —  | —           | —      | 16                      | —                           | pF  |

**ELECTRICAL CHARACTERISTICS**

**DC and Digital Interface Characteristics**

(V<sub>DD</sub> = 2.1 V to 5.5 V, T<sub>a</sub> = -30 to 70°C)

| Parameter                | Symbol            | Condition                         | Min                  | Typ  | Max                | Unit |    |
|--------------------------|-------------------|-----------------------------------|----------------------|------|--------------------|------|----|
| Power Supply Current *1  | I <sub>DD</sub>   | Normal mode (mode 5)              | 2.4 V                | —    | 10                 | 17   | mA |
|                          |                   |                                   | 5.5 V                | —    | 16                 | 33   |    |
|                          | I <sub>DDS1</sub> | Power Down mode 1                 | 5.5 V                | —    | 1.0                | 50   | μA |
|                          | I <sub>DDS2</sub> | Power Down mode 2                 | 2.4 V                | —    | 120                | 220  | mA |
|                          | I <sub>DDS3</sub> | Power Down mode 3                 |                      | —    | 5.3                | 9.2  |    |
| I <sub>DDS4</sub>        | Power Down mode 4 | —                                 | 6.0                  | 10.5 |                    |      |    |
| Input Leakage Current *2 | I <sub>IL</sub>   | V <sub>IN</sub> = 0 V             | -5.0                 | —    | 5.0                | μA   |    |
|                          | I <sub>IH</sub>   | V <sub>IN</sub> = V <sub>DD</sub> |                      |      |                    |      |    |
| Input Voltage *2         | V <sub>IL</sub>   | —                                 | 0                    | —    | 0.2V <sub>DD</sub> | V    |    |
|                          | V <sub>IH</sub>   |                                   | 0.8V <sub>DD</sub>   | —    | V <sub>DD</sub>    |      |    |
| Output Voltage *3        | V <sub>OL</sub>   | I <sub>OL</sub> = -20 μA          | 0                    | —    | 0.1                | V    |    |
|                          | V <sub>OH</sub>   | I <sub>OH</sub> = 20 μA           | V <sub>DD</sub> -0.1 | —    | V <sub>DD</sub>    |      |    |

\*1: Refer to PDN in the PIN AND FUNCTIONAL DESCRIPTIONS.

\*2: TVE, RVE, PDN, FDE, BYP, BR, EMP, VOL1, VOL2, PDRC, SD, BIT, FPS, RCK1, RCK2, SEC, ME

\*3: FD, RD, RT, ST

**MODEM AC Characteristics**

(V<sub>DD</sub> = 2.1 V to 5.5 V, T<sub>a</sub> = -30 to 70°C)

| Parameter                          | Symbol          | Condition   | Min   | Typ   | Max                  | Unit |   |
|------------------------------------|-----------------|---|-------|-------|----------------------|------|---|
| Transmit Carrier Frequency         | f <sub>M1</sub> | SD = "1"<br>BR = "0"  | 1199  | 1200  | 1201                 | Hz   |   |
|                                    | f <sub>S1</sub> | SD = "0"<br>ME = "1"  | 1799  | 1800  | 1801                 |      |   |
|                                    | f <sub>M2</sub> | SD = "1"<br>BR = "1"  | 1199  | 1200  | 1201                 |      |   |
|                                    | f <sub>S2</sub> | SD = "0"<br>ME = "1"  | 2399  | 2400  | 2401                 |      |   |
| Transmit Carrier Level             | V <sub>OX</sub> | R5 = R6   | -12.7 | -11.5 | -10.3                | dBV  |   |
| Receive Carrier Level              | V <sub>IR</sub> | V <sub>DD</sub> = 2.1 V to 5.5 V  | -30   | —     | -3                   |      |   |
|                                    |                 | V <sub>DD</sub> = 4.5 V to 5.5 V  | -30   | —     | +4                   |      |   |
| Bit Error Rate                     | 1200 bps        | S/N values measured at RAIO   | 8 dB  | —     | 1 × 10 <sup>-3</sup> | —    | — |
|                                    |                 |   | 10 dB | —     | 5 × 10 <sup>-5</sup> | —    |   |
|                                    | 2400 bps        |   | 11 dB | —     | 1 × 10 <sup>-3</sup> | —    |   |
|                                    |                 |   | 13 dB | —     | 5 × 10 <sup>-5</sup> | —    |   |
| Number of PLL Lock-in data bits *1 | B <sub>N</sub>  | Number of data bits required for the PLL to be Locked in within the phase difference of 22.5° or less | —     | —     | 18                   | bit  |   |
|                                    |                 | Number of data bits required for the PLL to be Locked in within the phase difference of 90° or less   | —     | —     | 11                   |      |   |

\*1: In the case where receive MSK signals are bit synchronous signals (modulated signals with the alternating pattern of "0" and "1")

Voice Signal Processing Characteristics

(V<sub>DD</sub> = 2.1 V to 5.5 V, T<sub>a</sub> = -30 to 70°C)

| Parameter                             | Symbol                | Condition  | Min       | Typ   | Max   | Unit  |    |
|---------------------------------------|-----------------------|--|-----------|-------|-------|-------|----|
| Limiter Clamp Level                   | V <sub>LIM</sub>      | R3 = R4, V <sub>DD</sub> = 2.4 V   | -16       | -15   | -14   | dBV   |    |
| Transmit Output Distortion            | H <sub>DT</sub>       | f <sub>IN</sub> = 1 kHz, -18 dBV   | —         | -48   | -40   | dB    |    |
| Receive Output Distortion             | H <sub>DR</sub>       | BYP = EMP = "0", R7 = R8   | —         | -45   | -38   |       |    |
| Transmit Idle Noise                   | N <sub>IT</sub>       | BYP = EMP = "0"  | —         | -62   | -52   | dBV   |    |
| Receive Idle Noise                    | N <sub>IR</sub>       | R7 = R8  | —         | -80   | —     |       |    |
| Crosstalk                             | (Receive to transmit) | C <sub>TT</sub>  | —         | -60   | -50   |       |    |
|                                       | (Transmit to receive) | C <sub>TR</sub>  | —         | -90   | —     |       |    |
| Transmit Gain                         | G <sub>T1</sub>       | f <sub>IN</sub> = 1 kHz<br>BYP = "1"   | SEC = "0" | -1.5  | 0     | +1    | dB |
|                                       | G <sub>T2</sub>       |  | SEC = "1" | -1.5  | 0     | +1    |    |
| Receive Gain                          | G <sub>R1</sub>       |  | SEC = "0" | -1.5  | 0     | +1    |    |
|                                       | G <sub>R2</sub>       |  | SEC = "1" | -1.5  | 0     | +1    |    |
| Reverse Frequency of Voice Scrambler  | f <sub>R</sub>        | Common to transmit and receive   | 3200 Hz   | 3197  | 3200  | 3203  | Hz |
|                                       |                       |  | 3291 Hz   | 3288  | 3291  | 3294  |    |
|                                       |                       |  | 3388 Hz   | 3385  | 3388  | 3391  |    |
| Transmit Reverse Frequency Leak Level | L <sub>RT</sub>       | No signal input<br>BYP = RCK2 = "0"<br>SEC = RCK1 = "1"<br>R7 = R8                   | —         | -88   | -60   | dBV   |    |
| Receive Reverse Frequency Leak Level  | L <sub>RR</sub>       |  | —         | -110  | —     |       |    |
| Transmit Input Signal Leak Level      | L <sub>IT</sub>       | f <sub>IN</sub> = 1 kHz, -15 dBV<br>BYP = RCK2 = "0"<br>SEC = RCK1 = "1", R7 = R8    | —         | -55   | -48   |       |    |
| Receive Input Signal Leak Level       | L <sub>IR</sub>       |  | —         | -55   | -48   |       |    |
| Transmit Filter                       | FT1                   | EMP = "1"<br>BYP = "1"<br>SEC = "0"<br>RCK1 = "0"<br>RCK2 = "0"<br>Reference = 1 kHz | 100 Hz    | —     | -28   | -23   | dB |
|                                       | FT3                   |  | 300 Hz    | -12.5 | -10.5 | -8.5  |    |
|                                       | FT25                  |  | 2.5 kHz   | +6.5  | +8.0  | +9.5  |    |
|                                       | FT30                  |  | 3 kHz     | +7    | +9    | +11   |    |
|                                       | FT50                  |  | 5 kHz     | —     | -32   | -27   |    |
| Receive Filter                        | FR1                   | Reference = 1 kHz  | 100 Hz    | +1.0  | +2.5  | +4.0  |    |
|                                       | FR3                   |  | 300 Hz    | +7.5  | +9.0  | +10.5 |    |
|                                       | FR25                  |  | 2.5 kHz   | -9.5  | -8.0  | -6.5  |    |
|                                       | FR30                  |  | 3 kHz     | -11.5 | -9.5  | -7.5  |    |
|                                       | FR50                  |  | 5 kHz     | —     | -35   | -30   |    |



**Voice Signal Processing Characteristics (Continued)**

( $V_{DD} = 2.1\text{ V to }5.5\text{ V}$ ,  $T_a = -30\text{ to }70^\circ\text{C}$ )

| Parameter                             |                                 | Symbol   | Condition   | Min                                     | Typ   | Max   | Unit      |     |
|---------------------------------------|---------------------------------|--|---|---|-------|-------|-----------|-----|
| Ceramic Receiver Amplifier (RCP, RCN) | Output Resistance               | $R_{OC}$   | —   | —                                       | 40    | —     | $\Omega$  |     |
|                                       | Output Load Resistance          | $R_{LC}$   |   | 1.35                                    | 1.5   | —     | $k\Omega$ |     |
|                                       | Receiver Equivalent Capacitance | $C_{CR}$   |   | —                                       | 68    | 75    | nF        |     |
|                                       | Output Level                    | $V_{CR}$   | $f_{IN} = 1\text{ kHz}$ , Distortion Ratio $\leq -30\text{ dB}$ , $V_{DD} = 2.4\text{ V}$ | —                                       | —     | -4    | dBV       |     |
|                                       | Output Distortion               | $H_{DC}$   | $f_{IN} = 1\text{ kHz}$ , $-18\text{ dBV}$  | —                                       | -68   | -45   | dB        |     |
| User-Available Amplifier (UAO)        | Output Resistance               | $R_{OU}$   | —   | —                                       | 40    | —     | $\Omega$  |     |
|                                       | Output Load Resistance          | $R_{LU}$   |   | 2                                       | —     | —     | $k\Omega$ |     |
|                                       | Output Level                    | $V_{OU}$   | Distortion Ratio $\leq -30\text{ dB}$   | $V_{DD} = 2.1\text{ V to }5.5\text{ V}$ | —     | —     | -6        | dBV |
|                                       |                                 |  |   | $V_{DD} = 4.5\text{ V to }5.5\text{ V}$ | —     | —     | 0         |     |
| Output Distortion Ratio               | $H_{DU}$                        | $f_{IN} = 1\text{ kHz}$ , $-18\text{ dBV}$               | —   | -64                                     | -45   | dB    |           |     |
| Compressor                            | Input Reference Level           | $V_{ICS}$  | $f_{IN} = 1\text{ kHz}$ , $R7 = R8$   | -19.8                                   | -17.8 | -15.8 | dBV       |     |
|                                       | Output Level *1                 | GC2  | $f_{IN} = 1\text{ kHz}$ , $R7 = R8$   | -20 dB                                  | -10.7 | -10   | -9.3      | dB  |
|                                       |                                 | GC4  |   | -40 dB                                  | -21.2 | -20   | -18.8     |     |
|                                       |                                 | GC6  |   | -60 dB                                  | —     | -30   | —         |     |
|                                       | Attack Time                     | $T_{AT1}$  | Input Level, $-34\text{ dBV} \rightarrow -22\text{ dBV}$                                  | —                                       | 3.0   | —     | ms        |     |
| Recovery Time                         | $T_{RE1}$                       | Input Level, $-22\text{ dBV} \rightarrow -34\text{ dBV}$ | —   | 16                                      | —     |       |           |     |
| Expander                              | Input Reference Level           | $V_{IES}$  | $f_{IN} = 1\text{ kHz}$ , $R7 = R8$   | -19.8                                   | -17.8 | -15.8 | dBV       |     |
|                                       | Maximum Input Level             | $V_{IEM1}$   | $R7 = R8$   | $V_{DD} = 2.1\text{ V to }5.5\text{ V}$ | —     | —     |           | -15 |
|                                       |                                 | $V_{IEM2}$   |   | $V_{DD} = 4.5\text{ V to }5.5\text{ V}$ | —     | —     | -12       |     |
|                                       | Output Level *1                 | GE1  | $f_{IN} = 1\text{ kHz}$ , $R7 = R8$   | -10 dB                                  | -21.5 | -20   | -18.5     | dB  |
|                                       |                                 | GE2  |   | -20 dB                                  | -42.2 | -40   | -37.8     |     |
|                                       |                                 | GE25   |   | -25 dB                                  | —     | -50   | —         |     |
| Attack Time                           | $T_{AT2}$                       | Input Level, $-26\text{ dBV} \rightarrow -20\text{ dBV}$ | —   | 3.0                                     | —     | ms    |           |     |
| Recovery Time                         | $T_{RE2}$                       | Input Level, $-20\text{ dBV} \rightarrow -26\text{ dBV}$ | —   | 16                                      | —     |       |           |     |
| Electronic Volume Gain                | GEV1                            | $VOL1 = VOL2 = "0"$<br>Referenced to RVO<br>level at "0" | +6 dB   | +5.5                                    | +6.0  | +6.5  | dB        |     |
|                                       | GEV2                            |  | -6 dB   | -6.5                                    | -6.0  | -5.5  |           |     |
|                                       | GEV3                            |  | -12 dB  | -12.5                                   | -12.0 | -11.5 |           |     |

\*1: 0 dB is defined as the input level and the output level when the standard input level is input.

**Common Characteristics**

(V<sub>DD</sub> = 2.1 V to 5.5 V, T<sub>a</sub> = -30 to 70°C)

| Parameter                          | Symbol           | Condition   | Min                              | Typ                | Max                         | Unit |     |
|------------------------------------|------------------|---|----------------------------------|--------------------|-----------------------------|------|-----|
| Input Resistance                   | R <sub>IA</sub>  | *1  | —                                | 10                 | —                           | MΩ   |     |
| Output Resistance                  | R <sub>OX</sub>  | f <sub>0</sub> ≤ 4 kHz, *2  | —                                | 200                | —                           | Ω    |     |
| Output Load Resistance             | R <sub>LX1</sub> | Output Level:<br>less than -12 dBV  | *3                               | 10                 | —                           | —    | kΩ  |
|                                    | R <sub>LX2</sub> | Output Level:<br>within the range of<br>V <sub>01</sub> and V <sub>02</sub> |                                  | 40                 | —                           | —    |     |
|                                    | R <sub>LX3</sub> | V <sub>REF</sub> , SGO  |                                  | 12                 | —                           | —    |     |
| Analog Signal Output Level         | V <sub>01</sub>  | R <sub>LX2</sub> = 40 kΩ *3   | V <sub>DD</sub> = 2.1 V to 5.5 V | —                  | —                           | -6   | dBV |
|                                    | V <sub>02</sub>  |   | V <sub>DD</sub> = 4.5 V to 5.5 V | —                  | —                           | 0    |     |
| V <sub>REF</sub> Output DC Voltage | V <sub>RF</sub>  | With respect to V <sub>SG</sub>   | 0.45                             | 0.5                | 0.55                        | V    |     |
| SG Output DC Potential             | V <sub>SG</sub>  | SGO, SGI  | V <sub>DD</sub> /2<br>-0.1       | V <sub>DD</sub> /2 | V <sub>DD</sub> /2<br>+0.1  |      |     |
| Analog Output DC Potential         | V <sub>AO</sub>  | TAO, RVO  | V <sub>DD</sub> /2<br>-0.15      | V <sub>DD</sub> /2 | V <sub>DD</sub> /2<br>+0.15 |      |     |

\*1: On TVI, MICN, MICP, UAI, MODL, LIML, CPDL, RAI, RVBU

\*2: On TVIO, MICO, TAO, RAI0, RVO

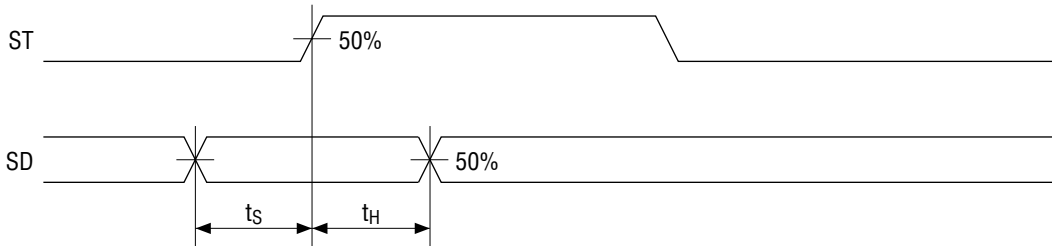
\*3: When the distortion ratio is less than or equal to -30 dB on TVIO, MICO, TAO, RAI0, RVO

**Digital Timing Characteristics**

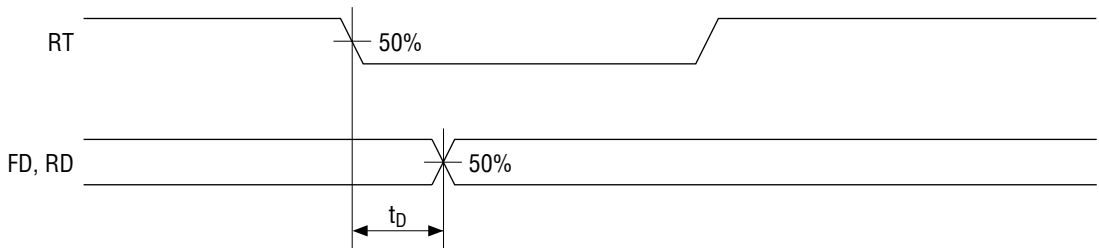
(V<sub>DD</sub> = 2.1 V to 5.5 V, T<sub>a</sub> = -30 to 70°C)

| Parameter                         | Symbol          | Condition                      | Min  | Typ | Max | Unit |
|-----------------------------------|-----------------|--------------------------------|------|-----|-----|------|
| Data Setup Time                   | t <sub>S</sub>  | Refer to Fig. 1                | 1    | —   | —   | μs   |
| Data Hold Time                    | t <sub>H</sub>  |                                | 1    | —   | —   |      |
| Receive Data Output (RT→RD, FD)   | t <sub>D</sub>  | Refer to Fig. 2                | -300 | —   | 300 | ns   |
| Synchronous Signal Output (ME→ST) | t <sub>MS</sub> | Refer to SD<br>pin description | 0    | —   | 834 | μs   |

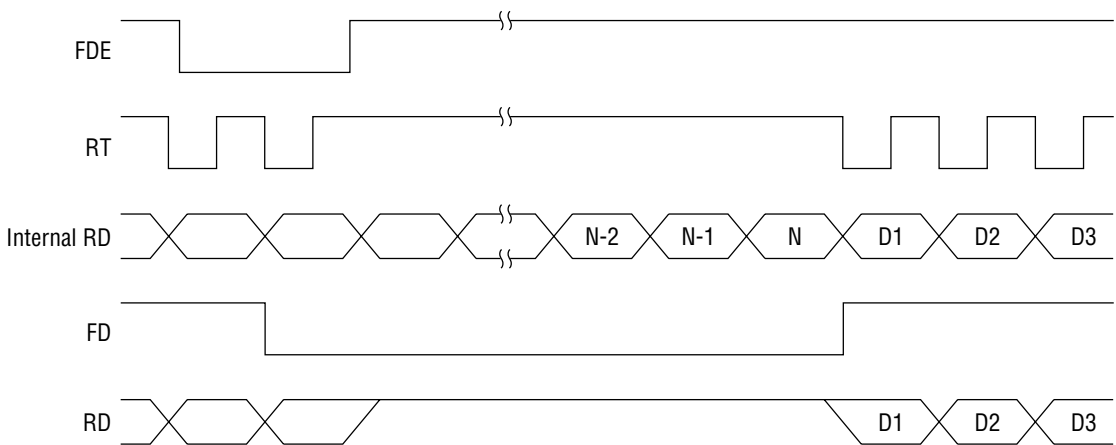
**TIMING DIAGRAM**



**Figure 1 Input Data Timing**



**Figure 2 Output Data Timing**



N-2, N-1, N : Frame synchronous signal

**Figure 3 Receive Signal Timing**

APPLICATION CIRCUIT

