OKI Semiconductor
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MSM7580

ITU-T G.721 ADPCM TRANSCODER

GENERAL DESCRIPTION

The MSM7580 is an ADPCM transcoder which is used by the new digital cordless system. It converts 64 kbps voice PCM serial data to 32 kbps ITU-T G.721 ADPCM serial data, and vice versa.

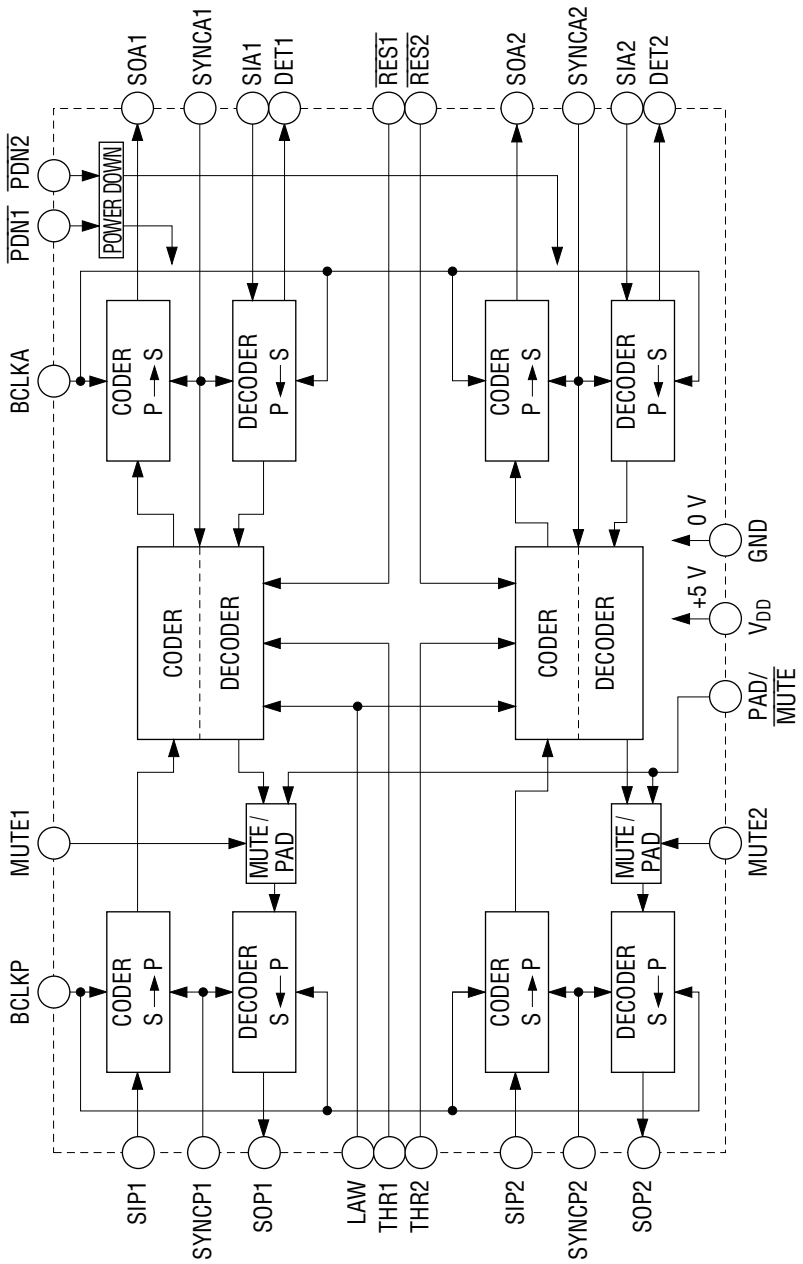
This device consists of two systems with full-duplex voice data channels and a data-through mode.

The MSM7580 provides cost effective solutions for digital cordless office telephone systems which are incorporated into PABXs and for the public base stations which are connected to the central office through digital PSTNs.

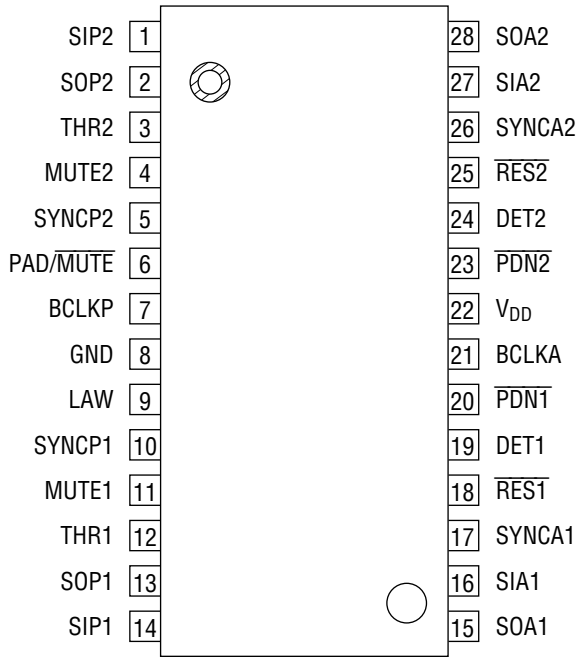
FEATURES

- Conforms to ITU-T G.721
- Built-in Full-duplex Transcoder with Two Data channels
- PCM companding Law: A-law/μ-law selectable
- Synchronized Operation between coder and decoder, and between two channels.
- Serial PCM Data Transmission Speed: 64 kbps to 2048 kbps
- Serial ADPCM Data Transmission Speed: 32 kbps to 2048 kbps
- Hardware Reset – ITU-T G.721 Optional Reset – for each channel
- Power Down Control for each channel
- Decoder (ADPCM → PCM) MUTE Mode and PAD Mode for each channel
- ADPCM Data-through Mode
- Capable of time slot conversion
- Special ADPCM Input Data Code (”0000”) Detector for each channel
- Master Clock Signal : Not necessary
- Power supply voltage/Consumption current :
  +5 V ±10%, 2.5 mA/channel
- Package :
  28-pin plastic SOP (SOP28-P-430-1.27-K) (Product name : MSM7580GS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



28-Pin Plastic SOP

PIN AND FUNCTIONAL DESCRIPTIONS

GND

Ground, 0 V.

SIP1, SOP1

PCM serial data input (SIP1) and output (SOP1) for Channel 1.
SOP1 is an open-drain output, which goes into a high impedance state after a continuous 8-bit serial data output.

SIP2, SOP2

PCM serial data input (SIP2) and output (SOP2) for Channel 2.
SOP2 is an open-drain output, which goes into a high impedance state after a continuous 8-bit serial data output.

PAD/ $\overline{\text{MUTE}}$

Control input for the selection of PAD or MUTE mode.
When digital "1" is input, the PAD mode is selected and when digital "0" is input, the MUTE mode is selected.

THR1, THR2

Control pins for the data through modes.
THR1 and THR2 are for Channel 1 and Channel 2, respectively. The data-through mode is selected when digital "1" is applied to THR1 and THR2. In this mode, 8-bit serial input data applied to SIA1 and SIA2 (ADPCM data input) is passed to the PCM serial data output pins, SOP1 and SOP2, without any data modification. SOP1 and SOP2 go to the high impedance state after the output of 8-bit data has been applied to SIA1 and SIA2.
Conversely 8-bit serial input data applied to SIP1 and SIP2 (PCM data input) is passed to ADPCM serial data output pins, SOA1 and SOA2, without any data modification.
SOA1 and SOA2 go to the high impedance state after the output of 8-bit data has been applied to SIP1 and SIP2.
Since ADPCM and PCM data interfaces have the mutually independent signal input pins for synchronizing signals the time slots for data input and output can be exchanged between them. Some timing at which data may be deleted or duplicated as described in "Notes on Usage" should not be used.

MUTE1, MUTE2

Setting a digital "1"at these pins sets the PCM output to the idle pattern state regardless of the ADPCM input data, when the MUTE mode is selected by the PAD/$\overline{\text{MUTE}}$ pin.
When the PAD mode is selected, the PCM output has a 12 dB loss.
Normally, these pins are set to a digital "0".
When the data through mode is selected, the function of these pins is invalid.

SYNCP1, SYNCP2

Synchronous signal input.
SYNCP1 and SYNCP2 control the PCM data input/output timing for Channel 1 (SIP1, SOP1) and Channel 2 (SIP2, SOP2), respectively.
Since other synchronous signal input pins SYNCA1 and SYNCA 2 for ADPCM interfaces are also provided, the PCM and ADPCM data can be input or output with different timing.
PCM and ADPCM data interfaces can be used at a mutually independent timing except same timing.

Note: When PCM and ADPCM data interfaces are used at a mutually independent timing, the timing described in "Notes on Usage" should not be used.

BCLKP

Bit clock input.
This signal defines the PCM data transmission speed at the PCM data input/output pins.
BCLKP is used for Channels 1 and 2. Since BCLKA defines the data rate of the ADPCM data interface, the PCM and ADPCM data can be input or output at different speeds.

LAW

PCM data companding law (A-law/μ-law) selection.
Digital "1" and "0" correspond to A-law and μ-law, respectively.

$\overline{\text{PDN1}}$, $\overline{\text{PDN2}}$

Power down mode selection.
$\overline{\text{PDN1}}$ and $\overline{\text{PDN2}}$ can be independently set to power down mode. When a digital "0" is applied, these pins are in the power-down mode.

SIA1, SOA1

ADPCM serial data input (SIA1) and output (SOA1) pins for Channel 1.
SOA1 is an open-drain pin and enters to the high impedance state after outputting a continuous 4-bit serial data stream. When the data-through mode is selected, SOA1 enters to the high impedance state after outputting an 8-bit serial data stream.

SIA2, SOA2

ADPCM serial data input (SIA2) and output (SOA2) pins for Channel 2.
These pins function the same as SIA1 and SOA1.

SYNCA1 , SYNCA2

Synchronous signal input pins.
SYNCA1 and SYNCA 2 control the ADPCM data input/output timing for Channel 1 (SIA1, SOA1) and Channel 2 (SIA2, SOA2), respectivery.
The ADPCM data can be input or output with timing other than the PCM data interface.
Therefore PCM and ADPCM interfaces can be used at a mutually independent timing except some timing.
Since master clocks are generated by the internal PLL using SYNCA, a synchronous signal should be input to there pins.

Note: When PCM and ADPCM data interfaces are used at a mutually independent timing, the timing described in "Notes on Usage" should not be used.

DET1, DET2

Special ADPCM input data pattern detect pins.
When a 4-bit continuous "0" pattern at the ADPCM input pins Channel 1 (STA1) and Channel 2 (SIA2) is detected, DET1 and DET2 go from a digital "0" to a digital "1" state.
A digital "1" is output at the rising edge of the clock.
The fourth data bit (LSB) is clocked into the register by the bit clock (BCLKA) and the held there until the rising edge in the next time frame.
When detecting the special data pattern in the next time frame, the digital "1" on the pins DET (1, 2) is remains. When the THR1 pin or THR2 pin is at digital "1" level, the functions of these pins are invalid.

$\overline{\text{RES1}}$, $\overline{\text{RES2}}$

Algorithm reset signal input pins for Channel 1 ($\overline{\text{RES1}}$) and Channel 2 ($\overline{\text{RES2}}$).
When a digital “0” is applied, the entire transcoder goes to its initial state.
This reset is defined by ITU-T G.721 and is an optional reset.

BCLKA

Bit clock input pin used to define the data transmission speed at the ADPCM interface.
This pin can be used for Channels 1 and 2, which allows the ADPCM data interface speed to be defined differently than the PCM data interface speed.

V_{DD}

Power supply.
The device must operate at +5 V ±10%.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	0 to 7	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	4.5	—	5.5	V
Operating Temperature	Ta	—	–30	+25	+80	°C
Digital Input High Voltage	V_{IH}	All Digital Input Pins	2.2	—	V_{DD}	V
Digital Input Low Voltage	V_{IL}		0	—	0.6	V
Bit Clock Frequency	F_{BCLKA}	BCLKA	32	—	2048	kHz
	F_{BCLKP}	BCLKP	64	—	2048	kHz
Synchronous Signal Frequency	F_{SYNC}	SYNCP1, SYNCP2, SYNCA1, SYNCA2	—	8.0	—	kHz
Clock Duty Ratio	D_C	BCLKA, BCLKP	30	50	70	%
Digital Input Rise Time	t_{Ir}	All Digital Input Pins	—	—	50	ns
Digital Input Fall Time	t_{If}		—	—	50	ns
Synchronous Signal Timing CODER	t_{XS}	BCLKA, BCLKP to SYNCP	100	—	—	ns
	t_{SX}	SYNCP to BCLKA, BCLKP	100	—	—	ns
Synchronous Signal Timing DECODER	t_{SX}	BCLKA, BCLKP to SYNCA	100	—	—	ns
	t_{SR}	SYNCA to BCLKA, BCLKP	100	—	—	ns
Synchronous Signal Width	t_{WS}	SYNCP1, SYNCP2, SYNCA1, SYNCA2	1 BCLK	—	100	µs
Data Set-up Time	t_{DS}	—	100	—	—	ns
Data Hold Time	t_{DH}	—	100	—	—	ns
Digital Output Load	R_{DL}	SOP1, SOP2, SOA1, SOA2 (Pull-up Resistor)	500	—	—	Ω
	C_{DL}	SOP1, SOP2, SOA1, SOA2, DET1, DET2	—	—	100	pF

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 4.5 V to 5.5 V, Ta = –30°C to +80°C)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Power Supply Current	I_{DD1}	Power On Mode: 2 Channels	—	5	10	mA
	I_{DD2}	Power Down Mode: 2 Channels	—	0.1	0.2	mA
Input High Voltage	V_{IH}	—	2.2	—	V_{DD}	V
Input Low Voltage	V_{IL}	—	0.0	—	0.6	V
Input Leakage Current	I_{IH}	$V_I = V_{DD}$	—	—	2.0	µA
	I_{IL}	V_I = 0 V	—	—	0.5	µA
Digital Output High Voltage	V_{OH}	DET1, DET2 : I_{OH} = –0.4 mA	2.8	—	V_{DD}	V
Digital Output Low Voltage	V_{OL1}	1 LSTTL, Pull-up : 500 Ω	0.0	0.2	0.4	V
	V_{OL2}	DET1, DET2 : I_{OL} = 1.6 mA	0.0	0.2	0.4	V
Output Leakage Current	I_{OL}	SOP1, SOP2, SOA1, SOA2	—	—	10	µA
Input Capacitance	C_{IN}	—	—	5	—	pF

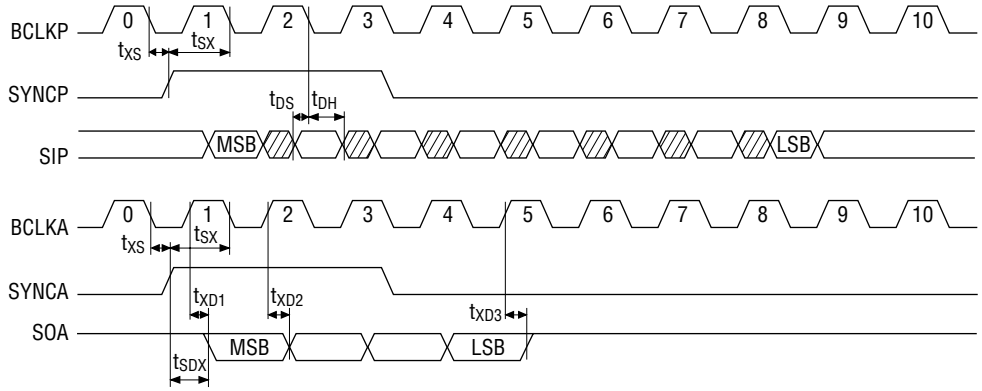
AC Characteristics

(V_{DD} = 4.5 V to 5.5 V,Ta = –30°C to +80°C)

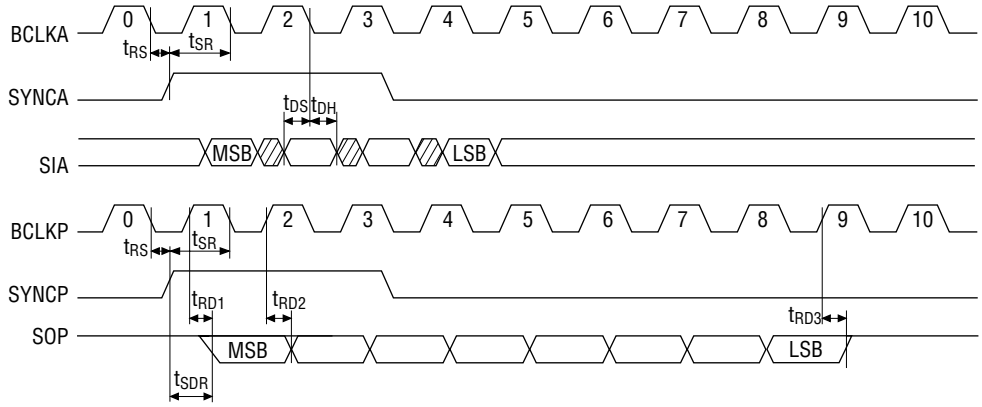
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital Output Delay Time	t_{SDX}	1 LSTTL + 100 pF Pull-up: 500 Ω	0	—	200	ns
	t_{SDR}		0	—	200	ns
	t_{XD1}, t_{RD1}		0	—	200	ns
	t_{XD2}, t_{RD2}		0	—	200	ns
	t_{XD3}, t_{RD3}		0	—	200	ns
	t_{DD1}		0	—	200	ns
	t_{DD2}		0	—	200	ns

TIMING DIAGRAM

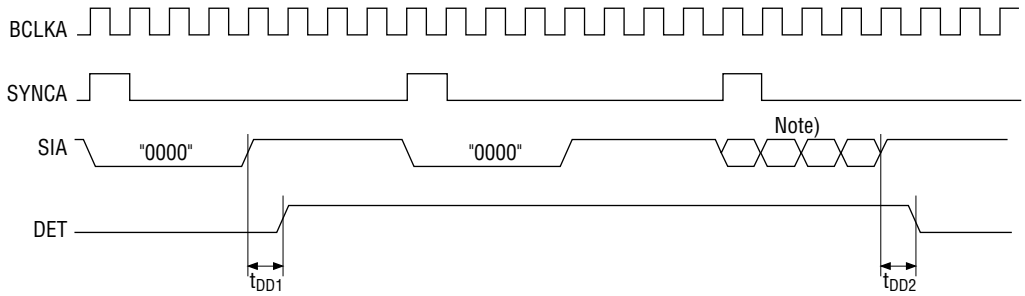
CODER



DECODER

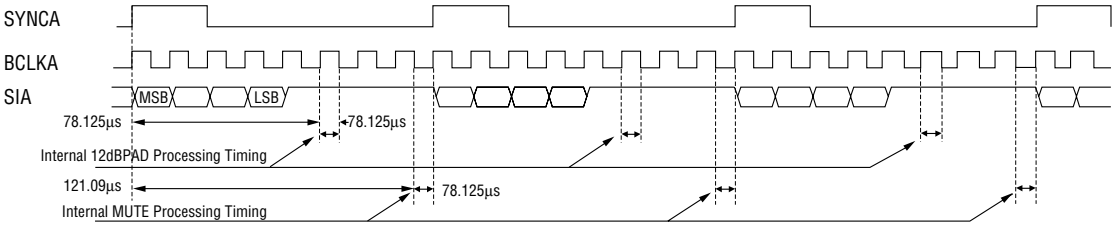


DET ("0000" detection) Output Timing

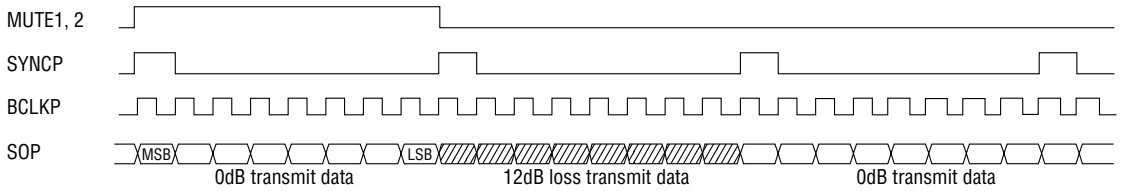


Note: 4-bit data pattern except "0000"

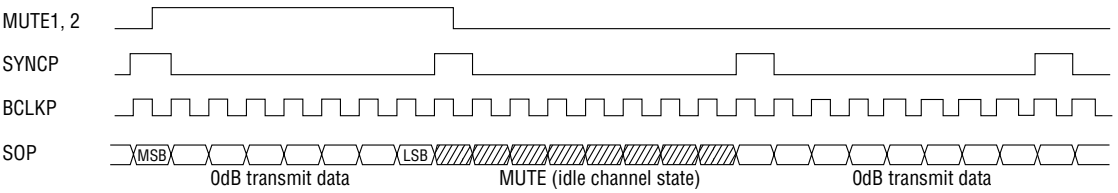
PAD/MUTE Processing Timing



PAD Mode; MUTE1 and MUTE 2 Timings PAD/MUTE="H"



MUTE Mode; MUTE1 and MUTE 2 Timings PAD/MUTE="L"

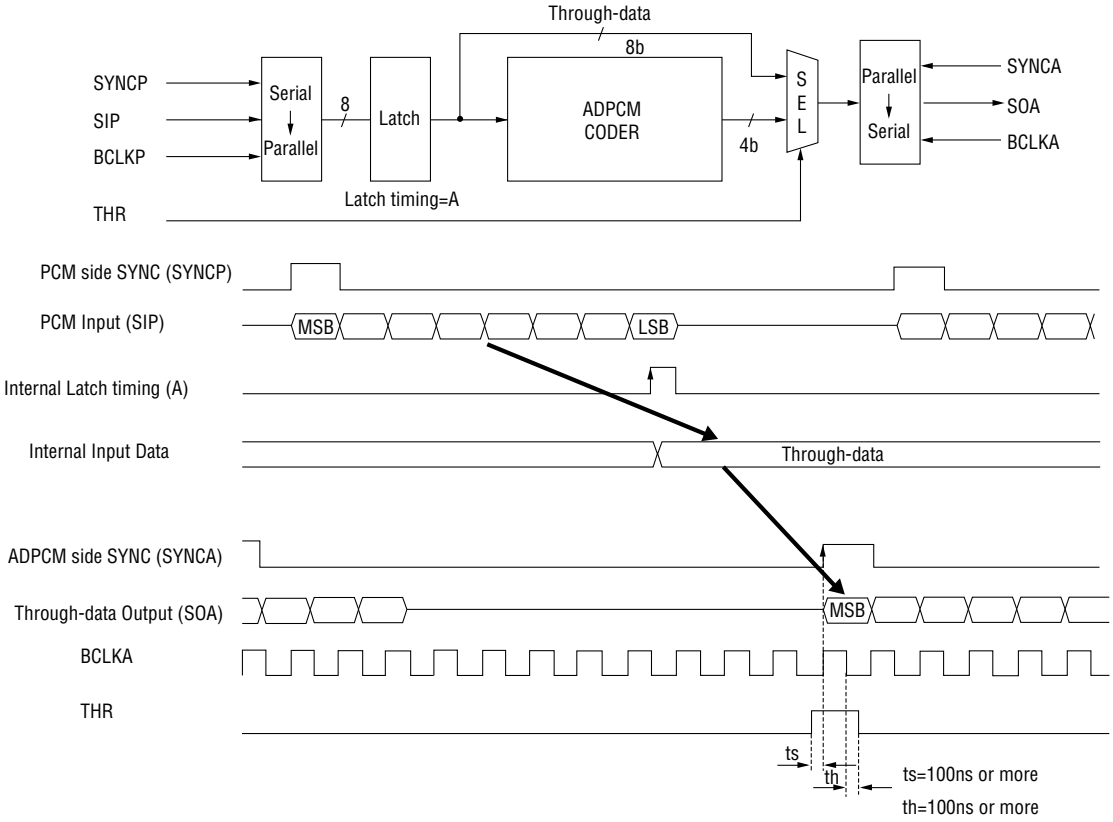


As mentioned above, PAD and MUTE processings are carried out according to the rising edge of SYNCA.
Even if BCLK is not 128 kHz, these processings are performed in the absolute time counted from the rising edge of SYNCA.
Therefore, MUTE1 and MUTE 2 pins must be controlled so as to cover there processsings.

THR Processing Timing

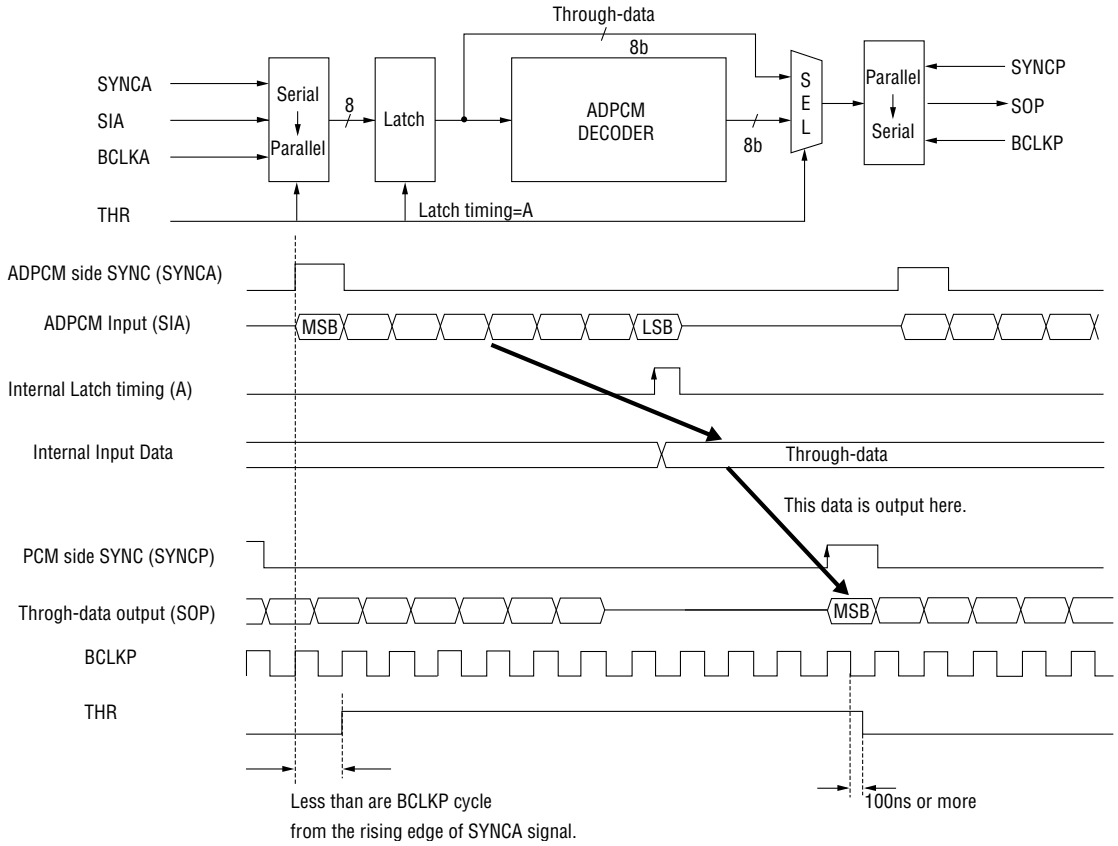
Timing Block Diagrams, when CODER and DECODER output data, are shown in the following figures.
The parallel to serial conversion of the output unit employs a load format and the load point is at the rising edge of a synchronous signal.
Therefore, input THR signal with respect to SYNCA for CODER with timing of satisfying ts and th conditions shown in the figure.
For DECODER, THR signal should be input even when through-data is input.
The input timing should satisfy the conditions shown in the following figures.

CODER

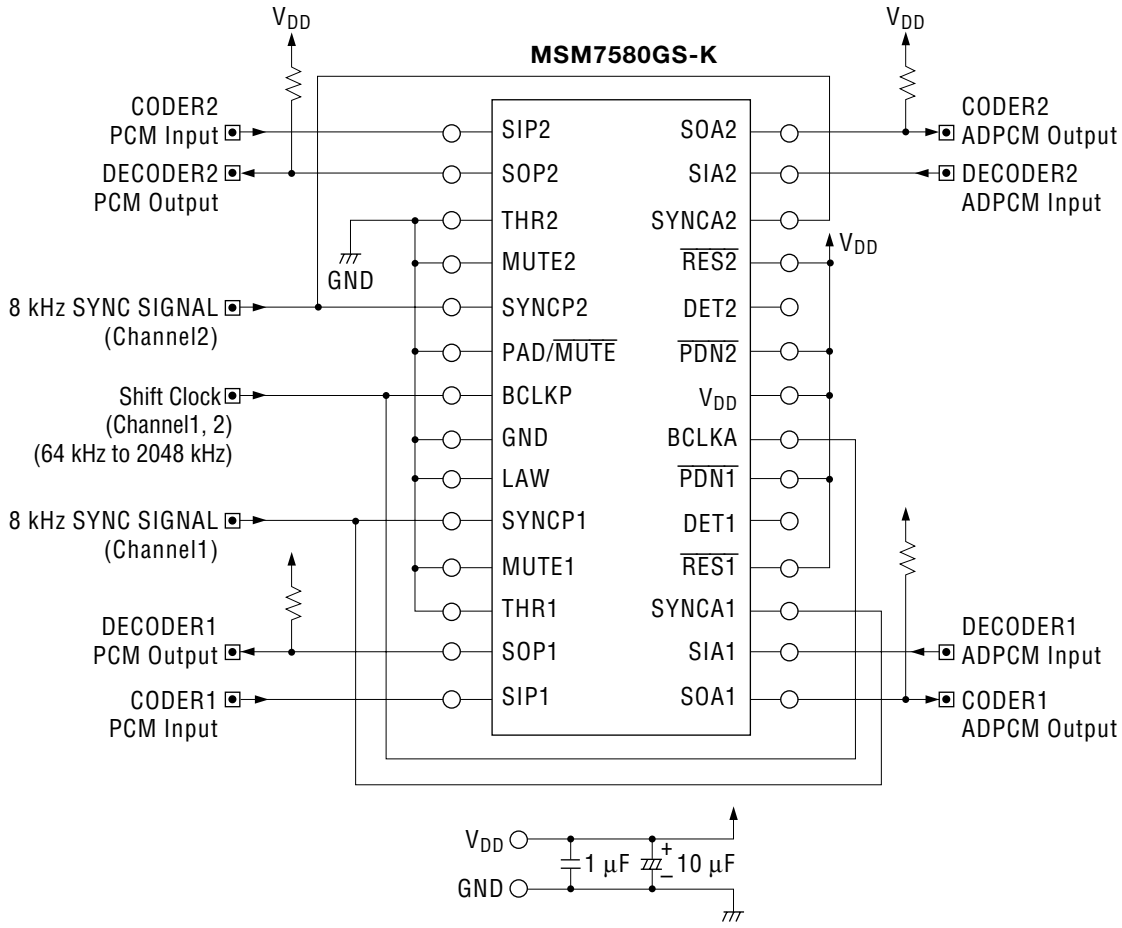


Note: That data-ship may occur when the rising edge (data load point) of SYNCA and input of the internal latch timing overlap each other.

DECODER

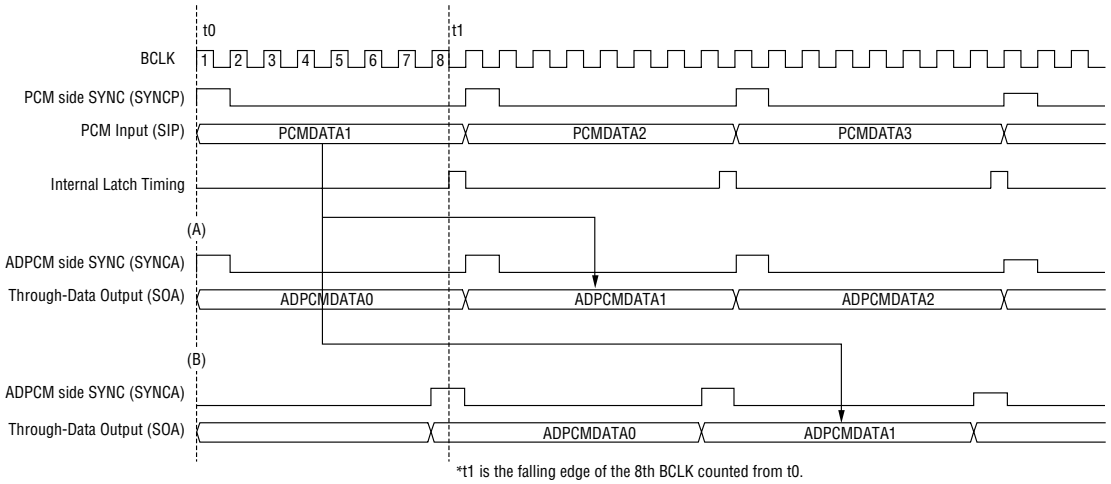

Through-data
8b
SYNCA
SIA
BCLKA
Serial
Parallel
8
Latch
ADPCM
DECODER
8b
S
E
L
Parallel
Serial
SYNCP
SOP
BCLKP
THR
Latch timing=A
ADPCM side SYNC (SYNCA)
ADPCM Input (SIA)
MSB
LSB
Internal Latch timing (A)
Internal Input Data
Through-data
This data is output here.
PCM side SYNC (SYNCP)
Throgh-data output (SOP)
MSB
BCLKP
THR
Less than are BCLKP cycle
from the rising edge of SYNCA signal.
100ns or more

APPLICATION CIRCUIT



NOTES ON USAGE

(1) Through Mode (CODER Side)

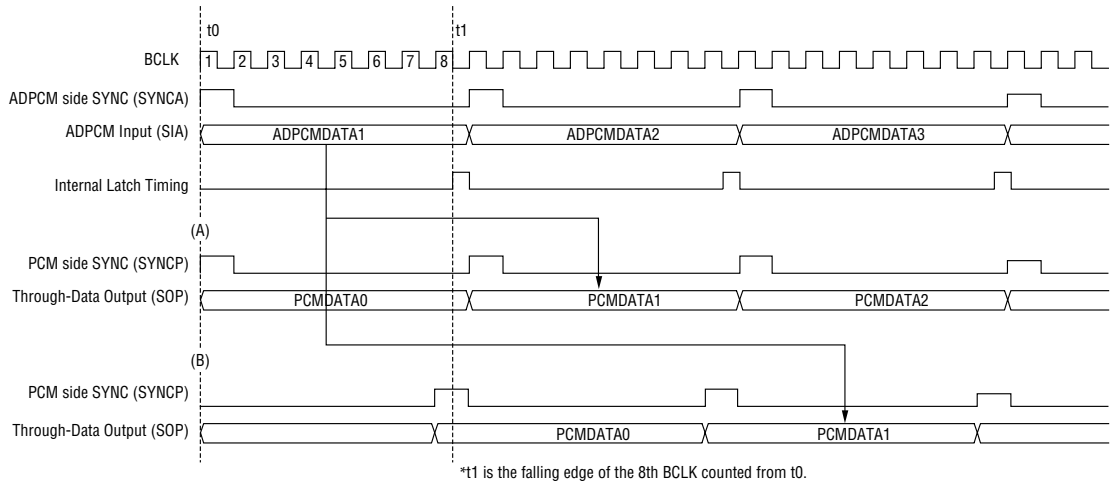


*t1 is the falling edge of the 8th BCLK counted from t0.

(A) When SYNCA rises after t1, PCMDATA1 is output to ADPCMDATA1.
(B) When SYNCA rises before t1, PCMDATA1 is output to ADPCMDATA1.

If SYNCA rises near the t1 and jitter occurs, data slip may occur. Therefore SYNCA should not rise in the range of ±500ns from t1.
Data slip means that data is deleted or the same data is output twice.

(2) Through Mode (DECODER Side)



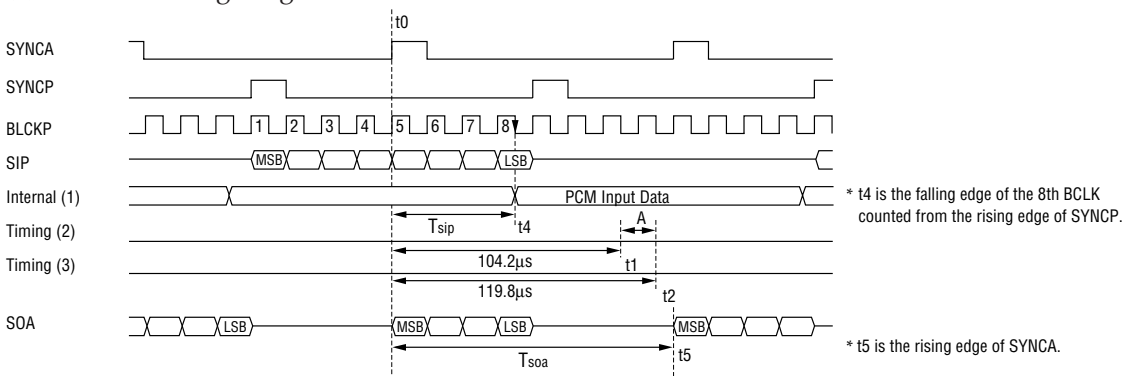
*t1 is the falling edge of the 8th BCLK counted from t0.

(A) When SYNCA rises after t1, ADPCMDATA1 is output to PCMDATA1.
(B) When SYNCA rises before t1, ADPCMDATA1 is output to PCMDATA1.

If SYNCP rises near the t1 and jitter occurs, data slip may occur. Therefore SYNCA should not rise in the range of ±500ns from t1.
Data slip means that data is deleted or the same data is output twice.

(3) PCM→ADPCM, ADPCM→PCM during Transcode

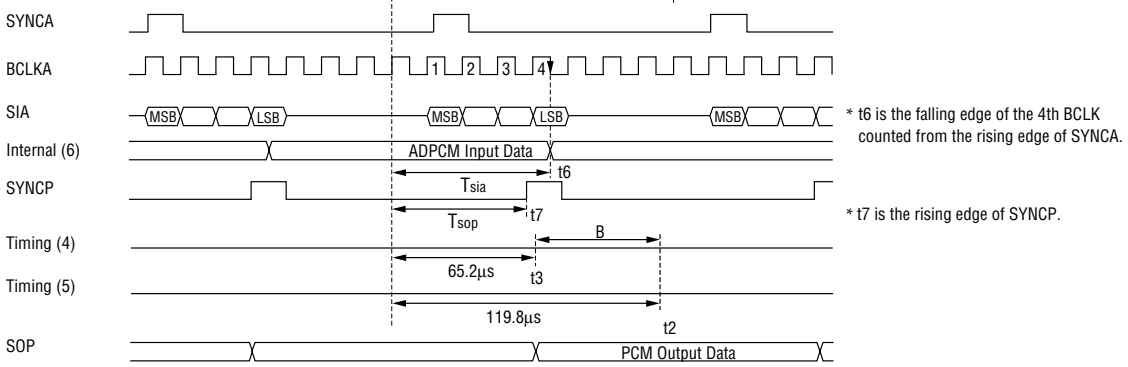
(a) CODER Timing Diagram



* t4 is the falling edge of the 8th BCLK counted from the rising edge of SYNCP.

* t5 is the rising edge of SYNCA.

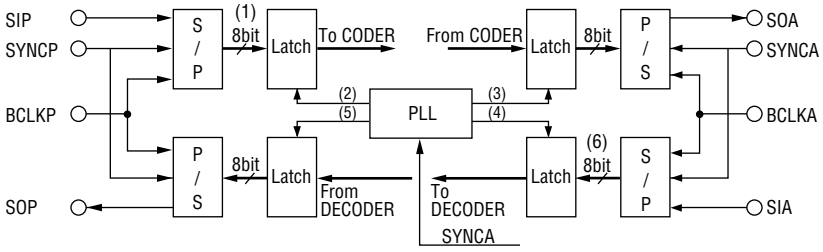
(b) DECODER Timing Diagram



* t6 is the falling edge of the 4th BCLK counted from the rising edge of SYNCA.

* t7 is the rising edge of SYNCP.

(c) Internal Circuit Configuration

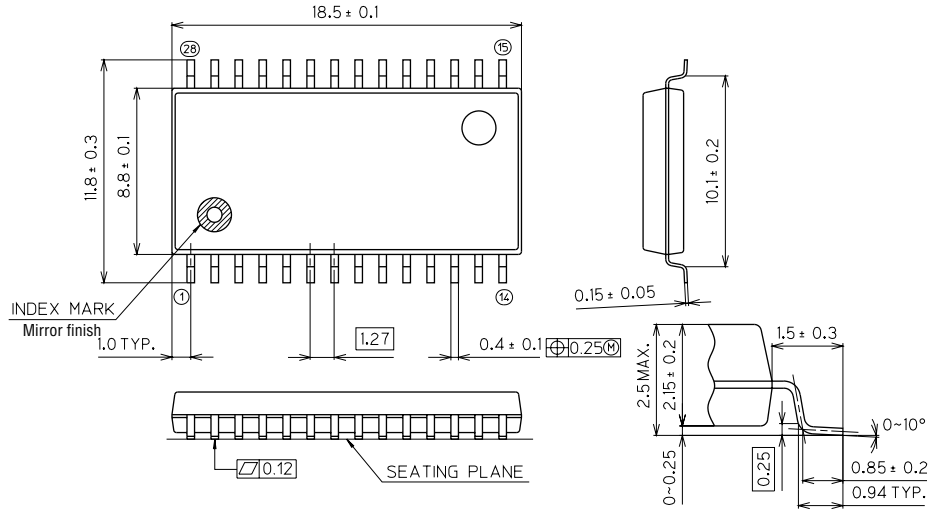


In this device, internal operating signals are generated according to the ADPCM side SYNC (SYNCA) signal.
The timings are shouwn in the figures (a) and (b);
The arithmetic operation of CODER is performed at "A" in the figure (a).
The arithmetic operation of DECODER is performed at "B" in the figure (b).
Therefore, when the conversion delay time Tsip of the CODER is less than t1, ADPCM is output at the timing of Tsoa.
When Tsip is more than t1, ADPCM is output at the timing of Tsoa + 125µs.
For DECODER, when Tsia<t3 and Tsop<t2, the conversion delay time is Tsop-Tsia.
As mentioned above, a data ship may occur at Tsip=t1 in CODER, and at Tsia=t3 and Tsop=t2 in DECODER.
Therefore, the timings of SYNC signals of both PCM and ADPCM sides should not be set up in the range about ±500nsec of Tsip=t1, Tsia=t3 and Tsop=t2.
For normal operation, SYNC clocks for ADPCM and PCM sides should be continuous at 8 kHz and synchronized with each other even if their phases are different.

PACKAGE DIMENSIONS

(Unit : mm)

SOP28-P-430-1.27-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.75 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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