Features

- 32-Mbit Flash and 4-Mbit/8-Mbit SRAM
- Single 66-ball (8 mm x 11 mm x 1.2 mm) CBGA Package
- 2.7V to 3.3V Operating Voltage

Flash

- 2.7V to 3.3V Read/Write
- Access Time – 85 ns
- Sector Erase Architecture
  - Sixty-three 32K Word (64K Byte) Sectors with Individual Write Lockout
  - Eight 4K Word (8K Byte) Sectors with Individual Write Lockout
- Fast Word Program Time – 20 µs
- Fast Sector Erase Time – 200 ms
- Suspend/Resume Feature for Erase and Program
  - Supports Reading and Programming from Any Sector by Suspending Erase of a Different Sector
  - Supports Reading Any Word by Suspending Programming of Any Other Word
- Low-power Operation
  - 25 mA Active
  - 10 µA Standby
- $\overline{\text{Data}}$ Polling, Toggle Bit, Ready/$\overline{\text{Busy}}$ for End of Program Detection
- VPP Pin for Write Protection and Accelerated Program/Erase Operations
- $\overline{\text{RESET}}$ Input for Device Initialization
- Sector Lockdown Support
- Top or Bottom Boot Block Configuration Available
- 128-bit Protection Register

SRAM

- 4-megabit (256K x 16)/8-megabit (512K x 16)
- 2.7V to 3.3V V_{CC}
- 70 ns Access Time
- Fully Static Operation and Tri-state Output
- 1.2V (Min) Data Retention
- Industrial Temperature Range

Device Number	Flash Boot Location	Flash Plane Architecture	SRAM Configuration
AT52BR3224	Bottom	32M	256K x 16
AT52BR3224T	Top	32M	256K x 16
AT52BR3228	Bottom	32M	512K x 16
AT52BR3228T	Top	32M	512K x 16

32-megabit Flash + 4-megabit/ 8-megabit SRAM Stack Memory

AT52BR3224
AT52BR3224T
AT52BR3228
AT52BR3228T

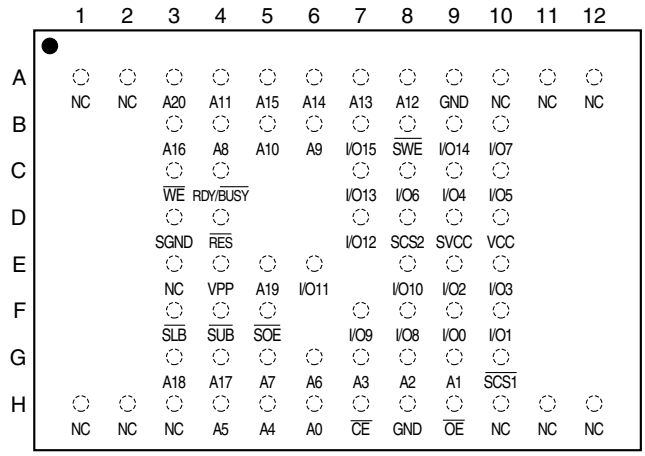
Preliminary

Rev. 1682A–10/01

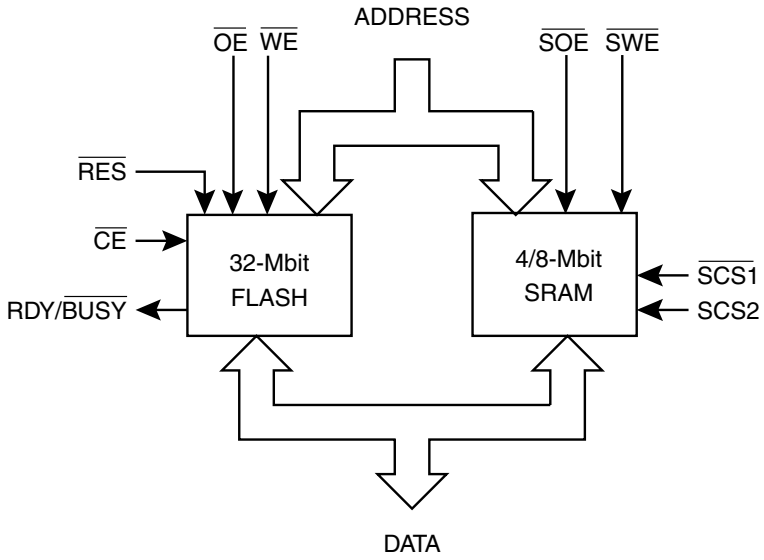
Pin Configurations

Pin Name	Function
A0 - A16	Flash/SRAM Common Address Input
A17 - A20	Flash Address Input
$\overline{CE}$	Flash Chip Enable
$\overline{OE}$	Flash Output Enable
$\overline{WE}$	Flash Write Enablee
$\overline{RESET}$	Flash Reset
RDY/$\overline{BUSY}$	Flash READY/$\overline{BUSY}$ Output
VPP	Flash Power Supply for Accelerated Program/Erase Operations
VCC	Flash Power
GND	Flash Ground
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect
$\overline{SLB}$	SRAM Lower Byte
$\overline{SUB}$	SRAM Upper Byte
SVCC	SRAM Power
SGND	SRAM Ground
$\overline{SCS1}$	SRAM Chip Select 1
SCS2	SRAM Chip Select 2
$\overline{SWE}$	SRAM Write Enable
$\overline{SOE}$	SRAM Output Enable

AT52BR3224(T)/3228(T) (Top View)



Block Diagram



Description

The AT52BR3224(T) combines a 32-megabit Flash (2M x 16) and a 4-megabit SRAM (organized as 256K x 16) in a stacked 66-ball CBGA package. The AT52BR3228(T) combines a 32-megabit Flash (2M x 16) and an 8-megabit SRAM (organized as 512K x 16) in a stacked 66-ball CBGA package. The stacked modules operate at 2.7V to 3.3V in the industrial temperature range.

Absolute Maximum Ratings

Temperature under Bias	-40°C to +85°C
Storage Temperature	-55°C to +150°C
All Input Voltages except V_{PP} and $\overline{RESET}$ (including NC Pins) with Respect to Ground	-0.2V to +3.3V
Voltage on V_{PP} with Respect to Ground	-0.2V to + 6.25V
Voltage on $\overline{RESET}$ with Respect to Ground	-0.2V to +13.5V
All Output Voltages with Respect to Ground	-0.2V to +0.2V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT52BR3224(T)/3228(T)-85
Operating Temperature (Case)	Industrial	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.3V

32-megabit Flash Description

The 32-megabit Flash memory is organized as 2,097,152 words of 16 bits each. The x16 data appears on I/O0 - I/O15. The memory is divided into 71 sectors for erase operations. The device features $\overline{CE}$ and $\overline{OE}$ control signals to avoid any bus contention. This device can be read or reprogrammed using a single power supply, making it ideally suited for in-system programming.

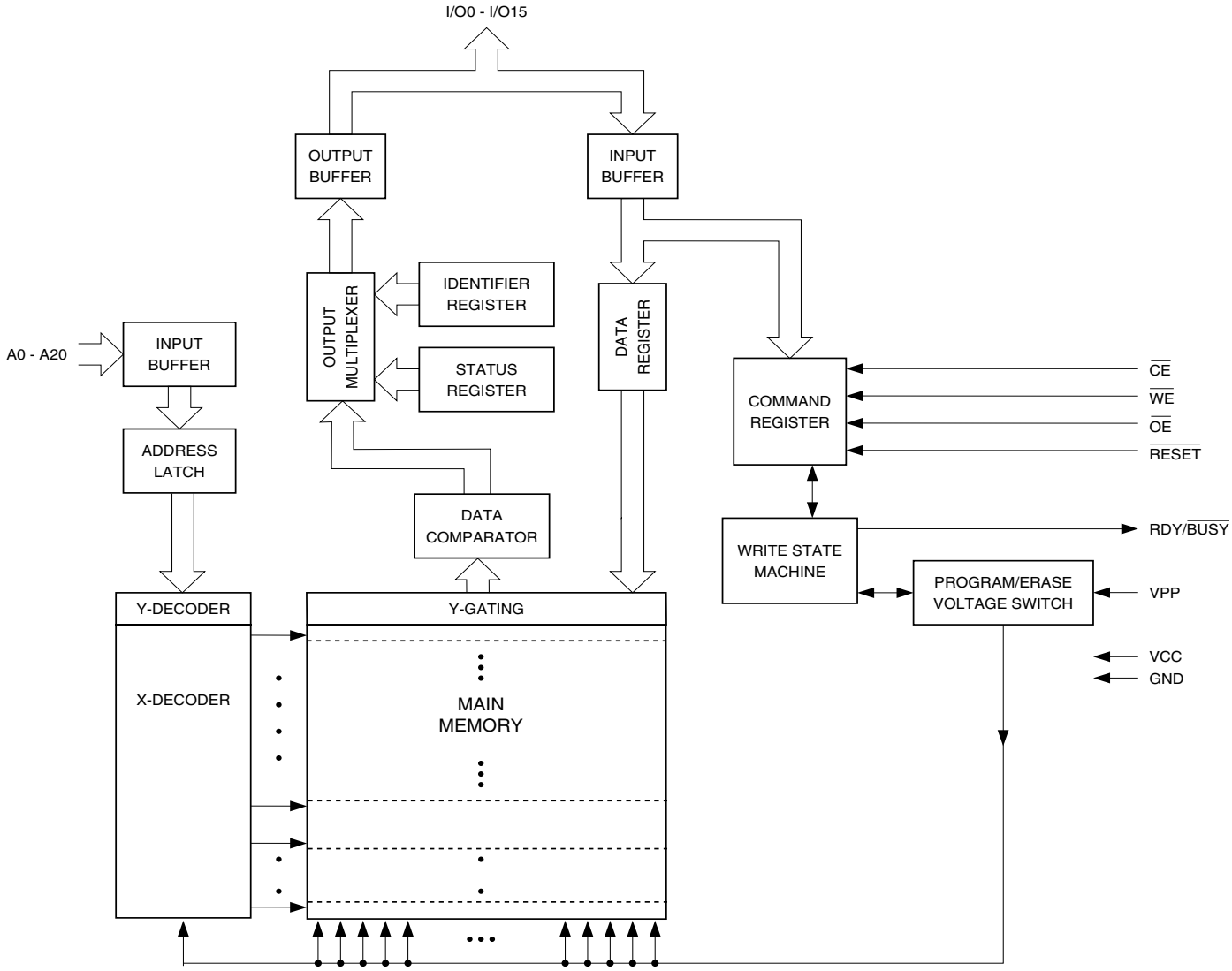
The device powers on in the read mode. Command sequences are used to place the device in other operation modes such as program and erase. The device has the capability to protect the data in any sector (see “Sector Lockdown” section).

To increase the flexibility of the device, it contains an Erase Suspend and Program Suspend feature. This feature will put the erase or program on hold for any amount of time and let the user read data from or program data to any of the remaining sectors within the memory. The end of a program or an erase cycle is detected by the READY/$\overline{BUSY}$ pin, $\overline{Data}$ Polling or by the toggle bit.

The VPP pin provides data protection and faster programming. When the V_{PP} input is below 0.8V, the program and erase functions are inhibited. When V_{PP} is at 1.65V or above, normal program and erase operations can be performed. With V_{PP} at 5.0V or 12.0V, the program and erase operations are accelerated.

A six-byte command (Enter Single Pulse Program Mode) sequence to remove the requirement of entering the three-byte program sequence is offered to further improve programming time. After entering the six-byte code, only single pulses on the write control lines are required for writing into the device. This mode (Single Pulse Byte/Word Program) is exited by powering down the device, or by pulsing the $\overline{RESET}$ pin low for a minimum of 500 ns and then bringing it back to V_{CC}. Erase, Erase Suspend/Resume and Program Suspend/Resume commands will not work while in this mode; if entered they will result in data being programmed into the device. It is not recommended that the six-byte code reside in the software of the final product but only exist in external programming code.

32-megabit Flash Memory Block Diagram



Device Operation

READ: The 32-megabit Flash is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins are asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on, it will be reset to the read or standby mode, depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the "Command Definition in Hex" table on page 14 (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ input halts the present device operation and puts the outputs of the device in a high impedance state. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to the read or standby mode, depending upon the state of the control inputs.

ERASURE: Before a word can be reprogrammed, it must be erased. The erased state of memory bits is a logical "1". The entire device can be erased by using the Chip Erase command or individual sectors can be erased by using the Sector Erase command.

CHIP ERASE: The entire device can be erased at one time by using the six-byte chip erase software code. After the chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time to erase the chip is t_{EC}.

If the sector lockdown has been enabled, the chip erase will not erase the data in the sector that has been locked out; it will erase only the unprotected sectors. After the chip erase, the device will return to the read or standby mode.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into 71 sectors (SA0 - SA70) that can be individually erased. The Sector Erase command is a six-bus cycle operation. The sector address is latched on the falling $\overline{WE}$ edge of the sixth cycle while the 30H data input command is latched on the rising edge of $\overline{WE}$. The sector erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. The maximum time to erase a sector is t_{SEC}. When the sector programming lockdown feature is not enabled, the sector will erase (from the same Sector Erase command). An attempt to erase a sector that has been protected will result in the operation terminating in 2 µs.

WORD PROGRAMMING: Once a memory block is erased, it is programmed (to a logical "0") on a word-by-word basis. Programming is accomplished via the internal device command register and is a four-bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is completed after the specified t_{BP} cycle time. The $\overline{Data}$ Polling feature or the Toggle Bit feature may be

used to indicate the end of a program cycle. If the erase/program status bit is a “1”, the device was not able to verify that the erase or program operation was performed successfully.

VPP PIN: The circuitry of the 32-megabit Flash is designed so that the device can be programmed or erased from the V_{CC} power supply or from the VPP input pin. When V_{PP} is greater than 1.65V and less than or equal to the VCC pin, the device selects the V_{CC} supply for programming and erase operations. When the VPP pin is greater than the V_{CC} supply, the device will select the V_{PP} input as the power supply for programming and erase operations. The device will allow for some variations between the V_{PP} input and the V_{CC} power supply in its selection of V_{CC} or V_{PP} for program or erase operations. If the VPP pin is within 0.3V of V_{CC} for $2.65V < V_{CC} < 3.6V$, then the program or erase operations will use V_{CC} and disregard the V_{PP} input signal. When the V_{PP} signal is used for program and erase operations, the V_{PP} must be in the 5V ± 0.5V or 12V ± 0.5V range to ensure proper operation. The V_{pp} pin cannot be left floating.

PROGRAM/ERASE STATUS: The device provides several bits to determine the status of a program or erase operation: I/O2, I/O3, I/O5, I/O6 and I/O7. The “Status Bit Table” on page 13 and the following four sections describe the function of these bits. To provide greater flexibility for system designers, the 32-megabit Flash contains a programmable configuration register. The configuration register allows the user to specify the status bit operation. The configuration register can be set to one of two different values, “00” or “01”. If the configuration register is set to “00”, the part will automatically return to the read mode after a successful program or erase operation. If the configuration register is set to a “01”, a Product ID Exit command must be given after a successful program or erase operation before the part will return to the read mode. It is important to note that whether the configuration register is set to a “00” or to a “01”, any unsuccessful program or erase operation requires using the Product ID Exit command to return the device to read mode. The default value (after power-up) for the configuration register is “00”. Using the four-bus cycle Set Configuration Register command as shown in the “Command Definition in Hex” table on page 14, the value of the configuration register can be changed. Voltages applied to the $\overline{\text{RESET}}$ pin will not alter the value of the configuration register. The value of the configuration register will affect the operation of the I/O7 status bit as described below.

$\overline{\text{DATA}}$ POLLING: The 32-megabit Flash features $\overline{\text{Data}}$ Polling to indicate the end of a program cycle. If the status configuration register is set to a “00”, during a program cycle an attempted read of the last word loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a “0” on I/O7. Once the program or erase cycle has completed, true data will be read from the device. $\overline{\text{Data}}$ Polling may begin at any time during the program cycle. Please see “Status Bit Table” on page 13 for more details.

If the status bit configuration register is set to a “01”, the I/O7 status bit will be low while the device is actively programming or erasing data. I/O7 will go high when the device has completed a program or erase operation. Once I/O7 has gone high, status information on the other pins can be checked.

The $\overline{\text{Data}}$ Polling status bit must be used in conjunction with the erase/program and V_{PP} status bit as shown in the algorithm in Figures 1 and 2 on page 11.

TOGGLE BIT: In addition to $\overline{\text{Data}}$ Polling the 32-megabit Flash provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the memory will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling

and valid data will be read. Examining the toggle bit may begin at any time during a program cycle. Please see “Status Bit Table” on page 13 for more details.

The toggle bit status bit should be used in conjunction with the erase/program and V_{PP} status bit as shown in the algorithm in Figures 3 and 4 on page 12.

ERASE/PROGRAM STATUS BIT: The device offers a status bit on I/O5, which indicates whether the program or erase operation has exceeded a specified internal pulse count limit. If the status bit is a “1”, the device is unable to verify that an erase or a word program operation has been successfully performed. The device may also output a “1” on I/O5 if the system tries to program a “1” to a location that was previously programmed to a “0”. Only an erase operation can change a “0” back to a “1”. If a program (Sector Erase) command is issued to a protected sector, the protected sector will not be programmed (erased). The device will go to a status read mode and the I/O5 status bit will be set high, indicating the program (erase) operation did not complete as requested. Once the erase/program status bit has been set to a “1”, the system must write the Product ID Exit command to return to the read mode. The erase/program status bit is a “0” while the erase or program operation is still in progress. Please see “Status Bit Table” on page 13 for more details.

V_{PP} STATUS BIT: The 32-megabit Flash provides a status bit on I/O3, which provides information regarding the voltage level of the VPP pin. During a program or erase operation, if the voltage on the VPP pin is not high enough to perform the desired operation successfully, the I/O3 status bit will be a “1”. Once the V_{PP} status bit has been set to a “1”, the system must write the Product ID Exit command to return to the read mode. On the other hand, if the voltage level is high enough to perform a program or erase operation successfully, the V_{PP} status bit will output a “0”. Please see “Status Bit Table” on page 13 for more details.

SECTOR LOCKDOWN: Each sector has a programming lockdown feature. This feature prevents programming of data in the designated sectors once the feature has been enabled. These sectors can contain secure code that is used to bring up the system. Enabling the lockdown feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; any sector’s usage as a write-protected region is optional to the user.

At power-up or reset, all sectors are unlocked. To activate the lockdown for a specific sector, the six-bus cycle Sector Lockdown command must be issued. Once a sector has been locked down, the contents of the sector is read-only and cannot be erased or programmed.

SECTOR LOCKDOWN DETECTION: A software method is available to determine if programming of a sector is locked down. When the device is in the software product identification mode (see “Software Product Identification Entry/Exit” sections on page 27), a read from address location 00002H within a sector will show if programming the sector is locked down. If the data on I/O0 is low, the sector can be programmed; if the data on I/O0 is high, the program lockdown feature has been enabled and the sector cannot be programmed. The software product identification exit code should be used to return to standard operation.

SECTOR LOCKDOWN OVERRIDE: The only way to unlock a sector that is locked down is through reset or power-up cycles. After power-up or reset, the content of a sector that is locked down can be erased and reprogrammed.

ERASE SUSPEND/ERASE RESUME: The Erase Suspend command allows the system to interrupt a sector or chip erase operation and then program or read data from a different sector within the memory. After the Erase Suspend command is given, the device requires a maximum time of 15 µs to suspend the erase operation. After the

erase operation has been suspended, the system can then read data or program data to any other sector within the device. An address is not required during the Erase Suspend command. During a sector erase suspend, another sector cannot be erased. To resume the sector erase operation, the system must write the Erase Resume command. The Erase Resume command is a one-bus cycle command. The device also supports an erase suspend during a complete chip erase. While the chip erase is suspended, the user can read from any sector within the memory that is protected. The command sequence for a chip erase suspend and a sector erase suspend are the same.

PROGRAM SUSPEND/PROGRAM RESUME: The Program Suspend command allows the system to interrupt a programming operation and then read data from a different word within the memory. After the Program Suspend command is given, the device requires a maximum of 20 µs to suspend the programming operation. After the programming operation has been suspended, the system can then read data from any other word within the device. An address is not required during the program suspend operation. To resume the programming operation, the system must write the Program Resume command. The program suspend and resume are one-bus cycle commands. The command sequence for the erase suspend and program suspend are the same, and the command sequence for the erase resume and program resume are the same.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see “Operating Modes” on page 20 (for hardware operation) or “Software Product Identification Entry/Exit” sections on page 27. The manufacturer and device codes are the same for both modes.

128-BIT PROTECTION REGISTER: The 32-megabit Flash contains a 128-bit register that can be used for security purposes in system design. The protection register is divided into two 64-bit blocks. The two blocks are designated as block A and block B. The data in block A is non-changeable and is programmed at the factory with a unique number. The data in block B is programmed by the user and can be locked out such that data in the block cannot be reprogrammed. To program block B in the protection register, the four-bus cycle Program Protection Register command must be used as shown in the “Command Definition in Hex” table on page 14. To lock out block B, the four-bus cycle Lock Protection Register command must be used as shown in the “Command Definition in Hex” table. Data bit D1 must be zero during the fourth bus cycle. All other data bits during the fourth bus cycle are don’t cares. To determine whether block B is locked out, the Product ID Entry command is given followed by a read operation from address 80H. If data bit D1 is zero, block B is locked. If data bit D1 is one, block B can be reprogrammed. Please see the “Protection Register Addressing Table” on page 15 for the address locations in the protection register. To read the protection register, the Product ID Entry command is given followed by a normal read operation from an address within the protection register. After determining whether block B is protected or not, or reading the protection register, the Product ID Exit command must be given prior to performing any other operation.

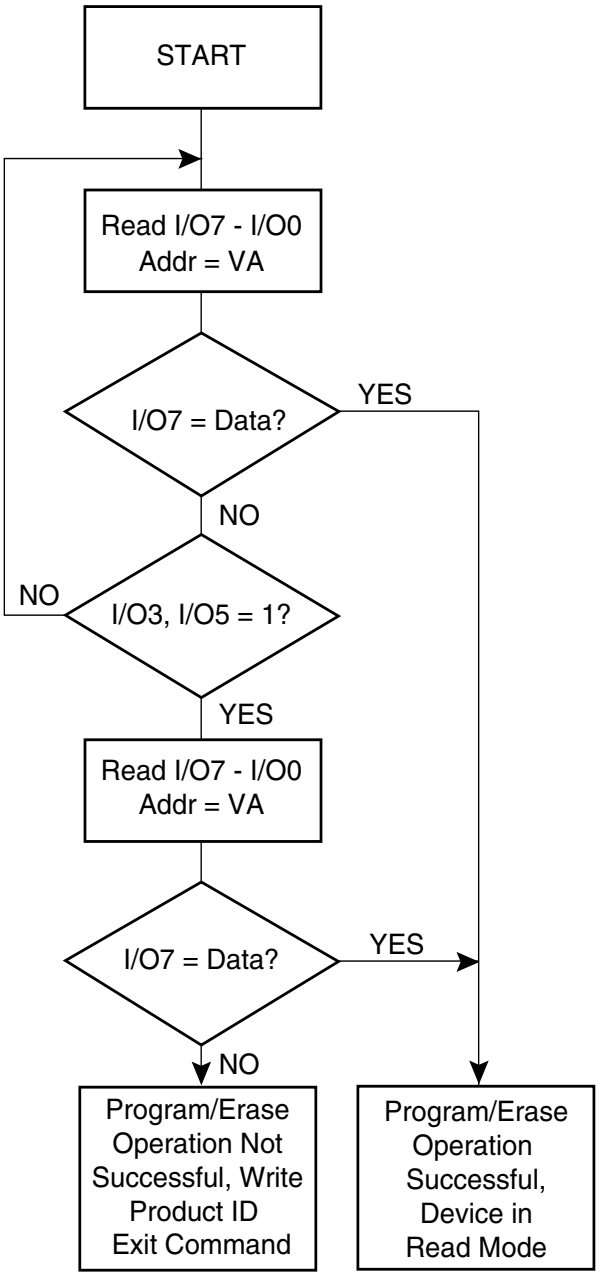
RDY/$\overline{\text{BUSY}}$: For the 32-megabit Flash, an open-drain READY/$\overline{\text{BUSY}}$ output pin provides another method of detecting the end of a program or erase operation. RDY/$\overline{\text{BUSY}}$ is actively pulled low during the internal program and erase cycles and is released at the completion of the cycle. The open-drain connection allows for OR-tying of several devices to the same RDY/$\overline{\text{BUSY}}$ line. Please see “Status Bit Table” on page 13 for more details.

HARDWARE DATA PROTECTION: The Hardware Data Protection feature protects against inadvertent programs to the Flash in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power-on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle. (e) Program inhibit: V_{PP} is less than V_{ILPP}. (f) V_{PP} power-on delay: once V_{PP} has reached 1.65V, program and erase operations are inhibited for 100 ns.

INPUT LEVELS: While operating with a 2.65V to 3.6V power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$ and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to V_{CC} + 0.6V.

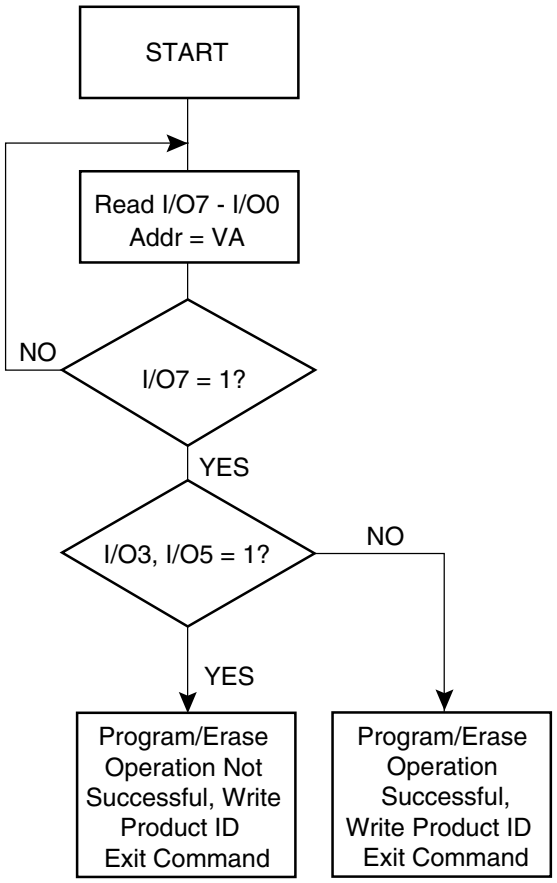
OUTPUT LEVELS: For the 32-megabit Flash, output high levels (V_{OH}) are equal to V_{CCQ} - 0.2V (not V_{CC}). For 2.65V - 3.6V output levels, V_{CCQ} must be tied to V_{CC}. For 1.8V - 2.2V output levels, V_{CCQ} must be regulated to 2.0V ± 10%, while V_{CC} must be regulated to 2.65V - 3.0V (for minimum power).

Figure 1. $\overline{\text{Data}}$ Polling Algorithm
(Configuration Register = 00)



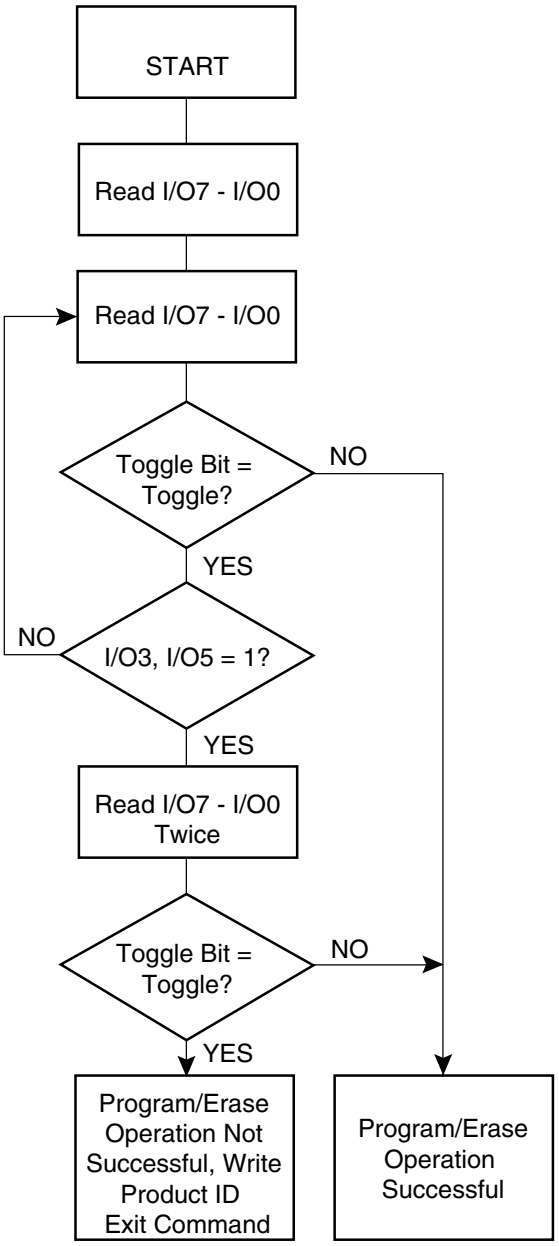
Notes:
1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
2. I/O7 should be rechecked even if I/O5 = "1" because I/O7 may change simultaneously with I/O5.

Figure 2. $\overline{\text{Data}}$ Polling Algorithm
(Configuration Register = 01)



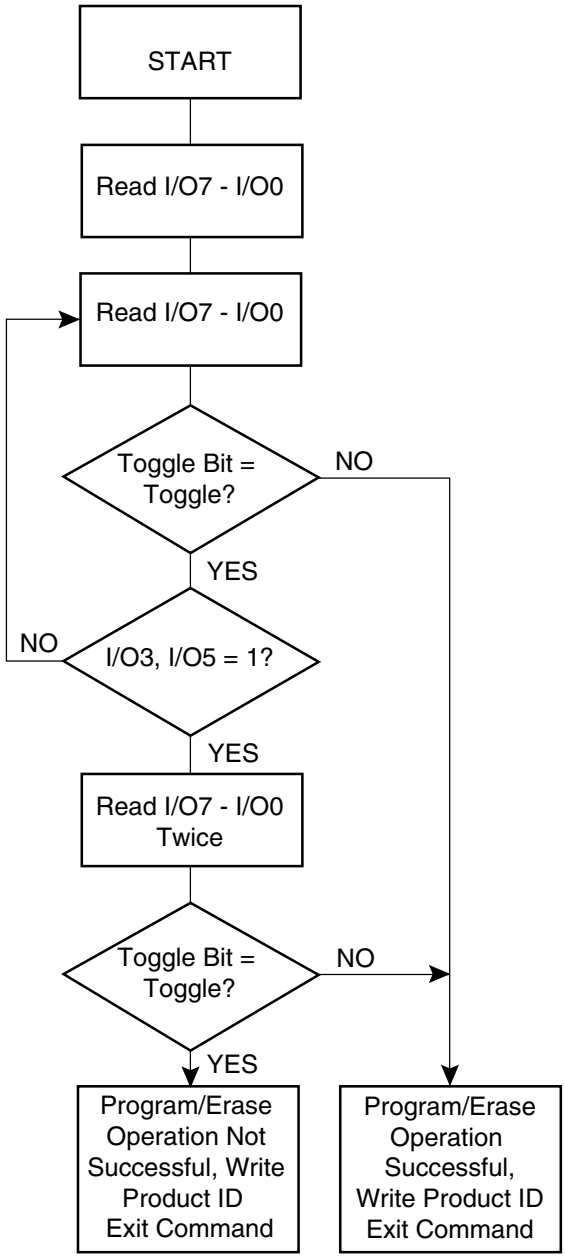
Note:
1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.

Figure 3. Toggle Bit Algorithm
(Configuration Register = 00)



Note: 1. The system should recheck the toggle bit even if I/O5 = “1” because the toggle bit may stop toggling as I/O5 changes to “1”.

Figure 4. Toggle Bit Algorithm
(Configuration Register = 01)



Note: 1. The system should recheck the toggle bit even if I/O5 = “1” because the toggle bit may stop toggling as I/O5 changes to “1”.

Status Bit Table

	Status Bit						
	I/O7	**I/O7**	**I/O6**	**I/O5**(1)	**I/O3**(2)	**I/O2**	**RDY/$\overline{\text{BUSY}}$**
Configuration Register	**00**	**01**	**00/01**	**00/01**	**00/01**	**00/01**	**00/01**
Programming	$\overline{\text{I/O7}}$	0	TOGGLE	0	0	1	0
Erasing	0	0	TOGGLE	0	0	TOGGLE	0
Erase Suspended & Read Erasing Sector	1	1	1	0	0	TOGGLE	1
Erase Suspended & Read Non-erasing Sector	DATA	DATA	DATA	DATA	DATA	DATA	1
Erase Suspended & Program Non-erasing Sector	$\overline{\text{I/O7}}$	0	TOGGLE	0	0	TOGGLE	0

Notes: 1. I/O5 switches to a “1” when a program or an erase operation has exceeded the maximum time limits or when a program or sector erase operation is performed on a protected sector.
2. I/O3 switches to a “1” when the V_{PP} level is not high enough to successfully perform program and erase operations.

Command Definition in Hex[1]

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	555	AA	AAA[2]	55	555	80	555	AA	AAA	55	555	10
Sector Erase	6	555	AA	AAA	55	555	80	555	AA	AAA	55	SA[3][4]	30
Word Program	4	555	AA	AAA	55	555	A0	Addr	D_{IN}				
Enter Single Pulse Program Mode	6	555	AA	AAA	55	555	80	555	AA	AAA	55	555	A0
Single Pulse Word Program	1	Addr	D_{IN}										
Sector Lockdown	6	555	AA	AAA[2]	55	555	80	555	AA	AAA	55	SA[3][4]	60
Erase/Program Suspend	1	XXX	B0										
Erase/Program Resume	1	XXX	30										
Product ID Entry	3	555	AA	AAA	55	555	90						
Product ID Exit[5]	3	555	AA	AAA	55	555	F0						
Product ID Exit[5]	1	XXX	F0										
Program Protection Register	4	555	AA	AAA	55	555	C0	Addr	D_{IN}				
Lock Protection Register - Block B	4	555	AA	AAA	55	555	C0	080	X0				
Status of Block B Protection	4	555	AA	AAA	55	555	90	80	D_{OUT}[6]				
Set Configuration Register	4	555	AA	AAA	55	555	D0	XXX	00/01[7]				

Notes:
1. The DATA FORMAT shown for each bus cycle is as follows; I/O7 - I/O0 (Hex). In word operation I/O15 - I/O8 are don't care. The ADDRESS FORMAT shown for each bus cycle is as follows: A11 - A0 (Hex). Address A20 through A11 are don't care.
2. Since A11 is a Don't Care, AAA can be replaced with 2AA.
3. SA = sector address. Any word address within a sector can be used to designate the sector address (see pages 16 and 18 for details).
4. Once a sector is in the lockdown mode, data in the protected sector cannot be changed unless the chip is reset or power cycled.
5. Either one of the Product ID Exit commands can be used.
6. If data bit D1 is "0", block B is locked. If data bit D1 is "1", block B can be reprogrammed.
7. The default state (after power-up) of the configuration register is "00".

Absolute Maximum Ratings*

Temperature under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including NC Pins)
with Respect to Ground .....-0.6V to +6.25V

All Output Voltages
with Respect to Ground .....-0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ and V_{PP}
with Respect to Ground .....-0.6V to +13.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Protection Register Addressing Table

Word	Use	Block	A7	A6	A5	A4	A3	A2	A1	A0
0	Factory	A	1	0	0	0	0	0	0	1
1	Factory	A	1	0	0	0	0	0	1	0
2	Factory	A	1	0	0	0	0	0	1	1
3	Factory	A	1	0	0	0	0	1	0	0
4	User	B	1	0	0	0	0	1	0	1
5	User	B	1	0	0	0	0	1	1	0
6	User	B	1	0	0	0	0	1	1	1
7	User	B	1	0	0	0	1	0	0	0

Note: All address lines not specified in the above table must be “0” when accessing the protection register, i.e., A20 - A8 = 0.

Bottom Boot 32-megabit Flash – Sector Address Table

Sector	Size (Words)	x16 Address Range (A20 - A0)
SA0	4K	00000 - 00FFF
SA1	4K	01000 - 01FFF
SA2	4K	02000 - 02FFF
SA3	4K	03000 - 03FFF
SA4	4K	04000 - 04FFF
SA5	4K	05000 - 05FFF
SA6	4K	06000 - 06FFF
SA7	4K	07000 - 07FFF
SA8	32K	08000 - 0FFFF
SA9	32K	10000 - 17FFF
SA10	32K	18000 - 1FFFF
SA11	32K	20000 - 27FFF
SA12	32K	28000 - 2FFFF
SA13	32K	30000 - 37FFF
SA14	32K	38000 - 3FFFF
SA15	32K	40000 - 47FFF
SA16	32K	48000 - 4FFFF
SA17	32K	50000 - 57FFF
SA18	32K	58000 - 5FFFF
SA19	32K	60000 - 67FFF
SA20	32K	68000 - 6FFFF
SA21	32K	70000 - 77FFF
SA22	32K	78000 - 7FFFF
SA23	32K	80000 - 87FFF
SA24	32K	88000 - 8FFFF
SA25	32K	90000 - 97FFF
SA26	32K	98000 - 9FFFF
SA27	32K	A0000 - A7FFF
SA28	32K	A8000 - AFFFF
SA29	32K	B0000 - B7FFF
SA30	32K	B8000 - BFFFF
SA31	32K	C0000 - C7FFF
SA32	32K	C8000 - CFFFF
SA33	32K	D0000 - D7FFF
SA34	32K	D8000 - DFFFF
SA35	32K	E0000 - E7FFF

Bottom Boot 32-megabit Flash – Sector Address Table (Continued)

Sector	Size (Words)	x16 Address Range (A20 - A0)
SA36	32K	E8000 - EFFFF
SA37	32K	F0000 - F7FFF
SA38	32K	F8000 - FFFFF
SA39	32K	100000 - 107FFF
SA40	32K	108000 - 10FFFF
SA41	32K	110000 - 117FFF
SA42	32K	118000 - 11FFFF
SA43	32K	120000 - 127FFF
SA44	32K	128000 - 12FFFF
SA45	32K	130000 - 137FFF
SA46	32K	138000 - 13FFFF
SA47	32K	140000 - 147FFF
SA48	32K	148000 - 14FFFF
SA49	32K	150000 - 157FFF
SA50	32K	158000 - 15FFFF
SA51	32K	160000 - 167FFF
SA52	32K	168000 - 16FFFF
SA53	32K	170000 - 177FFF
SA54	32K	178000 - 17FFFF
SA55	32K	180000 - 187FFF
SA56	32K	188000 - 18FFFF
SA57	32K	190000 - 197FFF
SA58	32K	198000 - 19FFFF
SA59	32K	1A0000 - 1A7FFF
SA60	32K	1A8000 - 1AFFFF
SA61	32K	1B0000 - 1B7FFF
SA62	32K	1B8000 - 1BFFFF
SA63	32K	1C0000 - 1C7FFF
SA64	32K	1C8000 - 1CFFFF
SA65	32K	1D0000 - 1D7FFF
SA66	32K	1D8000 - 1DFFFF
SA67	32K	1E0000 - 1E7FFF
SA68	32K	1E8000 - 1EFFFF
SA69	32K	1F0000 -1F7FFF
SA70	32K	1F8000 - 1FFFF

Top Boot 32-megabit Flash – Sector Address Table

Sector	Size (Words)	x16 Address Range (A20 - A0)
SA0	32K	00000 - 07FFF
SA1	32K	08000 - 0FFFF
SA2	32K	10000 - 17FFF
SA3	32K	18000 - 1FFFF
SA4	32K	20000 - 27FFF
SA5	32K	28000 - 2FFFF
SA6	32K	30000 - 37FFF
SA7	32K	38000 - 3FFFF
SA8	32K	40000 - 47FFF
SA9	32K	48000 - 4FFFF
SA10	32K	50000 - 57FFF
SA11	32K	58000 - 5FFFF
SA12	32K	60000 - 67FFF
SA13	32K	68000 - 6FFFF
SA14	32K	70000 - 77FFF
SA15	32K	78000 - 7FFFF
SA16	32K	80000 - 87FFF
SA17	32K	88000 - 8FFFF
SA18	32K	90000 - 97FFF
SA19	32K	98000 - 9FFFF
SA20	32K	A0000 - A7FFF
SA21	32K	A8000 - AFFFF
SA22	32K	B0000 - B7FFF
SA23	32K	B8000 - BFFFF
SA24	32K	C0000 - C7FFF
SA25	32K	C8000 - CFFFF
SA26	32K	D0000 - D7FFF
SA27	32K	D8000 - DFFFF
SA28	32K	E0000 - E7FFF
SA29	32K	E8000 - EFFFF
SA30	32K	F0000 - F7FFF
SA31	32K	F8000 - FFFFF
SA32	32K	100000 - 107FFF
SA33	32K	108000 - 10FFFF
SA34	32K	110000 - 117FFF
SA35	32K	118000 - 11FFFF

Top Boot 32-megabit Flash – Sector Address Table (Continued)

Sector	Size (Words)	x16 Address Range (A20 - A0)
SA36	32K	120000 - 127FFF
SA37	32K	128000 - 12FFFF
SA38	32K	130000 - 137FFF
SA39	32K	138000 - 13FFFF
SA40	32K	140000 - 147FFF
SA41	32K	148000 - 14FFFF
SA42	32K	150000 - 157FFF
SA43	32K	158000 - 15FFFF
SA44	32K	160000 - 167FFF
SA45	32K	168000 - 16FFFF
SA46	32K	170000 - 177FFF
SA47	32K	178000 - 17FFFF
SA48	32K	180000 - 187FFF
SA49	32K	188000 - 18FFFF
SA50	32K	190000 - 197FFF
SA51	32K	198000 - 19FFFF
SA52	32K	1A0000 - 1A7FFF
SA53	32K	1A8000 - 1AFFFF
SA54	32K	1B0000 - 1B7FFF
SA55	32K	1B8000 - 1BFFFF
SA56	32K	1C0000 - 1C7FFF
SA57	32K	1C8000 - 1CFFFF
SA58	32K	1D0000 - 1D7FFF
SA59	32K	1D8000 - 1DFFFF
SA60	32K	1E0000 - 1E7FFF
SA61	32K	1E8000 - 1EFFFF
SA62	32K	1F0000 - 1F7FFF
SA63	4K	1F8000 - 1F8FFF
SA64	4K	1F9000 - 1F9FFF
SA65	4K	1FA000 - 1FAFFF
SA66	4K	1FB000 - 1FBFFF
SA67	4K	1FC000 - 1FCFFF
SA68	4K	1FD000 - 1FDFFF
SA69	4K	1FE000 - 1FEFFF
SA70	4K	1FF000 - 1FFFFF

DC and AC Operating Range

		AT52BR3224(T)-85	AT52BR3228(T)-85
Operating Temperature (Case)	Industrial	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V - 3.3V	2.7V - 3.3V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	V_{PP}	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Ai	D_{OUT}
Program/Erase[2]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IHPP}[6]	Ai	D_{IN}
Standby/Program Inhibit	V_{IH}	X[1]	X	V_{IH}	X	X	High-Z
Program Inhibit	X	X	V_{IH}	V_{IH}	X		
	X	V_{IL}	X	V_{IH}	X		
	X	X	X	V_{IH}	V_{ILPP}[7]		
Output Disable	X	V_{IH}	X	V_{IH}	X		High-Z
Reset	X	X	X	V_{IL}	X	X	High-Z
Product Identification							
Hardware	V_{IL}	V_{IL}	V_{IH}	V_{IH}		A1 - A20 = V_{IL}, A9 = V_H[3], A0 = V_{IL}	Manufacturer Code[4]
						A1 - A20 = V_{IL}, A9 = V_H[3], A0 = V_{IH}	Device Code[4]
Software[5]				V_{IH}		A0 = V_{IL}, A1 - A20 = V_{IL}	Manufacturer Code[4]
						A0 = V_{IH}, A1 - A20 = V_{IL}	Device Code[4]

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC programming waveforms on page 25.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 001FH, Device Code: 00C8H (x16)-AT52BR3224/3228; 00C9H (x16)-AT52BR3224T/3228T.
5. See details under “Software Product Identification Entry/Exit” on page 27.
6. V_{IHPP} (min) = 1.65V; V_{IHPP} (max) = 3.6V. For faster erase/program operations, V_{PP} can be set to 5.0V ± 0.5V or 12V ± 0.5V.
7. V_{ILPP} (max) = 0.8V.

DC Characteristics

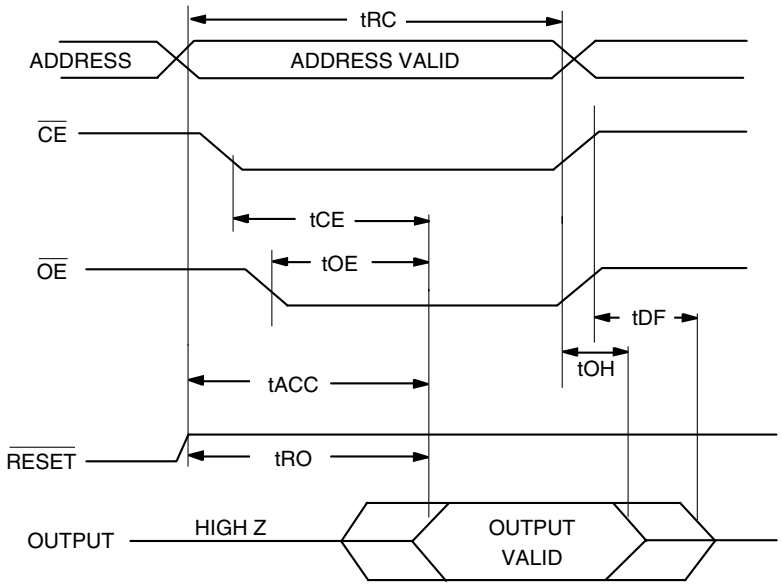
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		10	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		1	mA
I_{SB3}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}, V_{CC} = 2.85V		10	µA
I_{CC} [1][2]	V_{CC} Active Read Current	f = 5 MHz; I_{OUT} = 0 mA		25	mA
I_{CC1}	V_{CC} Programming Current (V_{PP} = V_{CC})			45	mA
I_{PP1}	V_{PP} Input Load Current	V_{PP} = 0V, V_{CC} = 3.0V		-100	µA
		V_{PP} = V_{CC} = 3.0V		100	µA
I_{CC2}	V_{CC} Programming Current (V_{PP} = 5.0V ± 0.5V)			40	mA
I_{PP2}	V_{PP} Programming Current (V_{PP} = 5.0V ± 0.5V)			5	mA
I_{CC3}	V_{CC} Programming Current (V_{PP} = 12.0V ± 0.5V)			40	mA
I_{PP3}	V_{PP} Programming Current (V_{PP} = 12.0V ± 0.5V)			10	mA
V_{IL}	Input Low Voltage			0.6	V
V_{IH}	Input High Voltage		2.0		V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OL2}	Output Low Voltage	I_{OL} = 1.0 mA		0.20	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA V_{CCQ} < 2.6V I_{OH} = -400 µA V_{CCQ} ≥ 2.6V	V_{CCQ} - 0.2 2.4		V V V
V_{OH2}	Output High Voltage	I_{OH} = -100 µA V_{CCQ} < 2.6V I_{OH} = -100 µA V_{CCQ} ≥ 2.6V	V_{CCQ} - 0.1 2.5		V V V

Notes: 1. For 3.3V < V_{CC} < 3.6V, I_{CC} (max) = 30 mA.
2. In the erase mode, I_{CC} is 65 mA.

AC Read Characteristics

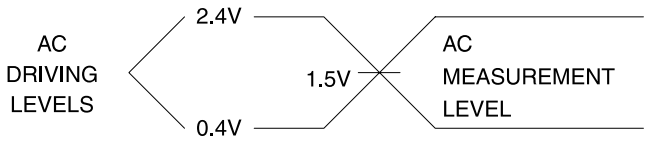
Symbol	Parameter	AT52BR3224(T)-85		AT52BR3228(T)-85		Units
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time		85		85	ns
t_{ACC}	Address to Output Delay		85		85	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		85		85	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	40	0	40	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	25	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns
t_{RO}	$\overline{RESET}$ to Output Delay		100		100	ns

AC Read Waveforms[1][2][3][4]



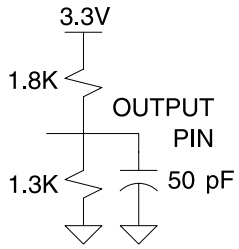
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

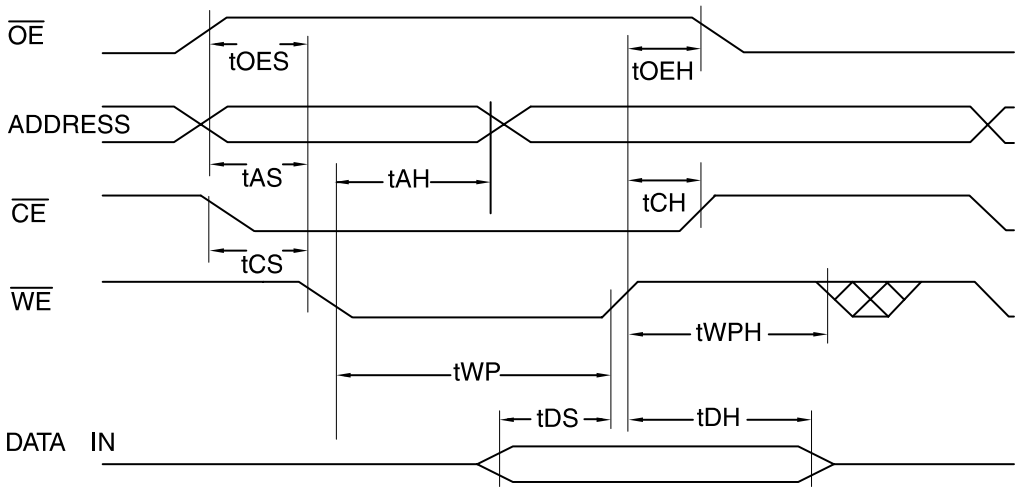
Note: This parameter is characterized and is not 100% tested.

AC Word Load Characteristics

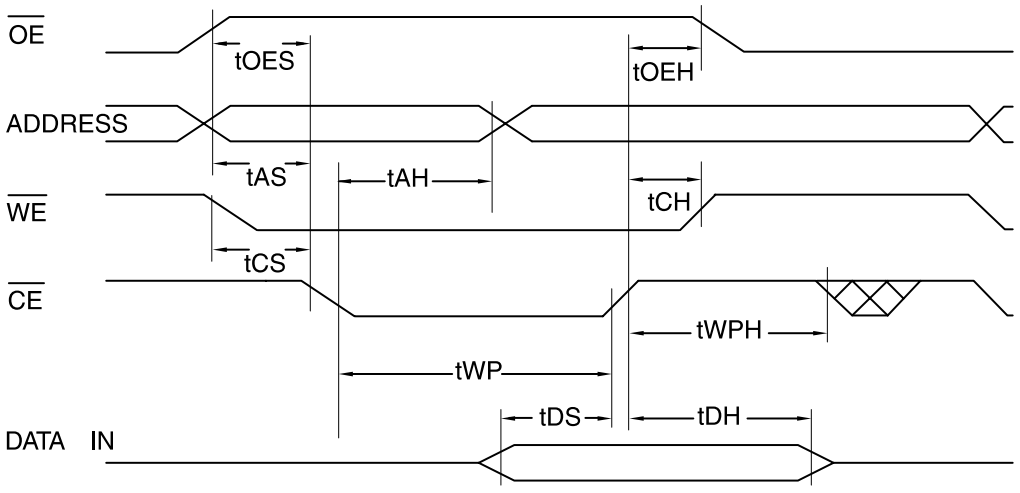
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Setup Time	0		ns
t_{AH}	Address Hold Time	75		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	50		ns
t_{DS}	Data Setup Time	40		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	35		ns

AC Word Load Waveforms

$\overline{WE}$ Controlled



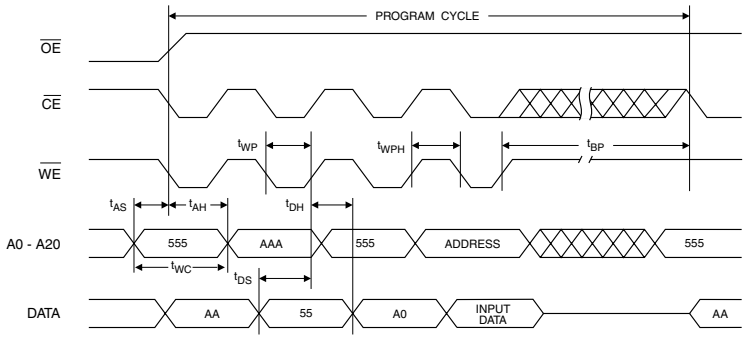
$\overline{CE}$ Controlled



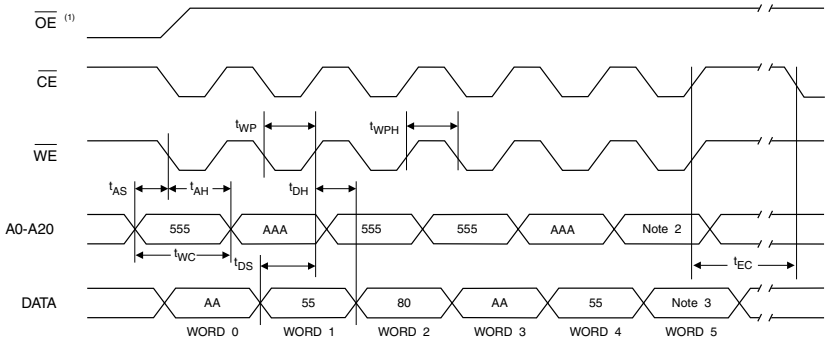
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Word Programming Time ($V_{IHPP} < V_{PP} < 4.5V$)		20	200	µs
t_{BPVPP}	Word Programming Time ($V_{PP} \geq 4.5V$)		10	100	µs
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	75			ns
t_{DS}	Data Setup Time	50			ns
t_{DH}	Data Hold Time	10			ns
t_{WP}	Write Pulse Width	50			ns
t_{WPH}	Write Pulse Width High	35			ns
t_{WC}	Write Cycle Time	85			ns
t_{RP}	$\overline{\text{Reset}}$ Pulse Width	500			ns
t_{EC}	Chip Erase Cycle Time ($V_{PP} < 4.5V$)			15	seconds
t_{ECVPP}	Chip Erase Cycle Time ($V_{PP} \geq 4.5V$)			8	seconds
t_{SEC}	Sector Erase Cycle Time ($V_{PP} < 4.5V$)		200	400	ms
t_{SECVPP}	Sector Erase Cycle Time ($V_{PP} \geq 4.5V$)		100	150	ms
t_{ES}	Erase Suspend Time			15	µs
t_{PS}	Program Suspend Time			20	µs

Program Cycle Waveforms



Sector or Chip Erase Cycle Waveforms



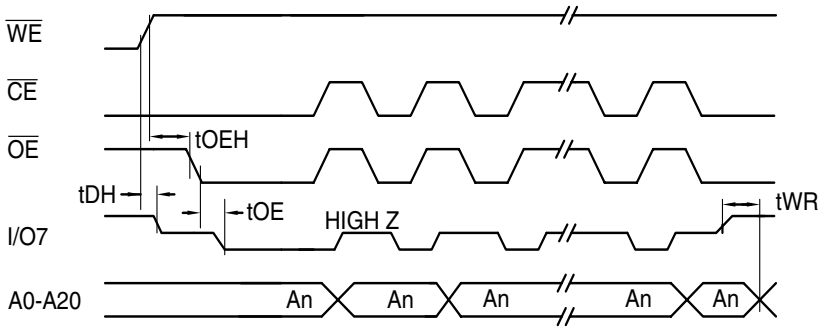
Notes:
1. $\overline{\text{OE}}$ must be high only when $\overline{\text{WE}}$ and $\overline{\text{CE}}$ are both low.
2. For chip erase, the address should be 555. For sector erase, the address depends on what sector is to be erased. (See note 3 under “Command Definitions in Hex” on page 14.)
3. For chip erase, the data should be 10H, and for sector erase, the data should be 30H.

$\overline{\text{Data}}$ Polling Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" on page 22.

$\overline{\text{Data}}$ Polling Waveforms

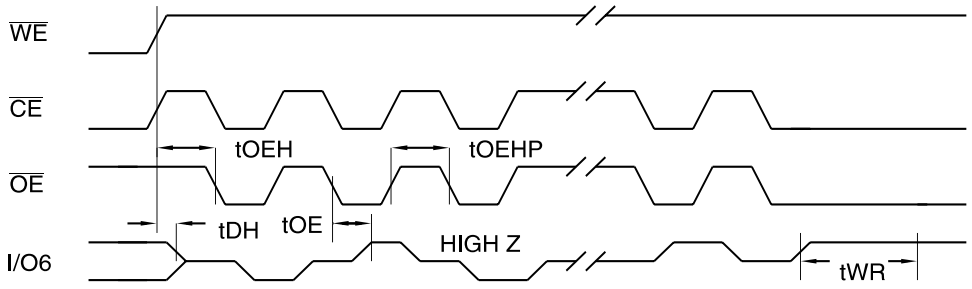


Toggle Bit Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	50			ns
t_{WR}	Write Recovery Time	0			ns

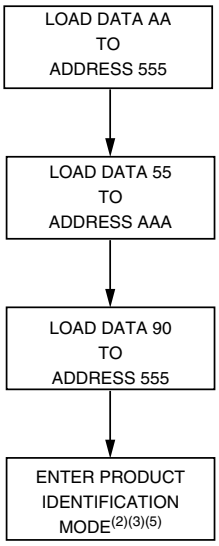
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" on page 22.

Toggle Bit Waveforms(1)(2)(3)

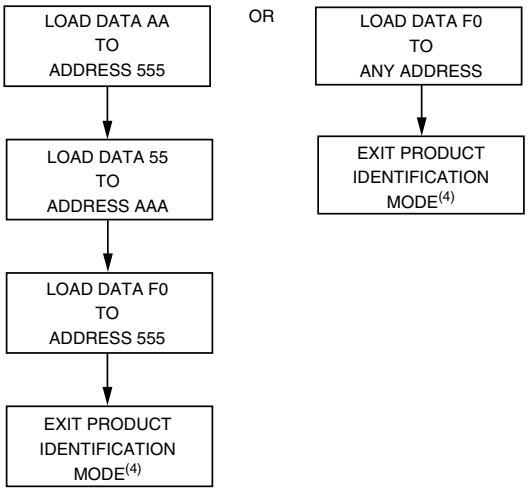


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry[1]

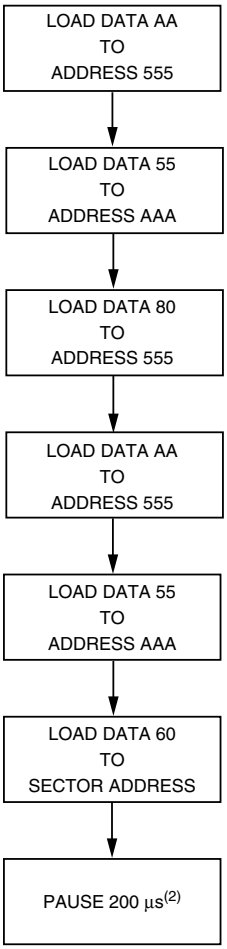


Software Product Identification Exit[1][6]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex) Address Format: A11 - A0 (Hex), A-1, and A11 - A20 (Don't Care).
2. A1 - A20 = V_{IL}. Manufacturer Code is read for A0 = V_{IL}; Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 001FH(x16)
   Device Code: 00C8 - AT52BR3224/3228.
   00C9H - AT52BR3224T/3228T.
6. Either one of the Product ID Exit commands can be used.

Sector Lockdown Enable Algorithm[1]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex) Address Format: A11 - A0 (Hex), A-1, and A11 - A20 (Don't Care).
2. Sector Lockdown feature enabled.

4-megabit SRAM Description

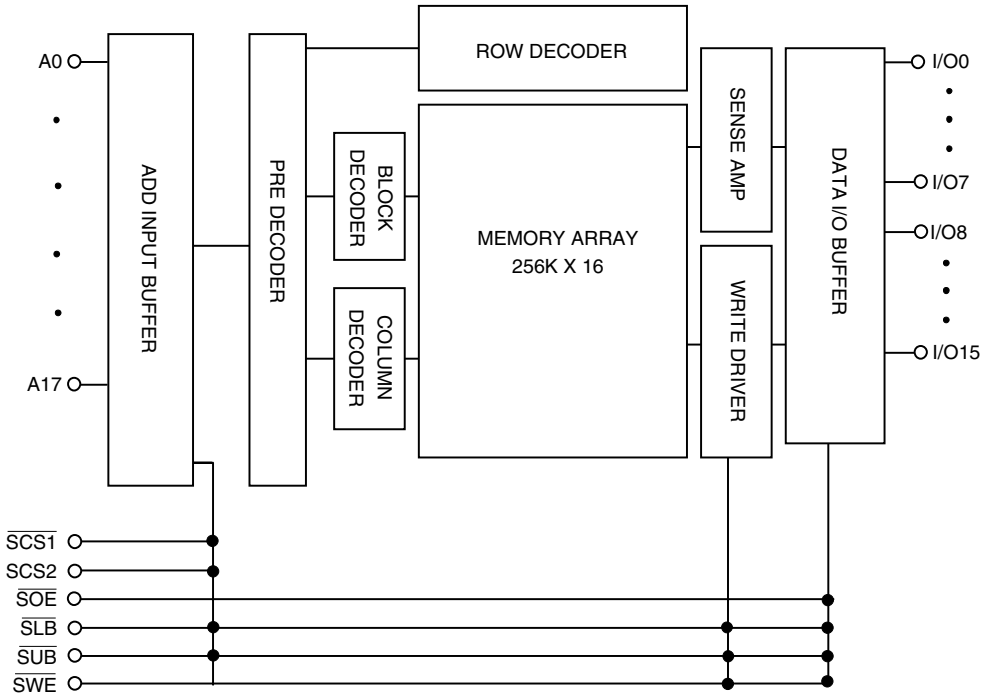
The 4-megabit SRAM is a high-speed, super low-power CMOS SRAM organized as 256K words by 16 bits. The SRAM uses high-performance full CMOS process technology and is designed for high-speed and low-power circuit technology. It is particularly well-suited for the high-density low-power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.2V.

Features

- **Fully Static Operation and Tri-state Output**
- **TTL Compatible Inputs and Outputs**
- **Battery Backup**
  - **1.2V (Min) Data Retention**

Voltage (V)	Speed (ns)	Operation Current/I_{CC} (mA) (Max)	Standby Current (µA) (Max)	Temperature (°C)
2.7 - 3.3	70	5	15	-40 - 85

Block Diagram



Absolute Maximum Ratings[1]

Symbol	Parameter	Rating	Unit
V_{IN}, V_{OUT}	Input/Output Voltage	-0.3 to 3.6	V
V_{CC}	Power Supply	-0.3 to 4.6	V
T_A	Operating Temperature	-40 to 85	°C
T_{STG}	Storage Temperature	-55 to 150	°C
P_D	Power Dissipation	1.0	W

Note: 1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

Truth Table

							I/O Pin		
$\overline{SCS1}$	SCS2	$\overline{SWE}$	$\overline{SOE}$	$\overline{SLB}$[2]	$\overline{SUB}$[2]	Mode	I/O0 - I/O7	I/O8 - I/O15	Power
H[1]	X	X	X	X	X	Deselected	High-Z	High-Z	Standby
X[1]	L								
X	X			H	H				
L[1]	H	H	H	L	H	Output Disabled	High-Z	High-Z	Active
				H	L				
				L	L				
L	H	L	X	L	H	Write	D_{IN}	High-Z	Active
				H	L		High-Z	D_{IN}	
				L	L		D_{IN}	D_{IN}	
							D_{IN}	High-Z	
L	H	H	L	L	H	Read	D_{OUT}	High-Z	Active
				H	L		High-Z	D_{OUT}	
				L	L		D_{OUT}	D_{OUT}	
							D_{OUT}	High-Z	

Notes: 1. H = V_{IH}, L = V_{IL}, X = Don't Care (V_{IL} or V_{IH})
2. $\overline{SUB}$, $\overline{SLB}$ (Upper, Lower Byte Enable). These active LOW inputs allow individual bytes to be written or read. When $\overline{SLB}$ is LOW, data is written or read to the lower byte, I/O0 - I/O7. When $\overline{SUB}$ is LOW, data is written or read to the upper byte, I/O8 - I/O15.

Recommended DC Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	2.7	3.0	3.3	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2		V_{CC} + 0.3	V
V_{IL}[1]	Input Low Voltage	-0.31[1]		0.6	V

Note: 1. Undershoot: V_{IL} = -1.5V for pulse width less than 30 ns. Undershoot is sampled, not 100% tested.

DC Electrical Characteristics

T_A = -40°C to 85°C

Symbol	Parameter	Test Condition		Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{SS} < V_{IN} < V_{CC}$		-1	1	µA
I_{LO}	Output Leakage Current	$V_{SS} < V_{OUT} < V_{CC}$, $\overline{SCS1} = V_{IH}$ or SCS2=V_{IL} or $\overline{SOE} = V_{IH}$ or $\overline{SWE}$ = VIL or $\overline{SUB} = V_{IH}$, $\overline{SLB} = V_{IH}$		-1	1	µA
I_{CC}	Operating Power Supply Current	$\overline{SCS1} = V_{IL}$, SCS2=V_{IH}, $V_{IN} = V_{IH}$ or V_{IL}, $I_{I/O}$ = 0 mA			5	mA
I_{CC1}	Average Operating Current	$\overline{SCS1} = V_{IL}$, SCS2 = V_{IH}, $V_{IN} = V_{IH}$ or V_{IL}, Cycle Time = Min 100% Duty, $I_{I/O}$ = 0 mA			35	mA
		$\overline{SCS1}$ < 0.2V, SCS2 > V_{CC} - 0.2V V_{IN} < 0.2V or $V_{IN} > V_{CC}$ - 0.2V, Cycle Time = 1 µs 100% Duty, $I_{I/O}$ = 0 mA			5	mA
I_{SB}	Standby Current (TTL Input)	$\overline{SCS1} = V_{IH}$ or SCS2 = V_{IL} or $\overline{SUB}$, $\overline{SLB} = V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}			0.5	mA
I_{SB1}	Standby Current (CMOS Input)	$\overline{SCS1} > V_{CC}$ - 0.2V or SCS2 < V_{SS} + 0.2V or $\overline{SUB}$, $\overline{SLB} > V_{CC}$ - 0.2V $V_{IN} > V_{CC}$ - 0.2V or $V_{IN} < V_{SS}$ + 0.2V	SL		4	µA
			LL		15	µA
V_{OL}	Output Low	I_{OL} = 0.1 mA			0.4	V
V_{OH}	Output High	I_{OH} = -0.1 mA		2.4		V

Capacitance[1]

(Temp = 25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max	Unit
C_{IN}	Input Capacitance (Add, $\overline{SCS1}$, SCS2, $\overline{SLB}$, $\overline{SUB}$, $\overline{SWE}$, $\overline{SOE}$)	V_{IN} = 0 V	8	pF
C_{OUT}	Output Capacitance (I/O)	$V_{I/O}$ = 0 V	10	pF

Note: 1. These parameters are sampled and not 100% tested.

AC Characteristics

T_A = -40°C to 85°C, Unless Otherwise Specified

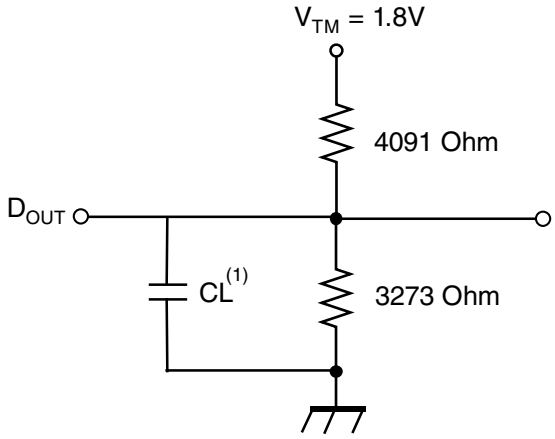
#	Symbol	Parameter	70 ns		Unit
			Min	Max	
1	t_{RC}	Read Cycle Time	70		ns
2	t_{AA}	Address Access Time		70	ns
3	t_{ACS}	Chip Select Access Time		70	ns
4	t_{OE}	Output Enable to Output Valid		35	ns
5	t_{BA}	$\overline{SLB}$, $\overline{SUB}$ Access Time		70	ns
6	t_{CLZ}	Chip Select to Output in Low Z	10		ns
7	t_{OLZ}	Output Enable to Output in Low Z	5		ns
8	t_{BLZ}	$\overline{SLB}$, $\overline{SUB}$ Enable to Output in Low Z	10		ns
9	t_{CHZ}	Chip Deselection to Output in High Z	0	30	ns
10	t_{OHZ}	Out Disable to Output in High Z	0	30	ns
11	t_{BHZ}	$\overline{SLB}$, $\overline{SUB}$ Disable to Output in High Z	0	30	ns
12	t_{OH}	Output Hold from Address Change	10		ns
13	t_{WC}	Write Cycle Time	70		ns
14	t_{CW}	Chip Selection to End of Write	60		ns
15	t_{AW}	Address Valid to End of Write	60		ns
16	t_{BW}	$\overline{SLB}$, $\overline{SUB}$ Valid to End of Write	60		ns
17	t_{AS}	Address Setup Time	0		ns
18	t_{WP}	Write Pulse Width	50		ns
19	t_{WR}	Write Recovery Time	0		ns
20	t_{WHZ}	Write to Output in High Z	0	20	ns
21	t_{DW}	Data to Write Time Overlap	30		ns
22	t_{DH}	Data Hold from Write Time	0		ns
23	t_{OW}	Output Active from End of Write	5		ns

AC Test Conditions

TA = -40°C to 85°C, Unless Otherwise Specified

Parameter		Value
Input Pulse Level		0.4V to 2.2V
Input Rise and Fall Time		5 ns
Input and Output Timing Reference Level		1.5V
Output Load	CL = 5 pF + 1 TTL Load	CL = 5 pF + 1 TTL Load
	CL = 30 pF + 1 TTL Load	CL = 30 pF + 1 TTL Load

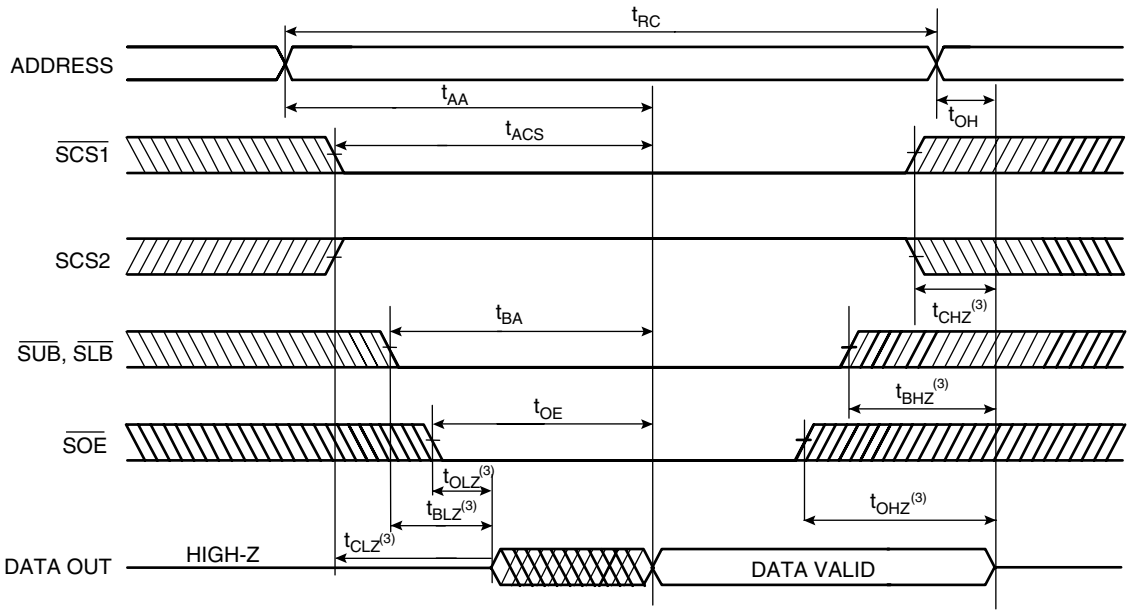
AC Test Loads



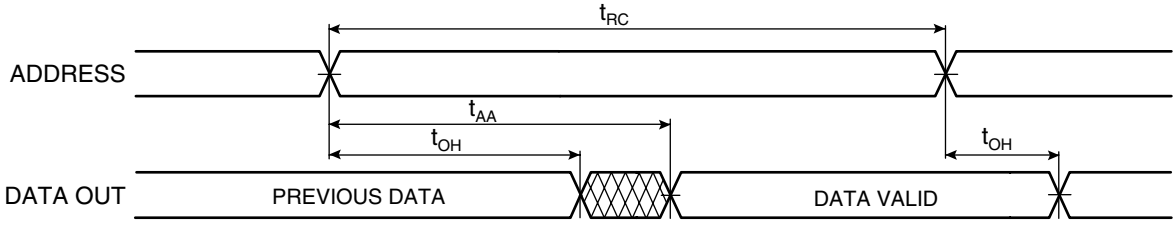
Note: Including jig and scope capacitance.

Timing Diagrams

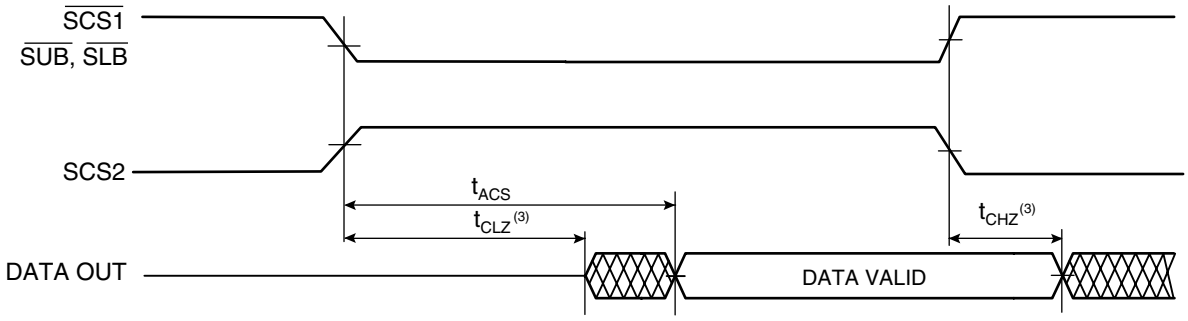
Read Cycle 1[1],[4]



Read Cycle 2[1],[2],[4]

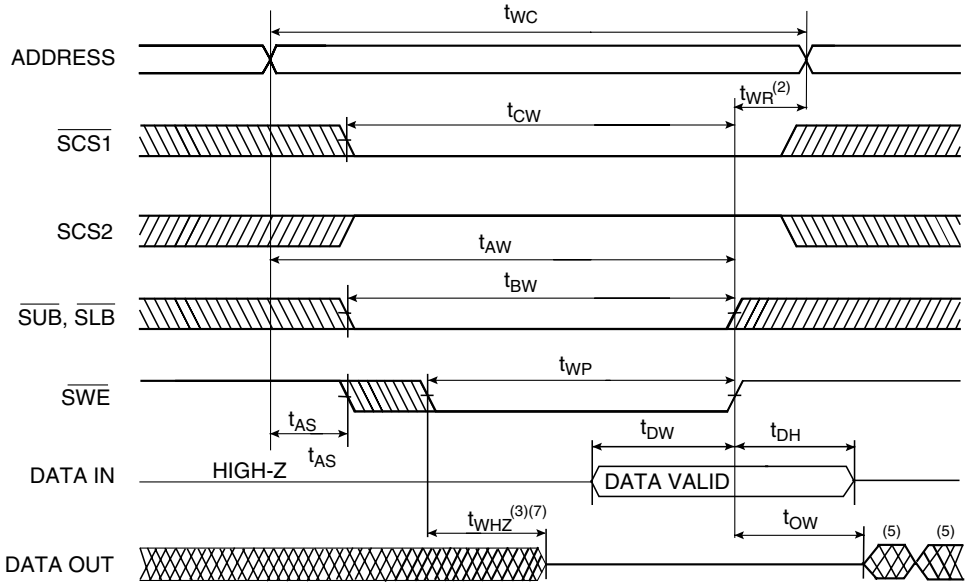


Read Cycle 3[1],[2],[4]

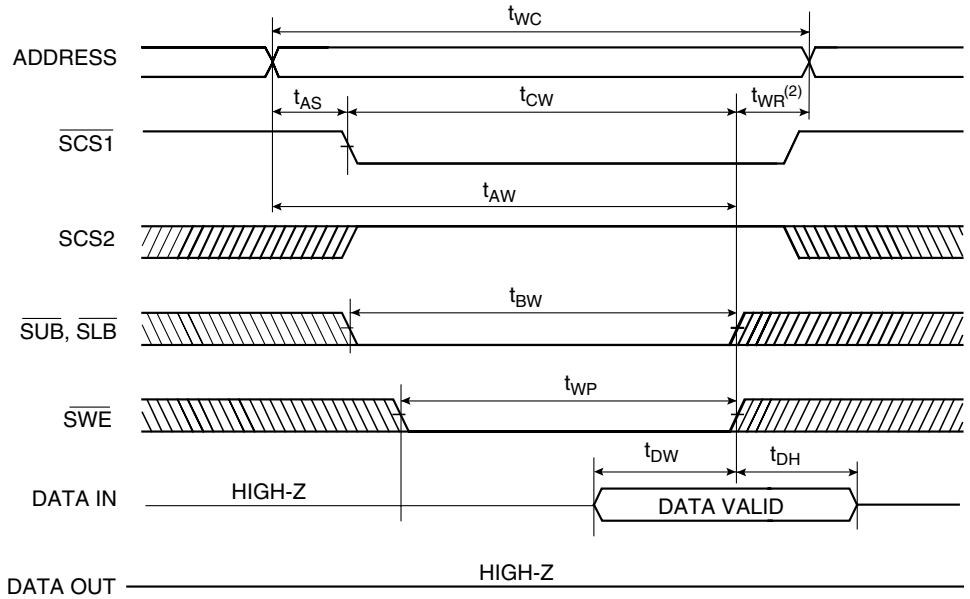


Notes:
1. Read Cycle occurs whenever a high on the $\overline{SWE}$ and $\overline{SOE}$ is low, while $\overline{SUB}$ and/or $\overline{SLB}$ and $\overline{SCS1}$ and SCS2 are in active status.
2. $\overline{SOE} = V_{IL}$.
3. Transition is measured + 200 mV from steady state voltage. This parameter is sampled and not 100% tested.
4. $\overline{SCS1}$ in high for the standby, low for active. SCS2 in low for the standby, high for active. $\overline{SUB}$ and $\overline{SLB}$ in high for the standby, low for active.

Write Cycle 1 ($\overline{SWE}$ Controlled)[1],[4],[8]



Write Cycle 2 ($\overline{SCS1}$, SCS2 Controlled)[1],[4],[8]



Notes:
1. A write occurs during the overlap of a low $\overline{SWE}$, a low $\overline{SCS1}$, a high SCS2 and a low $\overline{SUB}$ and/or $\overline{SLB}$.
2. t_{WR} is measured from the earlier of $\overline{SCS1}$, $\overline{SLB}$, $\overline{SUB}$, or $\overline{SWE}$ going high or SCS2 going low to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the $\overline{SCS1}$, $\overline{SLB}$ and $\overline{SUB}$ low transition and SCS2 high transition occur simultaneously with the $\overline{SWE}$ low transition or after the $\overline{SWE}$ transition, outputs remain in a high impedance state.
5. Q (data out) is the same phase with the write data of this write cycle.
6. Q (data out) is the read data of the next address.
7. Transition is measured + 200 mV from steady state. This parameter is sampled and not 100% tested.
8. $\overline{SCS1}$ in high for the standby, low for active SCS2 in low for the standby, high for active. $\overline{SUB}$ and $\overline{SLB}$ in high for the standby, low for active.

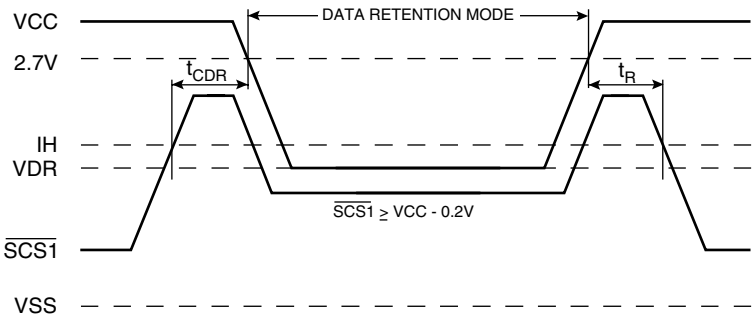
Data Retention Electric Characteristic

T_A = -40°C to 85°C

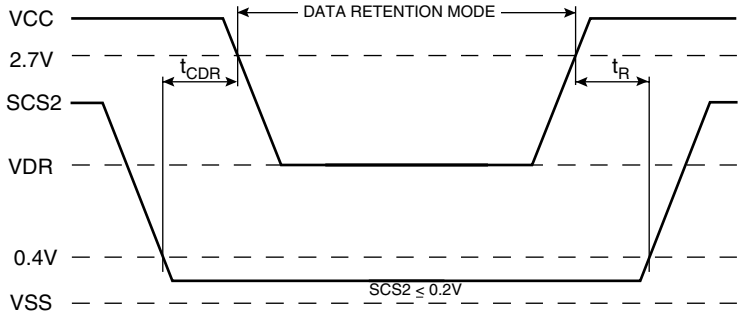
Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{SCS1} > V_{CC}$ - 0.2V or SCS2 < V_{SS} + 0.2V or $\overline{SUB}$, $\overline{SLB} > V_{CC}$ - 0.2V $V_{IN} > V_{CC}$ - 0.2V or $V_{IN} < V_{SS}$ + 0.2V		1.2		3.3	V
I_{CCDR}	Data Retention Current	Vcc=1.5V, $\overline{SCS1} > V_{CC}$ - 0.2V or SCS2 < V_{SS} + 0.2V or $\overline{SUB}$, $\overline{SLB} > V_{CC}$ - 0.2V $V_{IN} > V_{CC}$ - 0.2V or $V_{IN} < V_{SS}$ + 0.2V	SL		0.1	2	µA
			LL		0.1	10	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram		0			ns
t_R	Operating Recovery Time			t_{RC}			ns

Notes: 1. Typical values are under the condition of T_A = 25°C. Typical values are sampled and not 100% tested.
2. t_{RC} is read cycle time.

Data Retention Timing Diagram 1



Data Retention Timing Diagram 2



8-megabit SRAM Description

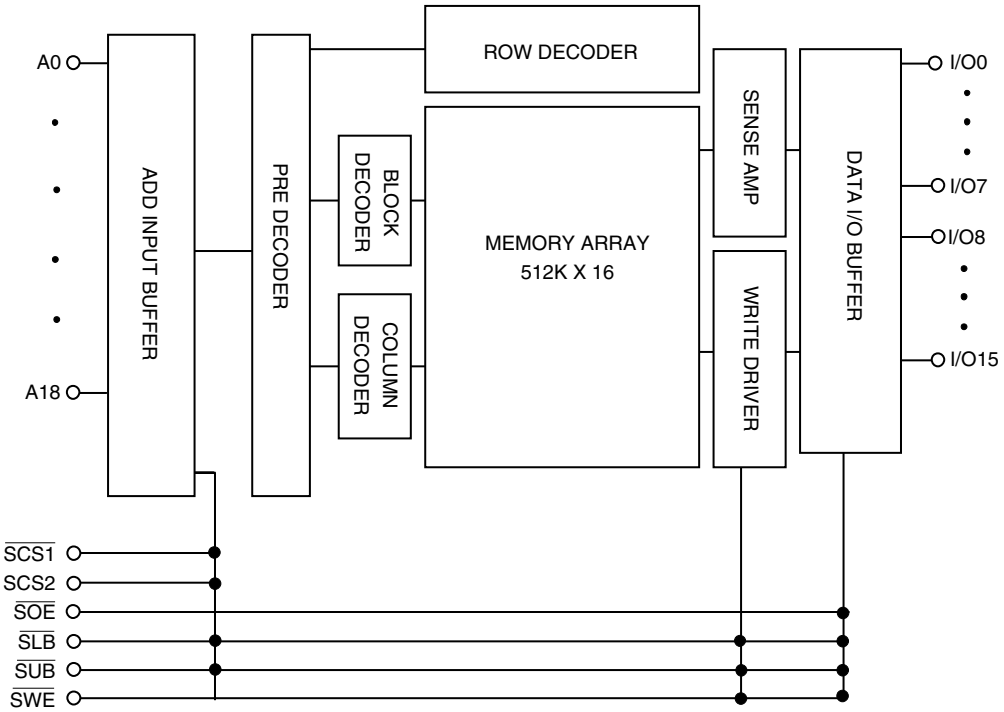
The 8-megabit SRAM is a high-speed, super low-power CMOS SRAM organized as 512K words by 16 bits. The SRAM uses high-performance full CMOS process technology and is designed for high-speed and low-power circuit technology. It is particularly well-suited for the high-density low-power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.2V.

Features

- **Fully Static Operation and Tri-state Output**
- **TTL Compatible Inputs and Outputs**
- **Battery Backup**
  - **1.2V (Min) Data Retention**

Voltage (V)	Speed (ns)	Operation Current/I_{CC} (mA) (Max)	Standby Current (µA) (Max)	Temperature (°C)
2.7 - 3.3	70	5	15	-40 - 85

Block Diagram



Absolute Maximum Ratings[1]

Symbol	Parameter	Rating	Unit
V_{IN}, V_{OUT}	Input/Output Voltage	-0.3 to 3.6	V
V_{CC}	Power Supply	-0.3 to 4.6	V
T_A	Operating Temperature	-40 to 85	°C
T_{STG}	Storage Temperature	-55 to 150	°C
P_D	Power Dissipation	1.0	W

Note: 1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

Truth Table

$\overline{SCS1}$	SCS2	$\overline{SWE}$	$\overline{SOE}$	$\overline{SLB}$[2]	$\overline{SUB}$[2]	Mode	I/O Pin		Power
							I/O0 - I/O7	I/O8 - I/O15	
H[1]	X	X	X	X	X	Deselected	High-Z	High-Z	Standby
X[1]	L								
X	X			H	H				
L[1]	H	H	H	L	H	Output Disabled	High-Z	High-Z	Active
				H	L				
				L	L				
L	H	L	X	L	H	Write	D_{IN}	High-Z	Active
				H	L		High-Z	D_{IN}	
				L	L		D_{IN}	D_{IN}	
							D_{IN}	High-Z	
L	H	H	L	L	H	Read	D_{OUT}	High-Z	Active
				H	L		High-Z	D_{OUT}	
				L	L		D_{OUT}	D_{OUT}	
							D_{OUT}	High-Z	

Notes: 1. H = V_{IH}, L = V_{IL}, X = Don't Care (V_{IL} or V_{IH})
2. $\overline{SUB}$, $\overline{SLB}$ (Upper, Lower Byte Enable). These active LOW inputs allow individual bytes to be written or read. When $\overline{SLB}$ is LOW, data is written or read to the lower byte, I/O0 - I/O7. When $\overline{SUB}$ is LOW, data is written or read to the upper byte, I/O8 - I/O15.

Recommended DC Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	2.7	3.0	3.3	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2		V_{CC} + 0.3	V
V_{IL}[1]	Input Low Voltage	-0.31[1]		0.6	V

Note: 1. Undershoot: V_{IL} = -1.5V for pulse width less than 30 ns. Undershoot is sampled, not 100% tested.

DC Electrical Characteristics

T_A = -40°C to 85°C

Symbol	Parameter	Test Condition		Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{SS} < V_{IN} < V_{CC}$		-1	1	µA
I_{LO}	Output Leakage Current	$V_{SS} < V_{OUT} < V_{CC}$, $\overline{SCS1} = V_{IH}$ or $\overline{SCS2}=V_{IL}$ or $\overline{SOE} = V_{IH}$ or $\overline{SWE}$ = VIL or $\overline{SUB} = V_{IH}$, $\overline{SLB} = V_{IH}$		-1	1	µA
I_{CC}	Operating Power Supply Current	$\overline{SCS1} = V_{IL}$, $SCS2=V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL}, $I_{I/O}$ = 0 mA			5	mA
I_{CC1}	Average Operating Current	$\overline{SCS1} = V_{IL}$, $SCS2 = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL}, Cycle Time = Min 100% Duty, $I_{I/O}$ = 0 mA			40	mA
		$\overline{SCS1} < 0.2V$, $SCS2 > V_{CC} - 0.2V$ $V_{IN} < 0.2V$ or $V_{IN} > V_{CC} - 0.2V$, Cycle Time = 1 µs 100% Duty, $I_{I/O}$ = 0 mA			5	mA
I_{SB}	Standby Current (TTL Input)	$\overline{SCS1} = V_{IH}$ or $SCS2 = V_{IL}$ or $\overline{SUB}$, $\overline{SLB} = V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}			0.5	mA
I_{SB1}	Standby Current (CMOS Input)	$\overline{SCS1} > V_{CC} - 0.2V$ or $SCS2 < V_{SS} + 0.2V$ or $\overline{SUB}$, $\overline{SLB} > V_{CC} - 0.2V$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < V_{SS} + 0.2V$	LL		25	µA
V_{OL}	Output Low	I_{OL} = 0.1 mA			0.4	V
V_{OH}	Output High	I_{OH} = -0.1 mA		2.4		V

Capacitance[1]

(Temp = 25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max	Unit
C_{IN}	Input Capacitance (Add, $\overline{SCS1}$, SCS2, $\overline{SLB}$, $\overline{SUB}$, $\overline{SWE}$, $\overline{SOE}$)	V_{IN} = 0 V	8	pF
C_{OUT}	Output Capacitance (I/O)	$V_{I/O}$ = 0 V	10	pF

Note: 1. These parameters are sampled and not 100% tested.

AC Characteristics

T_A = -40°C to 85°C, Unless Otherwise Specified

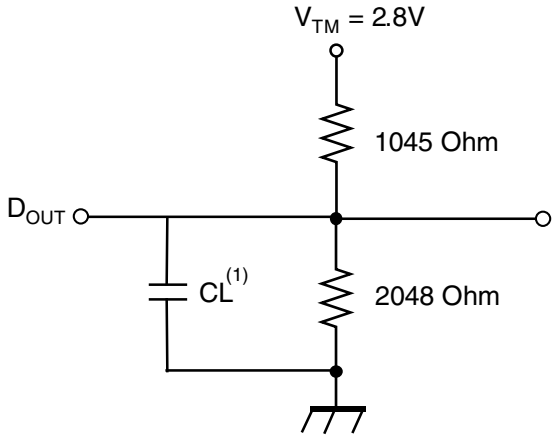
#	Symbol	Parameter	70 ns		Unit
			Min	Max	
1	t_{RC}	Read Cycle Time	70		ns
2	t_{AA}	Address Access Time		70	ns
3	t_{ACS}	Chip Select Access Time		70	ns
4	t_{OE}	Output Enable to Output Valid		35	ns
5	t_{BA}	$\overline{SLB}$, $\overline{SUB}$ Access Time		70	ns
6	t_{CLZ}	Chip Select to Output in Low Z	10		ns
7	t_{OLZ}	Output Enable to Output in Low Z	5		ns
8	t_{BLZ}	$\overline{SLB}$, $\overline{SUB}$ Enable to Output in Low Z	10		ns
9	t_{CHZ}	Chip Deselection to Output in High Z	0	30	ns
10	t_{OHZ}	Out Disable to Output in High Z	0	30	ns
11	t_{BHZ}	$\overline{SLB}$, $\overline{SUB}$ Disable to Output in High Z	0	30	ns
12	t_{OH}	Output Hold from Address Change	10		ns
13	t_{WC}	Write Cycle Time	70		ns
14	t_{CW}	Chip Selection to End of Write	60		ns
15	t_{AW}	Address Valid to End of Write	60		ns
16	t_{BW}	$\overline{SLB}$, $\overline{SUB}$ Valid to End of Write	60		ns
17	t_{AS}	Address Setup Time	0		ns
18	t_{WP}	Write Pulse Width	50		ns
19	t_{WR}	Write Recovery Time	0		ns
20	t_{WHZ}	Write to Output in High Z	0	20	ns
21	t_{DW}	Data to Write Time Overlap	30		ns
22	t_{DH}	Data Hold from Write Time	0		ns
23	t_{OW}	Output Active from End of Write	5		ns

AC Test Conditions

TA = -40°C to 85°C, Unless Otherwise Specified

Parameter		Value
Input Pulse Level		0.4V to 2.2V
Input Rise and Fall Time		5 ns
Input and Output Timing Reference Level		1.5V
Output Load	CL = 5 pF + 1 TTL Load	CL = 5 pF + 1 TTL Load
	CL = 30 pF + 1 TTL Load	CL = 30 pF + 1 TTL Load

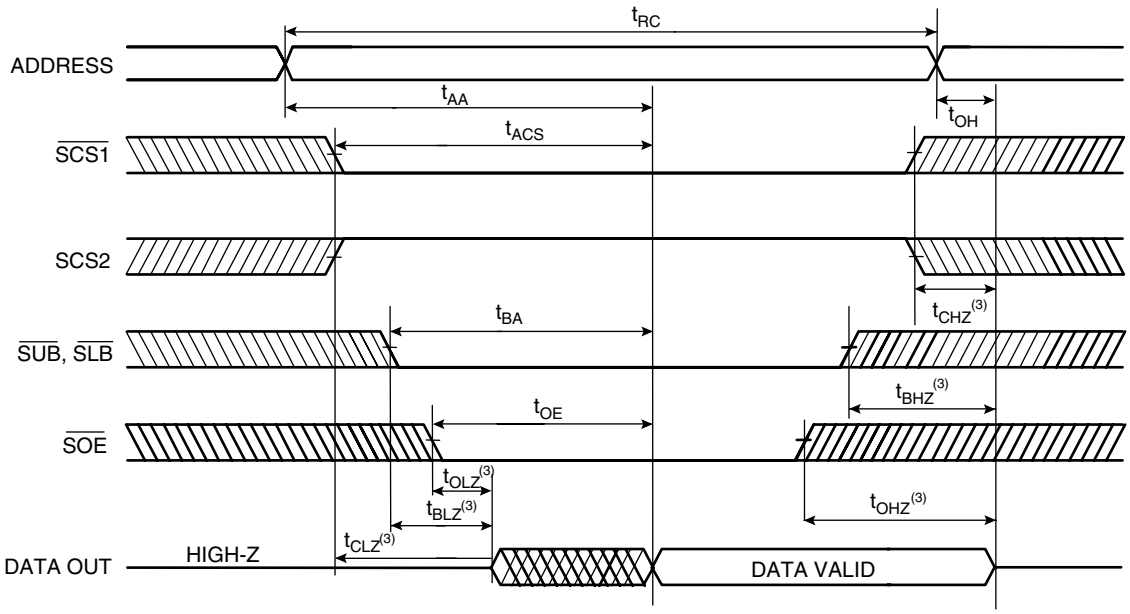
AC Test Loads



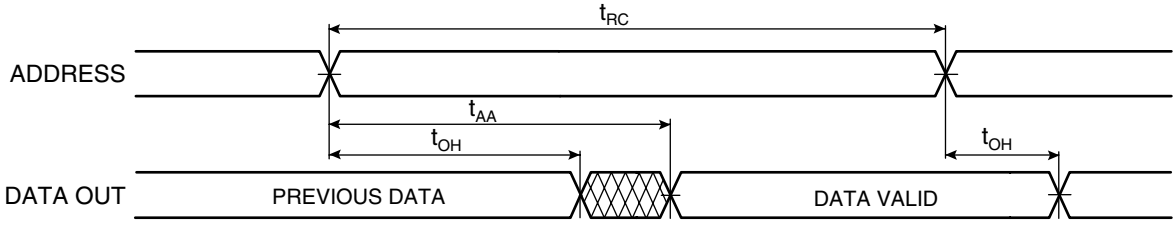
Note: Including jig and scope capacitance.

Timing Diagrams

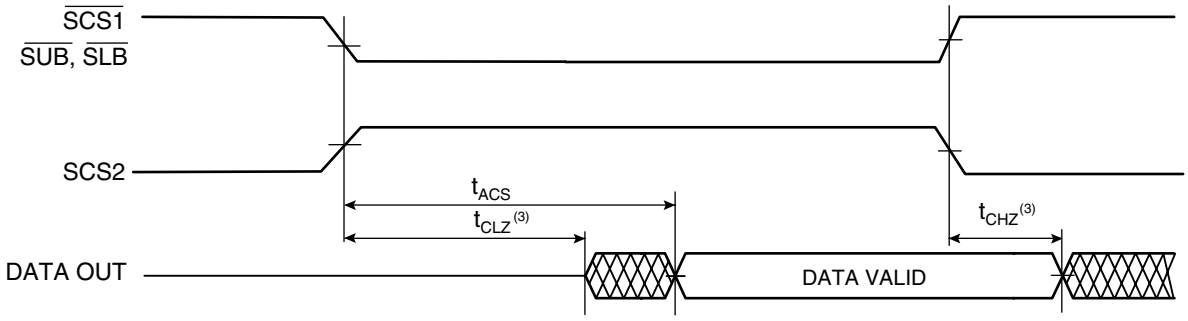
Read Cycle 1[1],[4]



Read Cycle 2[1],[2],[4]

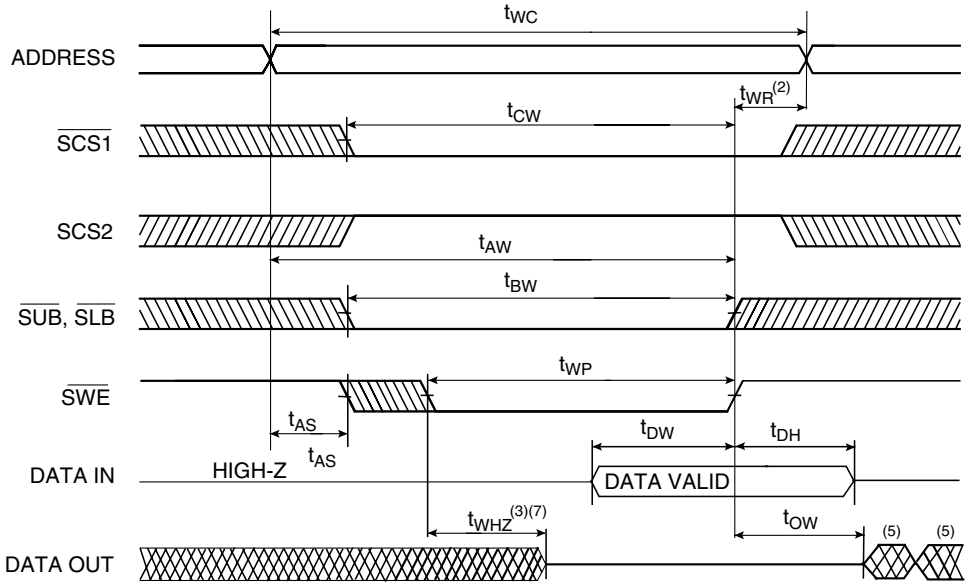


Read Cycle 3[1],[2],[4]

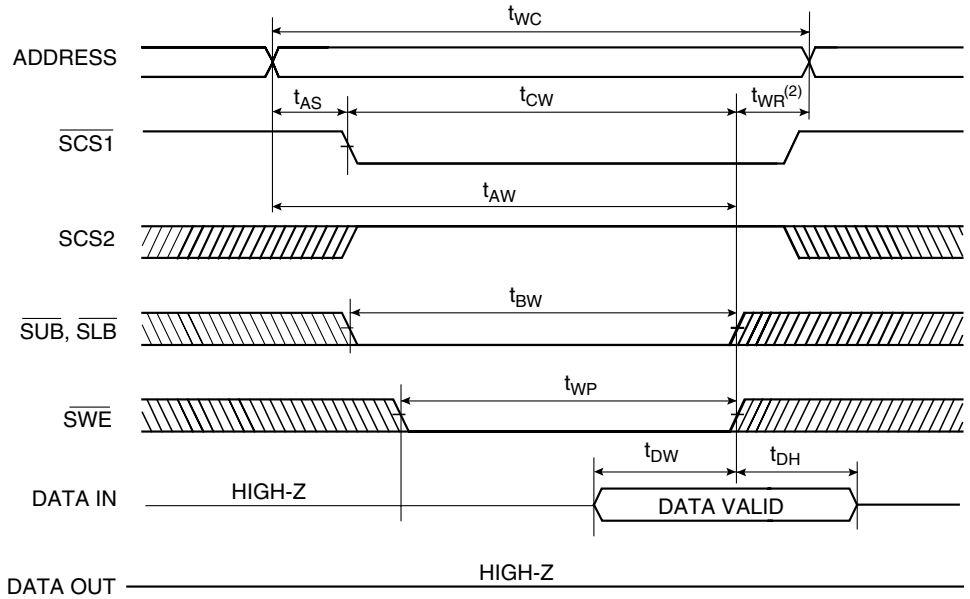


Notes:
1. Read Cycle occurs whenever a high on the $\overline{SWE}$ and $\overline{SOE}$ is low, while $\overline{SUB}$ and/or $\overline{SLB}$ and $\overline{SCS1}$ and SCS2 are in active status.
2. $\overline{SOE} = V_{IL}$.
3. Transition is measured + 200 mV from steady state voltage. This parameter is sampled and not 100% tested.
4. $\overline{SCS1}$ in high for the standby, low for active. SCS2 in low for the standby, high for active. $\overline{SUB}$ and $\overline{SLB}$ in high for the standby, low for active.

Write Cycle 1 ($\overline{SWE}$ Controlled)[1],[4],[8]



Write Cycle 2 ($\overline{SCS1}$, SCS2 Controlled)[1],[4],[8]



Notes:
1. A write occurs during the overlap of a low $\overline{SWE}$, a low $\overline{SCS1}$, a high SCS2 and a low $\overline{SUB}$ and/or $\overline{SLB}$.
2. t_{WR} is measured from the earlier of $\overline{SCS1}$, $\overline{SLB}$, $\overline{SUB}$, or $\overline{SWE}$ going high or SCS2 going low to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the $\overline{SCS1}$, $\overline{SLB}$ and $\overline{SUB}$ low transition and SCS2 high transition occur simultaneously with the $\overline{SWE}$ low transition or after the $\overline{SWE}$ transition, outputs remain in a high impedance state.
5. Q (data out) is the same phase with the write data of this write cycle.
6. Q (data out) is the read data of the next address.
7. Transition is measured + 200 mV from steady state. This parameter is sampled and not 100% tested.
8. $\overline{SCS1}$ in high for the standby, low for active SCS2 in low for the standby, high for active. $\overline{SUB}$ and $\overline{SLB}$ in high for the standby, low for active.

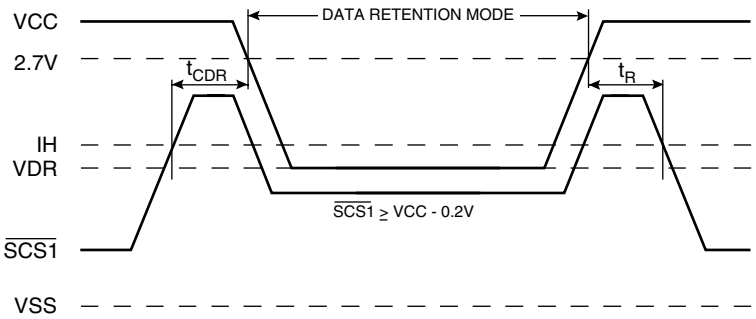
Data Retention Electric Characteristic

T_A = -40°C to 85°C

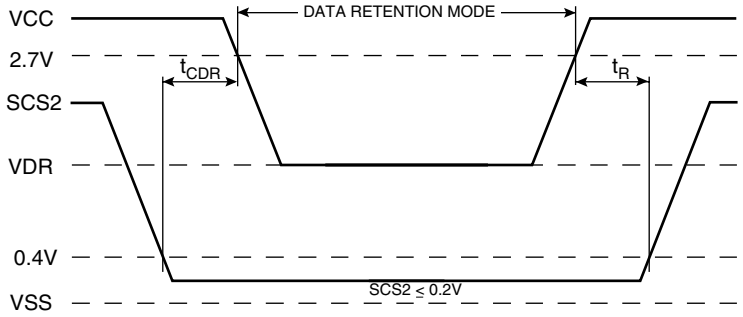
Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{SCS1} > V_{CC}$ - 0.2V or SCS2 < V_{SS} + 0.2V or $\overline{SUB}$, $\overline{SLB} > V_{CC}$ - 0.2V $V_{IN} > V_{CC}$ - 0.2V or $V_{IN} < V_{SS}$ + 0.2V		1.2		3.3	V
I_{CCDR}	Data Retention Current	Vcc=1.5V, $\overline{SCS1} > V_{CC}$ - 0.2V or SCS2 < V_{SS} + 0.2V or $\overline{SUB}$, $\overline{SLB} > V_{CC}$ - 0.2V $V_{IN} > V_{CC}$ - 0.2V or $V_{IN} < V_{SS}$ + 0.2V	SL		0.1	2	µA
			LL		0.1	10	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram		0			ns
t_R	Operating Recovery Time			t_{RC}			ns

Notes: 1. Typical values are under the condition of T_A = 25°C. Typical values are sampled and not 100% tested.
2. t_{RC} is read cycle time.

Data Retention Timing Diagram 1



Data Retention Timing Diagram 2



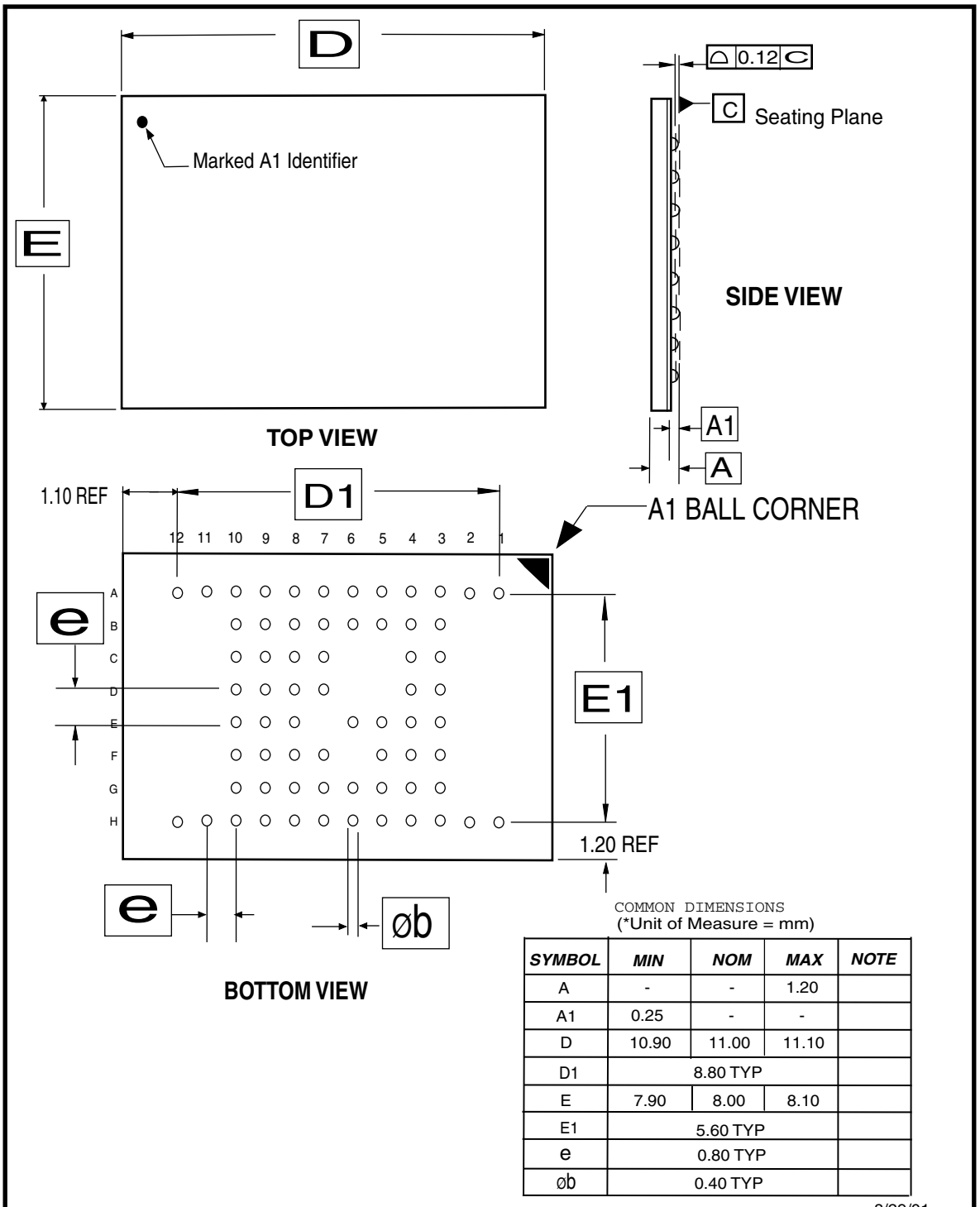
AT52BR3224T Ordering Information

t_{ACC} (ns)	Ordering Code	Flash Boot Block	Flash Plane Architecture	SRAM	Package	Operation Range
85	AT52BR3224-85CI	Bottom	32M	256K x 16	66C4	Industrial (-40° to 85°C)
85	AT52BR3224T-85CI	Top	32M	256K x 16	66C4	Industrial (-40° to 85°C)
85	AT52BR3228-85CI	Bottom	32M	512K x 16	66C4	Industrial (-40° to 85°C)
85	AT52BR3228T-85CI	Top	32M	512K x 16	66C4	Industrial (-40° to 85°C)

Package Type	
66C4	66-ball, Plastic Chip-size Ball Grid Array Package (CBGA)

Packaging Information

66C4 – CBGA



COMMON DIMENSIONS
(*Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.25	-	-	
D	10.90	11.00	11.10	
D1		8.80 TYP		
E	7.90	8.00	8.10	
E1		5.60 TYP		
e		0.80 TYP		
øb		0.40 TYP		

8/29/01

	TITLE:	DRAWING NO.	REV
2325 Orchard Parkway San Jose, CA 95131	*66C4, 66 ball (12X8 Array), 11x8x1.2mm body, 0.8mm ball pitch* *Chip-scale Ball Grid Array package (CBGA)*	*66C4*	*A*

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