Features

- Incorporates the ARM7TDMI™ ARM® Thumb® Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - Embedded ICE (In-Circuit Emulation)
- 4K Bytes Internal RAM
- Fully-programmable External Bus Interface (EBI)
  - Maximum External Address Space of 64M Bytes
  - Up to Eight Chip Selects
  - Software Programmable 8/16-bit External Data Bus
- Eight-level Priority, Individually Maskable, Vectored Interrupt Controller
  - 4 External Interrupts, Including a High-priority Low-latency Interrupt Request
- 32 Programmable I/O Lines
- Three-channel 16-bit Timer/Counter
  - Three External Clock Inputs
  - Two Multi-purpose I/O Pins per Channel
- Two USARTs
  - Two Dedicated Peripheral Data Controller (PDC) Channels per USART
- Programmable Watchdog Timer
- Low-power Idle Mode
- Fully Static Operation: 0 Hz to 33 MHz
- 2.7V to 3.6V Operating Range
- -40°C to 85°C Operating Temperature Range
- Available in a 100-lead TQFP Package

Description

The AT91M40400 is a member of the Atmel AT91 16/32-bit microcontroller family which is based on the ARM7TDMI processor core. This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications. The AT91 ARM-based microcontroller unit family also features Atmel's high-density, nonvolatile memory technology. The on-chip Flash program memory is in-system programmable.

The AT91M40400 has a direct connection to off-chip memory, including Flash, through the External Bus Interface (EBI).

The device is manufactured using Atmel's high-density CMOS technology. By combining the ARM7TDMI processor core with an on-chip RAM and a wide range of peripheral functions on a monolithic chip, the AT91M40400 is a powerful microcontroller that offers a flexible, cost-effective solution to many compute-intensive embedded control applications.

AT91 ARM® Thumb® 16/32-bit Microcontroller

AT91M40400

Electrical and Mechanical Characteristics

Rev. 1078C–12/00

Pin Configuration

Figure 1. AT91M40400 Pinout (Top View)

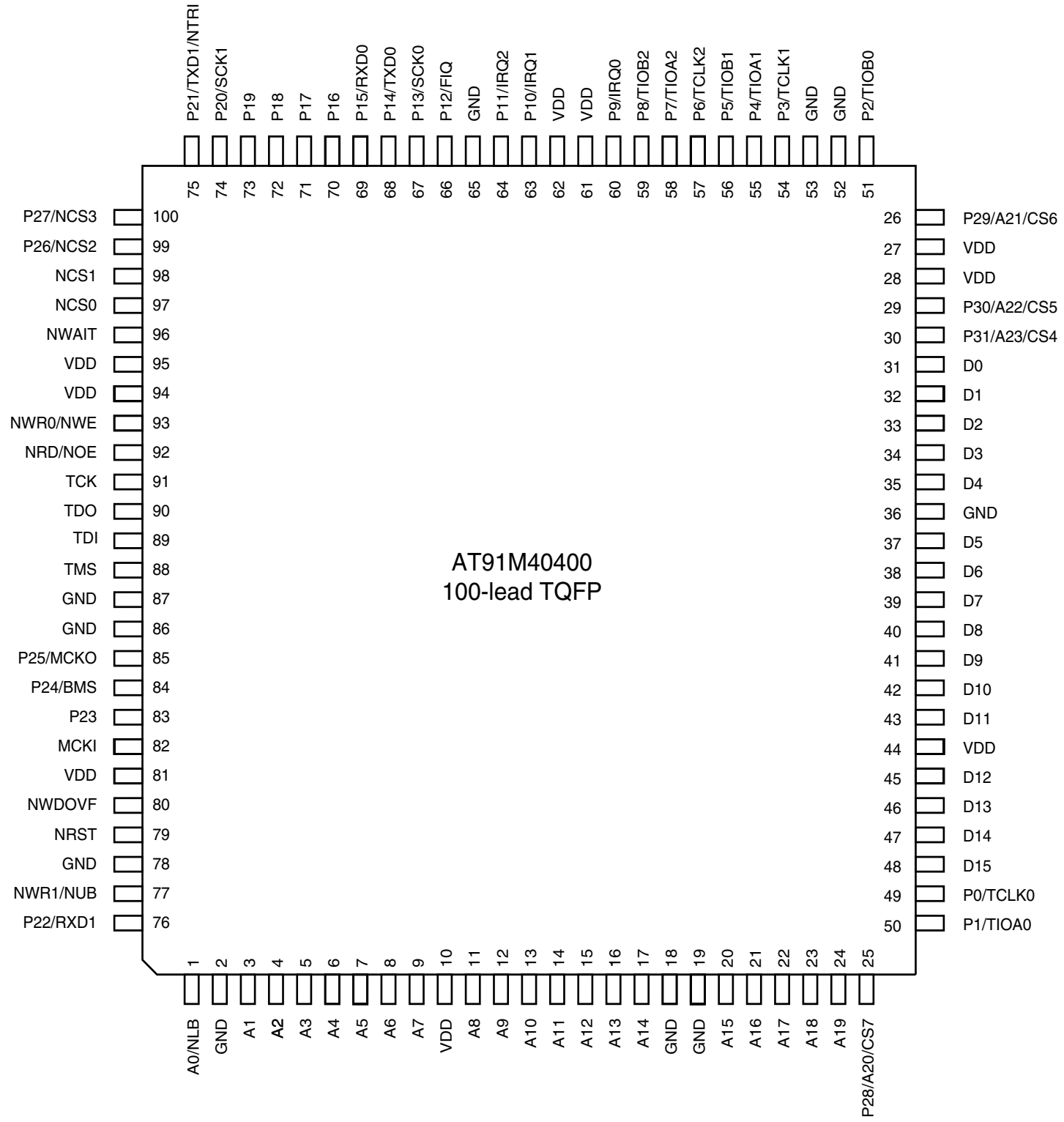


Table 1. AT91M40400 Pin Description

Module	Name	Function	Type	Active Level	Comments
EBI	A0 - A23	Address Bus	Output	–	All valid after reset
	D0 - D15	Data Bus	I/O	–	
	NCS0 - NCS3	Chip Select	Output	Low	
	CS4 - CS7	Chip Select	Output	High	A23 - A20 after reset
	NWR0	Lower Byte 0 Write Signal	Output	Low	Used in Byte Write Option
	NWR1	Upper Byte 1 Write Signal	Output	Low	Used in Byte Write Option
	NRD	Read Signal	Output	Low	Used in Byte Write Option
	NWE	Write Enable	Output	Low	Used in Byte Select Option
	NOE	Output Enable	Output	Low	Used in Byte Select Option
	NUB	Upper Byte Select	Output	Low	Used in Byte Select Option
	NLB	Lower Byte Select	Output	Low	Used in Byte Select Option
	NWAIT	Wait Input	Input	Low	
	BMS	Boot Mode Select	Input	–	Sampled during reset
AIC	FIQ	Fast Interrupt Request	Input	–	PIO - controlled after reset
	IRQ0-IRQ2	External Interrupt Request	Input	–	PIO - controlled after reset
Timer	TCLK0-TCLK2	Timer External Clock	Input	–	PIO - controlled after reset
	TIOA0-TIOA2	Multipurpose Timer I/O Pin A	I/O	–	PIO - controlled after reset
	TIOB0-TIOB2	Multipurpose Timer I/O Pin B	I/O	–	PIO - controlled after reset
USART	SCK0-SCK1	External Serial Clock	I/O	–	PIO - controlled after reset
	TXD0-TXD1	Transmit Data Output	Output	–	PIO - controlled after reset
	RXD0-RXD1	Receive Data Input	Input	–	PIO - controlled after reset
PIO	P0-P31	Parallel IO Line	I/O	–	
WD	NWDOVF	Watchdog Overflow	Output	Low	Open drain
Clock	MCKI	Master Clock Input	Input	–	Schmidt trigger
	MCKO	Master Clock Output	Output	–	
Reset	NRST	Hardware Reset Input	Input	Low	Schmidt trigger, internal pull-up
	NTRI	Tri-state Mode Select	Input	Low	Sampled during reset
ICE	TMS	Test Mode Select	Input	–	Schmidt trigger, internal pull-up
	TDI	Test Data Input	Input	–	Schmidt trigger, internal pull-up
	TDO	Test Data Output	Output	–	
	TCK	Test Clock	Input	–	Schmidt trigger, internal pull-up
Power	VDD	Power			
	GND	Ground			

Absolute Maximum Ratings*

Operating Temperature (Commercial)	0 to +70°C
Operating Temperature (Industrial)	-40°C to +85°C
Voltage on any input Pin with respect to Ground	-0.5V to +5.5V
Maximum Operating Voltage	4.6V
DC Output Current	2 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{DD} = 2.7V to 3.6V unless otherwise specified. All pads are 5V tolerant.

Table 2. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	V_{DD} = 2.7V to 3.6V	-0.5		0.3 x V_{DD}	V
V_{IH}	Input High Voltage	V_{DD} = 2.7V to 3.6V	0.7 x V_{DD}		V_{DD} + 0.5 or 5.5	V
V_{OL}	Output Low Voltage	I_{OL} = 0.8 mA, V_{DD} = 3.0V			0.1	V
V_{OH}	Output High Voltage	I_{OH} = 0.8 mA, V_{DD} = 3.0V	V_{DD} - 0.1			V
I_{OH}	Output Source Current	V_{DD} = 3.0V, V_{OH} = 2.4V			2	mA
I_{OL}	Output Sink Current	V_{DD} = 3.0V, V_{OL} = 0.4V			2	mA
I_{LEAK}	Input Leakage Current				100	nA
I_{PULL}	Input Pull-up Current	V_{DD} = 3.3V, V_{IN} = 0	-400		-80	µA
I_{CAP}	Input Capacitance for all Pins				12	pF
I_{SC}	Static Current	V_{DD} = 3.6V, MCKI = 0 Hz All inputs driven, TMS, TDI, TCK, NRST = 1		30		µA

Power Supply Current

The following table shows results of measurements peformed at typical conditions (V_{DD} = 3.3V and T_A = 25°C).

Table 3. Power Consumption

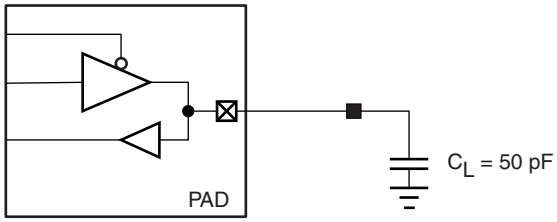
Mode	Conditions	Typ	Unit
Reset	NRST = 0	1.08	mW/MHz
Normal	Fetch in Internal SRAM	1.42	mW/MHz
Idle	–	0.63	mW/MHz

Conditions

Environment Constraints

The output delays are valid for a capacitive load of 50 pF as shown in Figure 2.

Figure 2. Output/Bi-directional Pad Capacitive Load



Timing Results

The output delays are for a capacitive load of 50 pF as shown in Figure 2 above.

In order to obtain the timing for other capacitance values, the following equation should be used:

$$t = t_{datasheet} + ""factor \times (C_{load} - 50\ \text{pF})$$

Table 4. Derating Factor Due to Capacitive Load Variation

Parameter	Commercial	Industrial	Units
Factor	0.052	0.058	ns/pF

Clock Waveforms

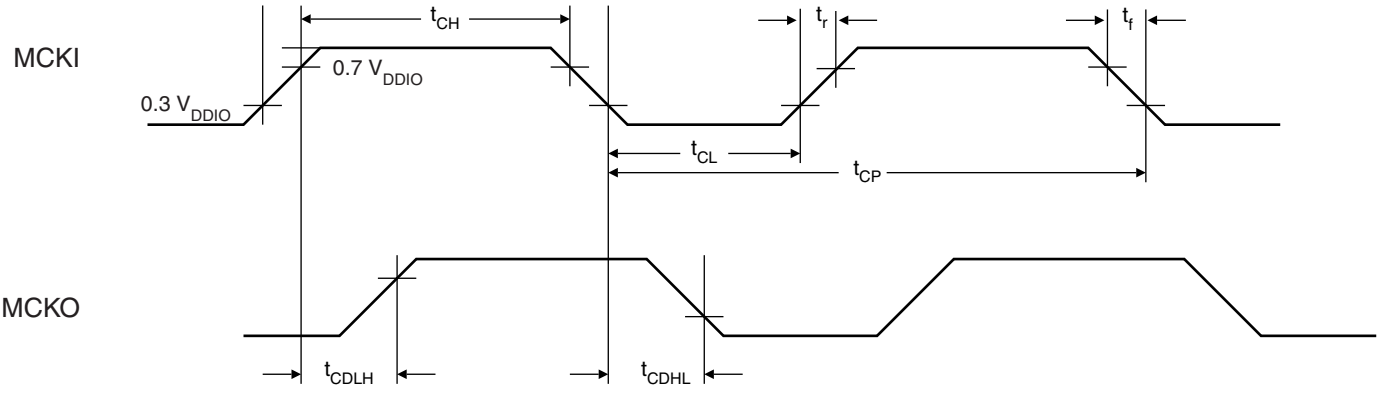
Table 5. Clock Waveform Parameters

Symbol	Parameter	Minimum		Maximum		Units
		25 MHz	33 MHz	25 MHz	33 MHz	
$1/t_{CP}$	Oscillator Frequency			25	33	MHz
t_{CP}	Main Clock Period	40	30			ns
t_{CH}	High Time	17	12			ns
t_{CL}	Low Time	17	12			ns
t_r	Rising Edge			TBD	TBD	ns
t_f	Falling Edge			TBD	TBD	ns

Table 6. Clock Propagation Times

Symbol	Parameter	Maximum		Units
		25 MHz	33 MHz	
t_{CDLH}	Rising Edge Propagation Time	12	9	ns
t_{CDHL}	Falling Edge Propagation Time	12	9	ns

Figure 3. Clock Waveform



AC Characteristics

The following tables refer to Figure 4.

Table 7. General-purpose EBI Signals

Symbol	Parameter	Minimum		Maximum		Units
		25 MHz	33 MHz	25 MHz	33 MHz	
EBI_1	MCKI Falling to NUB Valid	4	4	16	11	ns
EBI_2	MCKI Falling to NLB/A0 Valid	6	6	22	14	ns
EBI_3	MCKI Falling to A7 - A1 Valid	6	6	22	15	ns
EBI_4	MCKI Falling to A23 - A8 Valid	6	6	21	14	ns
EBI_5	MCKI Falling to Chip Select	5	5	21	14	ns
EBI_6	NWAIT Setup before MCKI Rising	4	4	8	6	ns
EBI_7	NWAIT Hold after MCKI Rising	1	1	5	4	ns

Table 8. EBI Write Signals

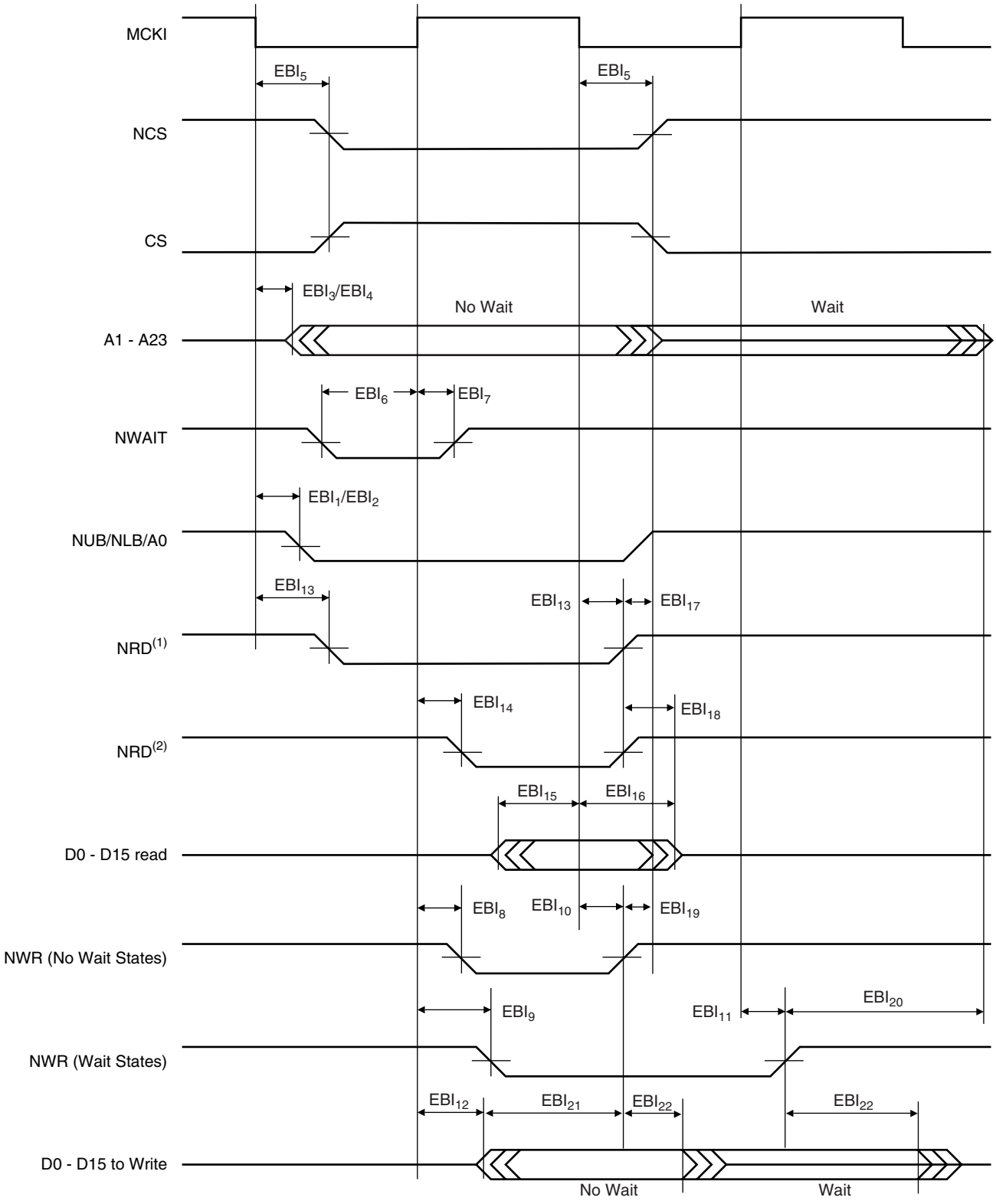
Symbol	Parameter	Minimum		Maximum		Units
		25 MHz	33 MHz	25 MHz	33 MHz	
EBI_8	MCKI Rising to NWR Active (No Wait States)	3	3	14	10	ns
EBI_9	MCKI Rising to NWR Active (Wait States)	3	3	14	10	ns
EBI_{10}	MCKI Falling to NWR Inactive (No Wait States)	4	4	16	11	ns
EBI_{11}	MCKI Rising to NWR Inactive (Wait States)	4	4	16	11	ns
EBI_{12}	MCKI Rising to D0 - D15 Out Valid	5	5	20	14	ns
EBI_{19}	NWR High to A23 - A1, NUB/NLB/A0, NCS, CS changes (No Wait States)	TBD	TBD			ns
EB_{20}	NWR High to A23 - A1, NCS, CS Changes (Wait States)	$t_{CP}/2$	$t_{CP}/2$			ns
EBI_{21}	Data Out Valid before NWR High	TBD	TBD			ns
EBI_{22}	Data Out Valid after NWR High (No Wait States)	TBD	TBD			ns
EBI_{23}	Data Out Valid after NWR High (Wait States)	$t_{CP}/2$	$t_{CP}/2$			ns

Table 9. EBI Read Signals

Symbol	Parameter	Minimum		Maximum		Units
		25 MHz	33 MHz	25 MHz	33 MHz	
EBI_{13}	MCKI Falling to NRD Valid(1)	4	4	15	10	ns
EBI_{14}	MCKI Rising to NRD Valid(2)	4	4	15	10	ns
EBI_{15}	D0 - D15 in Setup before MCKI Falling	2	2	3	3	ns
EBI_{16}	D0 - D15 in Hold after MCKI Falling	1	1	2	2	ns
EBI_{17}	NRD High to A23 - A1, NCS, CS Changes	TBD	TBD			ns
EBI_{18}	Data Hold after NRD High	TBD	TBD			ns

Notes: 1. Early Read Protocol
2. Standard Read Protocol

Figure 4. EBI Signals Relative to MCKI



Notes: 1. Early Read Protocol
2. Standard Read Protocol

Peripheral Signals

USART Signals

The inputs have to meet the minimum pulse width and period constraints shown in Table 10 and Table 11, and represented in Figure 5.

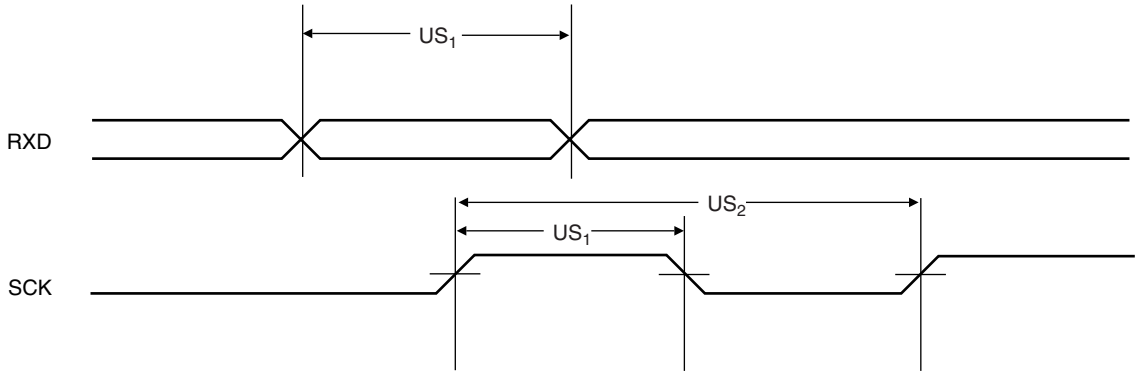
Table 10. USART Input Minimum Pulse Width

Symbol	Parameter	Minimum Pulse Width	Units
US_1	SCK/RXD Minimum Pulse Width	$3(t_{CP}/2)$	ns

Table 11. USART Minimum Input Period

Symbol	Parameter	Minimum Input Period	Units
US_2	SCK Minimum Input Period	$5(t_{CP}/2)$	ns

Figure 5. USART Signals



Timer/Counter Signals

Due to internal synchronization of input signals, there is a delay between an input event and a corresponding output event. This delay is $3(t_{CP})$ in Waveform Event Detection mode and $4(t_{CP})$ in Waveform Total Count Detection mode. The inputs have to meet the minimum pulse width and minimum input period shown in Tables 12 and 13, and as represented in Figure 6.

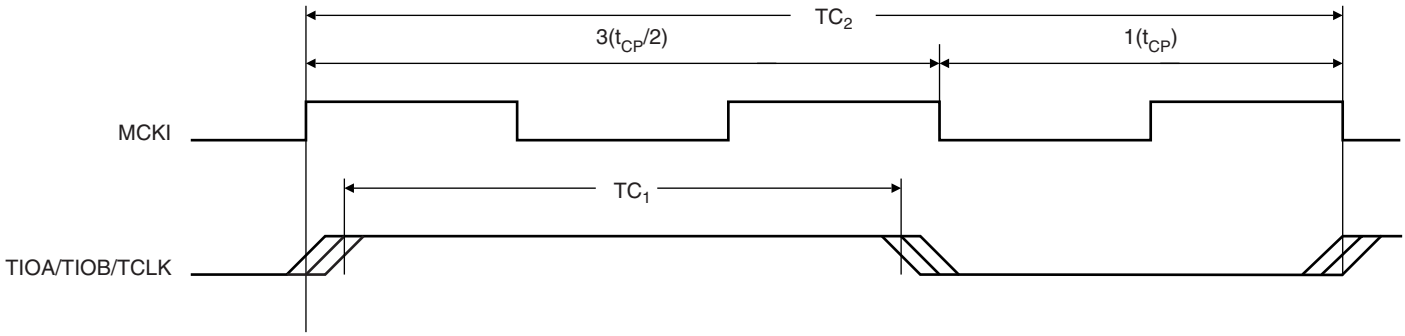
Table 12. Timer Input Minimum Pulse Width

Symbol	Parameter	Minimum Pulse Width	Units
TC_1	TCLK/TIOA/TIOB Minimum Pulse-Width	$3(t_{CP}/2)$	ns

Table 13. Timer Input Minimum Period

Symbol	Parameter	Minimum Input Period	Units
TC_2	TCLK/TIOA/TIOB Minimum Input Period	$5(t_{CP}/2)$	ns

Figure 6. Timer Input

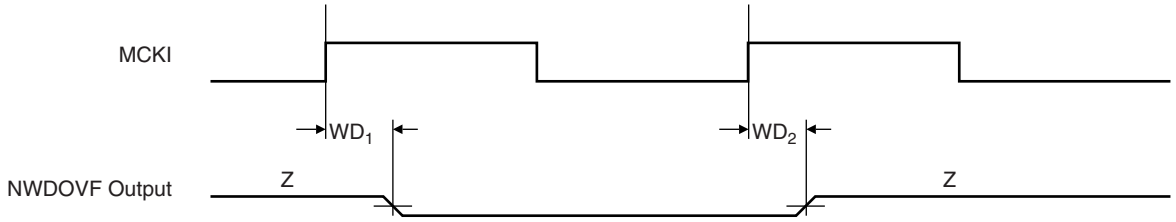


Watchdog Timer Signals

Table 14. Watchdog Timer Outputs

Symbol	Parameter	Minimum		Maximum		Units
		25 MHz	33 MHz	25 MHz	33 MHz	
WD_1	MCKI Rising to NWDOVF Rising	3	3	13	9	ns
WD_2	MCKI Rising to NWDOVF Falling	4	4	14	10	

Figure 7. Watchdog Signals Relative to MCKI



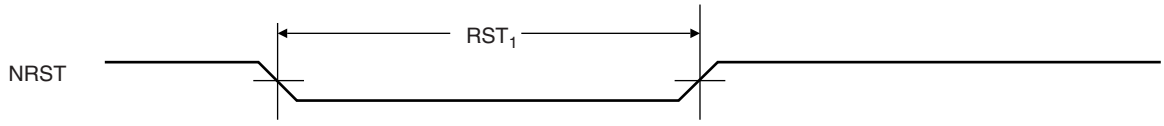
Reset Signals

A minimum pulse width is necessary, as shown in Table 15 and as represented in Figure 8.

Table 15. Reset Minimum Pulse Width

Symbol	Parameter	Minimum Pulse Width	Units
RST_1	NRST Minimum Pulse Width	$10(t_{CP})$	ns

Figure 8. Reset Signal



Only the NRST rising edge is synchronized with MCKI. The falling edge is asynchronous.

Advanced Interrupt Controller Signals

Inputs have to meet the minimum pulse width and mimimum input period shown in Table 16 and Table 17 and represented in Figure 9.

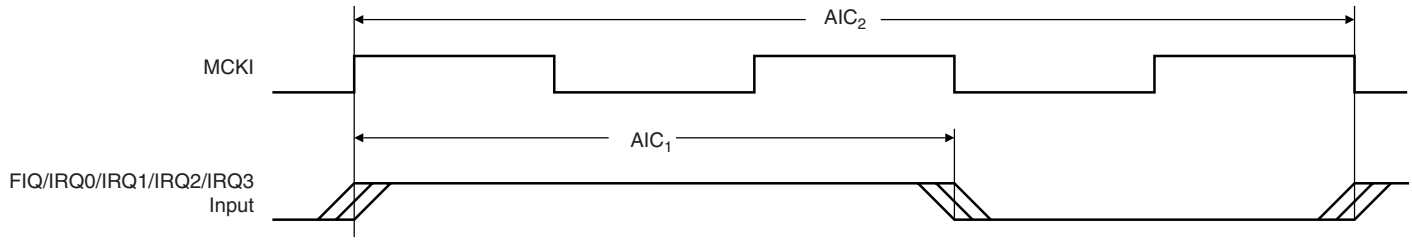
Table 16. AIC Input Minimum Pulse Width

Symbol	Parameter	Minimum Pulse Width	Units
AIC_1	FIQ/IRQ0/IRQ1/IRQ2/IRQ3 Minimum Pulse Width	$3(t_{CP}/2)$	ns

Table 17. AIC Input Minimum Period

Symbol	Parameter	Minimum Input Period	Units
AIC_2	AIC Minimum Input Period	$5(t_{CP}/2)$	ns

Figure 9. AIC Signals



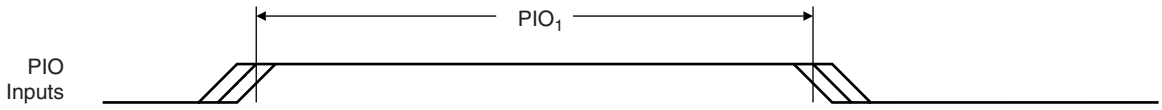
Parallel I/O Signals

The inputs have to meet the minimum pulse width shown in Table 18 and represented in Figure 10.

Table 18. PIO Input Minimum Pulse Width

Symbol	Parameter	Minimum Pulse Width	Units
PIO_1	PIO Input Minimum Pulse Width	$3(t_{CP}/2)$	ns

Figure 10. PIO Signal

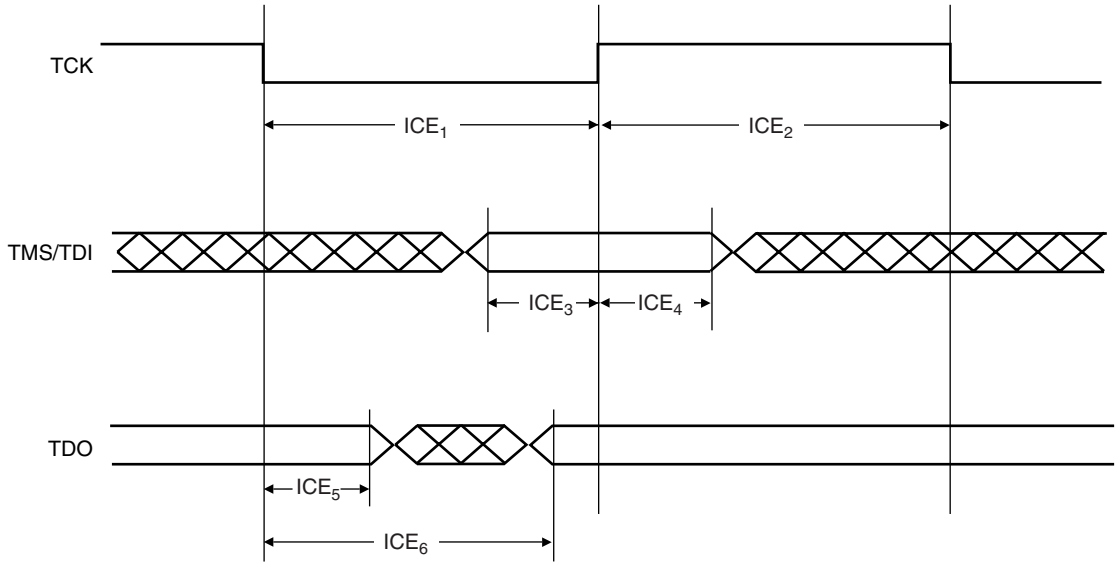


ICE Interface Signals

Table 19. ICE Interface Timing Specifications

Symbol	Parameter	Minimum		Maximum		Units
		25 MHz	33 MHz	25 MHz	33 MHz	
ICE_1	TCK Low Period	TBD	TBD			ns
ICE_2	TCK High Period	TBD	TBD			
ICE_3	TDI, TMS Setup to TCK			TBD	TBD	
ICE_4	TDI, TMS Hold from TCK	TBD	TBD			
ICE_5	TDO Hold Time	TBD	TBD			
ICE_6	TCK to TDO Valid	TBD	TBD	TBD	TBD	

Figure 11. ICE Interface Signal



Package Outline TQFP 100

100-lead Thin (1.4 mm) Quad Flat Pack

Table 20. Common Dimensions (mm)

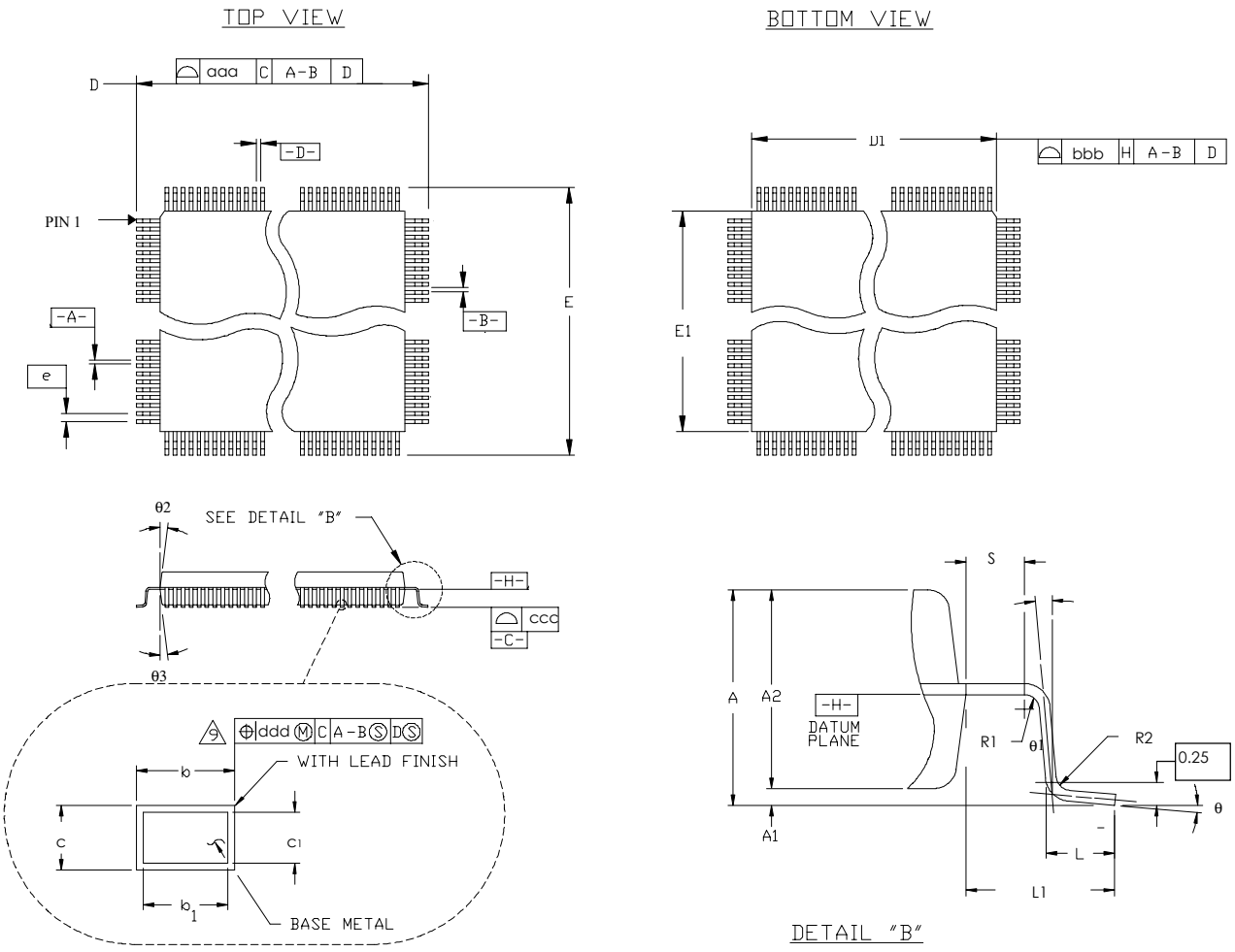
Symbol	Min	Nom	Max
c	0.09		0.2
c1	0.09		0.16
L	0.45	0.6	0.75
L1		1.00 REF	
R2	0.08		0.2
R1	0.08		
S	0.2		
q	0°	3.5°	7°
θ1	0°		
θ2	11°	12°	13°
θ3	11°	12°	13°
A			1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
Tolerances of form and position			
aaa		0.2	
bbb		0.2	

Table 21. Lead Count Dimensions

Pin Count	D/E BSC	D1/E1 BSC	b			b1			e BSC	ccc	ddd
			Min	Nom	Max	Min	Nom	Max			
100	16.0	14.0	0.17	0.22	0.27	0.17	0.2	0.23	0.50	0.10	0.06

Thermal resistance of package: 40°C/W.

Figure 12. 100-lead TQFP Package Drawing



Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
25	2.7V to 3.6V	AT91M40400-25AI	TQFP 100	Industrial (-40°C to 85°C)
33	2.7V to 3.6V	AT91M40400-33AC		Commercial (0°C to 70°C)

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