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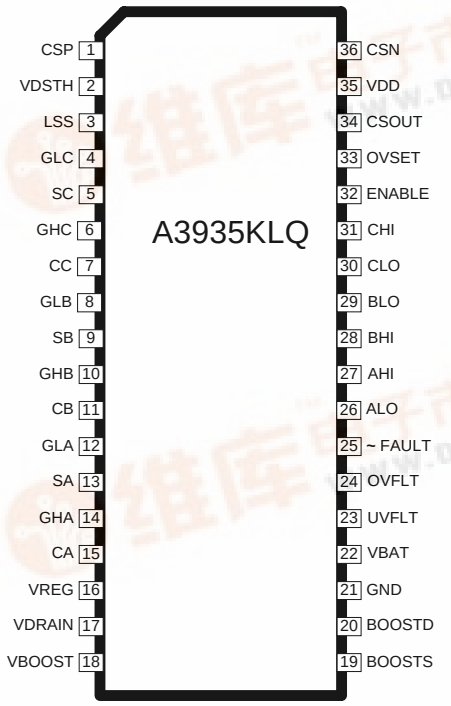
ADVANCED DATA SHEET –- 8/29/02

AUTOMOTIVE POWER-MOSFET CONTROLLER



[44-pin, PLCC pkg. ED also available]

ABSOLUTE MAXIMUM RATINGS

Load Supply Voltages, VBAT, VDRAIN, VBOOST, BOOSTD ..... **40 V**

GHA/GHB/GHC, V_{GHX} ..... ***-4 to 55 V***

SA/SB/SC, V_{SX} ..... ***-4 to 40 V***

GLA/GLB/GLC, V_{GLX} ..... ***-4 to 16 V***

CSP,CSN, LSS ..... ***-4 to 6.5 V***

CA/CB/CC, V_{CX} ..... **-0.6 to 55 V**

Logic Supply Voltage, V_{DD} ..... **- 0.3 V to 6.5 V**

Logic Input/Outputs and OVSET, BOOSTS, CSOUT, VDSTH ..... **-0.3 V to 6.5 V**

Package Thermal Impedances (T_A = +25°C)

ED pkg: Θ_{JA} (JEDEC Hi-K PCB) ..... ***23°C/W***

LQ pkg: Θ_{JA} (JEDEC Hi-K PCB) ..... ***44 °C/W***

Operating Ambient Temperature Range, T_A ..... **-40 °C to +135 °C**

Operating Junction Temperature Range, T_J ..... **-40 °C to +150 °C**

Storage Temperature Range, T_S ..... **-55 °C to +150 °C**

The A3935 is designed specifically for automotive applications that require high-power motors. The A3935 provides six high-current gate drive outputs capable of driving a wide range of power n-channel MOSFETs.

A requirement of automotive systems is steady operation over a varying battery input range. The A3935 integrates a pulse frequency modulated boost converter to create a constant supply voltage for driving the external MOSFETs. Bootstrap capacitors are utilized to provide the above battery supply voltage required for n-channel MOSFETs.

Direct control of each gate output is possible via six TTL-compatible inputs. A differential amplifier is integrated to allow accurate measurement of the current in the three-phase bridge.

A diagnostic output can be continuously monitored to protect the driver from short-to-battery, short-to-supply, bridge-open, and battery under/overvoltage conditions. Additional protection features include dead-time, VDD undervoltage, and thermal shutdown.

FEATURES

- Drives Wide Range of N-Channel MOSFETs in 3-Phase Bridges
- PFM Boost Converter for Use With Low-Voltage Battery Supplies
- Internal LDO Regulator for Gate-Driver Supply
- Bootstrap Circuits for High-Side Gate Drivers
- Current Monitor Output
- Adjustable Battery Overvoltage Detection.
- Diagnostic Outputs
- Motor Lead Short-to-Battery, Short-to-Ground, and Bridge-Open Protection
- Undervoltage Protection
- -40°C to 150°C, T_J Operation
- Thermal Shutdown

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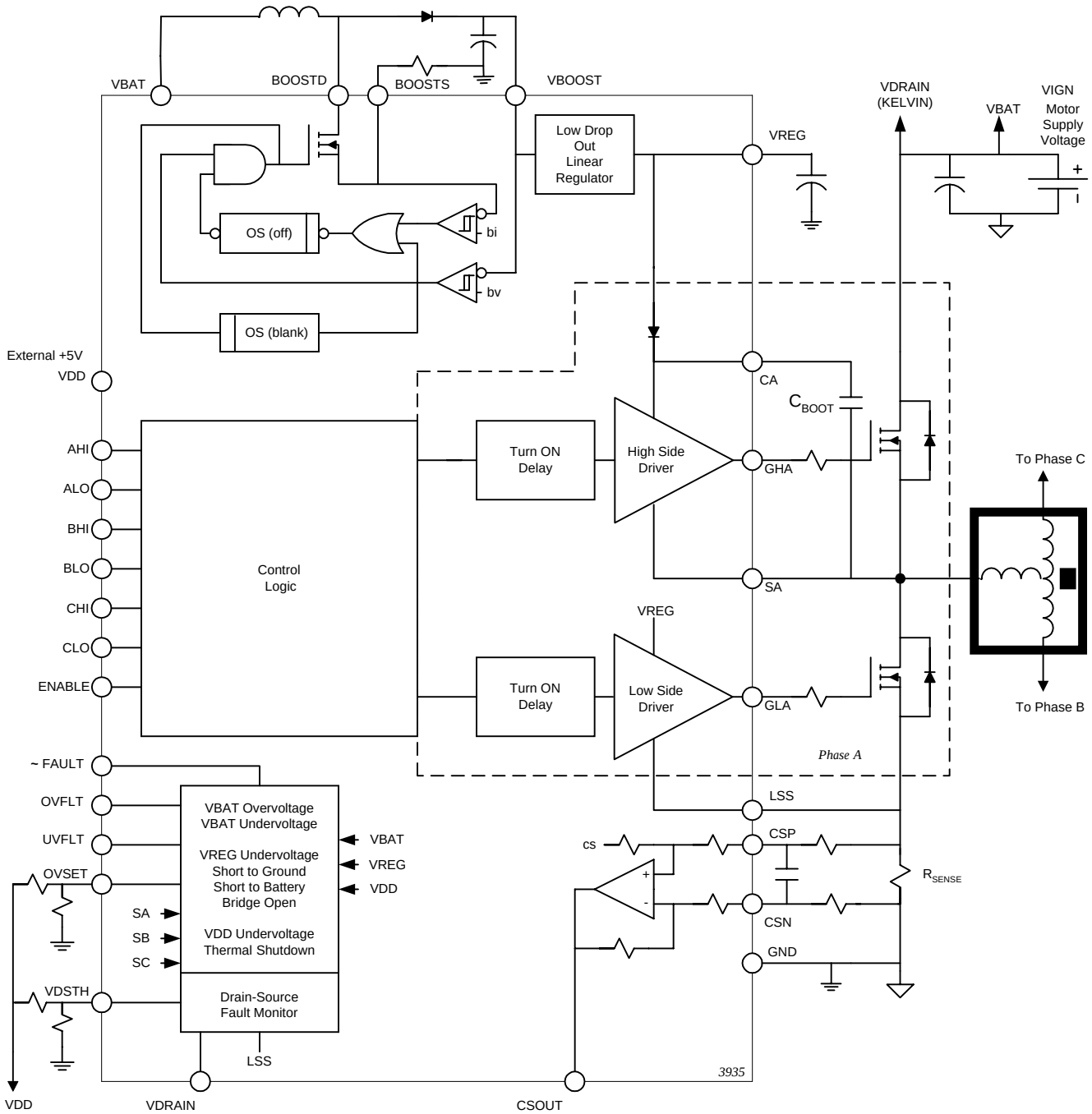
Functional Block Diagram (1 of 3 outputs shown)



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Terminal Descriptions

AHI/BHI/CHI. Direct control of high-side gate outputs GHA/GHB/GHC. Logic “1” drives the gate “on”. Logic ”0” pulls the gate down, turning off the external power MOSFET. Internally pulled down when terminal is open.

ALO/BLO/CLO. Direct control of low-side gate outputs GLA/GLB/GLC. Logic “1” drives the gate “on”. Logic ”0” pulls the gate down, turning off the external power MOSFET**.** Internally pulled down when terminal is open.

BOOSTD. Boost converter switch drain connection**.**

BOOSTS. Boost converter switch source connection

CA/CB/CC. High-side connection for bootstrap capacitor, positive supply for high-side gate drive. The bootstrap capacitor is charged to VREG when the output Sx terminal is Low. When the output swings High, the voltage on this pin rises with the output to provide the boosted gate voltage needed for n-channel power MOSFETs.

CSN. Input for current-sense, differential amplifier, inverting, negative side. Kelvin connection for ground side of current-sense resistor.

CSOUT. Amplifier output voltage proportional to current sensed across an external low-value resistor placed in the ground-side of the power MOSFET bridge.

CSP. Input for current-sense differential amplifier, non-inverting, positive side. Connected to positive side of sense resistor.

ENABLE. Logic “0” disables the gate control signals and switches off all the gate drivers “low” causing a “Coast”. Can be used in conjunction with the gate inputs to PWM the load current. Internally pulled down when terminal is open.

FAULT\. Diagnostic logic output signal indicates that one or more fault conditions has occurred, when “Low”.

GHA/GHB/GHC. High-side gate drive outputs for n-ch MOSFET drivers. External series gate resistors can control slew rate seen at the power driver gate; thereby, controlling the di/dt and dv/dt of Sx outputs.

GLA/GLB/GLC. Low-side gate drive outputs for external, n-channel MOSFET drivers. External series gate resistors can control slew rate

GND. Ground or negative side of VDD and VBAT supplies.

LSS. Low-side gate driver returns. Connects to the common sources in the low-side of the power MOSFET bridge.

OVFLT. Logic “1” means that the VBAT exceeded the VBAT overvoltage trip point set by OVSET level. It will recover after a hysteresis below that maximum value. Has a Hi-Z state.

OVSET. A positive, dc level that controls the VBAT Overvoltage trip point. Usually, provided from precision resistor divider network between VDD and GND, but can be held grounded for a preset value. When terminal is open sets unspecified but high overvoltage trip point.

SA/SB/SC. Directly connected to the motor terminals, these pins sense the voltages switched across the load and are connected to the negative side of the bootstrap capacitors. Also, are the negative supply connection for the floating, high-side drivers.

UVFLT. Logic “1” means that VBAT is below its minimum value and will recover after a hysteresis above that minimum value. Has a Hi-Z state. [If UVFLT and OVFLT are both in Hi-Z state; then, at least, a Thermal shutdown or VDD Undervoltage has occurred.]

VBAT. Battery voltage, positive input and is usually connected to the motor voltage supply.

VBOOST. Boost converter output, nominally 16 V, is also input to regulator for VREG. Has internal boost current and boost voltage control loops. In high-voltage systems is approximately one diode drop below VBAT.

VDD. Logic supply, positive side.

VDRAIN. Kelvin connection for drain-to-source voltage monitor and is connected to high-side drains of MOSFET bridge. High Z when pin is open and registers as a short-to-ground fault on all motor phases.

VDSTH. A positive, dc level that sets the drain-to-source monitor threshold voltage. Internally pulled down when terminal is open.

VREG. High-side, gate-driver supply, nominally, 13.5 V. Has low-voltage dropout (LDO) feature.

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ELECTRICAL CHARACTERISTICS (unless noted; -40°C < T_j < 150°C, 7V < V_{BAT} < 16 V, 4.75V < V_{DD} < 5.25V, ENABLE = 22.5 kHz, 50% Duty cycle, two phases active. (*) or Typ. for design guide, only. Neg. current flows out of designated pin.)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Power Supply						
V_{DD} Supply Current	I_{DD}	All logic inputs = 0 V.			7	mA
V_{BAT} Supply Current	I_{BAT}	All logic inputs = 0 V.			3	mA
Battery Voltage Operating Range	V_{BAT}	See Absolute Maximum Ratings.	7		40	V
Bootstrap Diode Forward Voltage	V_{DBOOT}	I_{DBOOT} = 10 mA	0.8		2	V
		I_{DBOOT} = 100 mA	1.5		2.3	V
Bootstrap Diode Resistance	r_{DBOOT}	r_D(100 mA)=[V_D (150) -V_D (50]/100	2.5		7.5	Ω
Bootstrap Diode Current Limit	I_{LIM}	3 V < [V_{REG} – V_{CX}] < 12 V	-150		-900	mA
Bootstrap Quiescent Current	I_{CX}	V_{CX} = 40V, GHx = ON	10		30	uA
Bootstrap Refresh Time *	$t_{REFRESH}$	V_{SX} = LOW to guarantee ΔV=+0.5 V refresh of 0.47 uF Boot Cap at Vcx –Vsx = +10 V.			2.0	us
VREG Output Voltage [1]	V_{REG}	VBAT=7 V to 40 V, Vboost from Boost Reg.	12.7		14	V
VREG Dropout Voltage [2]	*V_{REGDO}*	*V_{REGDO} = Vboost – Vreg, Ireg = 40 mA*	-	*0.9*	-	*V*
Gate Drive Avg. Supply Current *	I_{REG}	No external dc load at Vreg. Creg=10 uF.			40	mA
VREG Input Bias Current	$I_{REGBIAS}$	Current into VBOOST, ENABLE = 0.			4	mA
Boost Supply						
V_{BOOST} Output Voltage Limit	$V_{BOOSTLIM}$	VBAT = 7 V	14.9		16.3	V
V_{BOOST} Output Volt. Limit Hysteresis	V_{HYST}		35		180	mV
Boost Switch ON	$r_{DS(on)}$	I_{BOOSTD} ≤ 300 mA.		1.4	3.3	Ω
Max. Boost Switch Current	I_{BOOST_SW}				300	mA
Boost Current Limit Threshold Volt.	V_{BI}	Increasing V_{BOOSTS}	0.45		0.55	V
OFF Time	t_{OFF}		3		8	uS
Blanking Time	t_{BLANK}		100		220	nS

Footnotes: 1) For Vboostlim < Vboost ≤ 40 V power dissipation in the Vreg LDO increases. Observe Tj < 150°C limit.

2) With Vboost decreasing Dropout Voltage measured at VREG = VREGref – 200 mV where VREGref = VREG at Vboost= 16 V.

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Control Logic						
Logic Input Voltages	V_{IN} (1)	Minimum high level input for logical “one”.	2.0	–	–	V
	V_{IN} (0)	Maximum low level input for logical “zero”.	–	–	.8	V
Logic Input Currents	I_{IN} (1)	$V_{IN} = V_{DD}$	–		500	µA
	I_{IN} (0)	V_{IN} = 0.8 V	50			µA
Input Hysteresis	Vhys		100		200	mV
Logic Output HIGH Voltage	Voh	Ioh = - 800 uA	VDD -.8			V
Logic Output LOW Voltage	Vol	Iol = 1.6 mA			.4	V
Gate Drives, GHx, GLx (internal SOURCE or upper switch stages)						
Output HIGH Voltage	V_{DSL}(HI)	GHx: I_{xU} = -10 mA, Vsx=0	V_{REG} – 2.26		V_{REG}	V
		GLx: I_{xU} = -10 mA, Vlss=0	V_{REG} – 0.26		V_{REG}	V
Source Current (pulsed)	I_{xU}	V_{SDU} = 10 V, Tj = 25 °C		800		mA
		V_{SDU} = 10 V, Tj = 135 °C	400			mA
Source ON Resistance	r_{SDU}(on)	I_{xU} = -150 mA, Tj = 25 °C	4		10	Ω
		I_{xU} = -150 mA, Tj = 135 °C	7		15	Ω
Gate Drives, GHx, GLx (internal SINK or lower switch stages)						
Sink Current (pulsed)	I_{xL}	V_{DSL} = 10 V, Tj = 25 °C		850		mA
		V_{DSL} = 10 V, Tj = 135 °C	550			mA
Sink ON Resistance	r_{DSL}(on)	I_{xL} = +150 mA, Tj = 25 °C	1.8		6.0	Ω
		I_{xL} = +150 mA, Tj = 135 °C	3.0		7.5	Ω
Gate Drives, GHx, GLx (General)						
Propagation Delay, *Logic only*	t_{PROP}	Logic input to *unloaded* GHx, GLx			150	nS
Prop Delay Differences	t_{PROP}	Grouped by edge, phase-to-phase.			50	nS
Dead Time (Shoot-through Prevention)	t_{DEAD}	Between GHx, GLx transitions of same phase	75		180	nS

Notes: For $\mathbf{GH_X}$: $V_{SDU} = V_{CX} - V_{GHX}$. For $\mathbf{GL_X}$: $V_{SDU} = V_{REG} - V_{GLX}$.

$V_{DSL} = V_{GHX} - V_{SX}$. $V_{DSL} = V_{GLX} - V_{LSS}$.

$V_{DSL}(HI) = V_{CX} - V_{SDU} - V_{SX}$. $V_{DSL}(HI) = V_{REG} - V_{SDU} - V_{LSS}$.

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Sense Amplifier						
Input Bias Current	I_{BIAS}	CSP=CSN=0 V.	-360		-180	uA
Input Offset Current	I_{OS}	CSP=CSN=0 V.	-35		35	uA
Input Impedance *	R_{IN}	CSP with respect to gnd.		80		kΩ
		CSN with respect to gnd.		4		kΩ
Diff. Input Operating Voltage *	V_{ID}	V_{ID} = CSP – CSN. -1.3V < CSP,N < 4V.			200	mV
Output Offset Voltage	V_{OSOUT}	CSP=CSN=0V	77	250	450	mV
Output Offset Voltage Drift *	V_{OSOUT}	CSP=CSN=0V		100		uV/°C
Input Common Mode Oper. Range *	V_{CM}	CSP = CSN	-1.5		4	V
Voltage Gain	A_V	V_{ID} = 40 mV to 200 mV	18.6	19.2	19.8	V/V
Low Output Voltage Error	Verr	Vid = 0 to 40 mV, Vout = 19.2*Vid + Vos + Verr	-25		+25	mV
DC Common Mode Gain	A_{CM}	CSP = CSN = +200 mV			-28	dB
Output Impedance *	R_{OUT}	V_{CSOUT} = 2.0 V		8		Ω
Output Dynamic Range	V_{CSOUT}	I_{CSOUT} = -100 uA at top rail, 100 uA at bottom rail.	0.075		V_{DD} - .25	V
Output Current, Sink	I_{SINK}	V_{CSOUT} = 2.5 V	20			mA
Output Current, Source	I_{SOURCE}	V_{CSOUT} = 2.5 V	-1			mA
VDD Supply Ripple Gain	PSRG	CSP=CSN=GND. Freq = 0 to 1 MHz			-20	dB
VREG Supply Ripple Gain	PSRG	CSP=CSN=GND. Freq = 0 to 300 kHz			-45	dB
Small Signal 3-dB Bandwidth (*)	B	10 mv input		1.6		MHz
AC Common-Mode Gain	A_{cm}	Vcm = 250 mV/pp, Freq = 0 to 800 kHz			-26	dB
| Output Slew Rate |	SR	200 mV step input. Meas. 10/90 % points.	10			V/us

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Fault Logic						
VDD Under-voltage	V_{UVDD}	Decreasing V_{DD}	3.8		4.3	V
VDD Under-voltage Hysteresis	V_{HYSDD}	$V_{UVDD\_RECOVERY} = V_{UVDD} + V_{HYSDD}$	100		300	mV
OVSET Operating Voltage Range *	V_{OVSET}		0		V_{DD}	V
OVSET Calibrated Voltage Range	V_{OVSET}		0		2.5	V
OVSET Input Current Range	I_{OVSET}		-1		+1	uA
VBAT Over-voltage Range	V_{OVBAT}	0 V < V_{OVSET} < 2.5	19.4		40	V
VBAT Over-voltage	V_{OVBAT}	Increasing V_{BAT} , V_{OVSET} = 0 v	19.4	22.4	25.4	V
VBAT Over-voltage Hysteresis	$V_{HYSOVBAT}$	Percent of V_{OVBAT} value set by V_{OVSET}	9		15	%
VBAT Over-voltage Gain Constant *	K_{OVBAT}	$V_{OVBAT} = (K_{OVBAT} * V_{OVSET}) + V_{OVBAT}[0]$		12		V/V
VBAT Under-voltage	V_{UVBAT}	Decreasing V_{BAT}	5	5.25	5.5	V
VBAT Under-voltage Hysteresis	$V_{HYSUVBAT}$	Percent of V_{UVBAT}	8		12	%
VREG Under-voltage	V_{UVREG}	Decreasing VREG	9.9		11.1	V
VDSTH Input Range *	V_{DSTH}		0.5		3	V
VDSTH Input Current	I_{DSTH}	VDSTH $\geq$ 0.8 V	40		100	uA
Short-to-Ground Threshold	V_{STG}	With a High-side driver “on”, as V_{SX} decreases, $V_{DRAIN} - V_{SX} > V_{STG}$ causes a fault.	V_{DSTH} -0..3		V_{DSTH} + 0.2	V
Short-to-Battery Threshold	V_{STB}	With a Low-side driver “on”, as V_{SX} increases, $V_{SX} - V_{LSS} > V_{STB}$ causes a fault.	V_{DSTH} -0.3		V_{DSTH} + 0.2	V
V_{DRAIN} /Open Bridge Operating Range	V_{DRAIN}	7 V < VBAT < 40 V	-0.3		V_{BAT}+ 2	V
V_{DRAIN} /Open Bridge Leakage Curr.	I (V_{DRAIN})	7 V < VBAT < 40 V.	0		1.0	mA
V_{DRAIN} /Open Bridge Threshold Volt.	V_{BDGOTH}	If $V_{DRAIN} < V_{BDGOTH}$ then a Bridge fault occurs.	1		3	V
Thermal Shutdown Temp. *	T_J		160	170	180	°C
Thermal Shutdown Hysteresis *	ΔT_J		7	10	13	°C

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Functional Description

Motor Lead Protection. A fault detection circuit monitors the voltage across the drain to source of the external MOSFETs. A fault is asserted "Low" on the output pin, FAULT\, if the voltage across the drain-to-source of any MOSFET that is instructed to turn on is greater than the voltage applied to the V_{DSTH} input terminal. When a high-side switch is turned on, the voltage from pin V_{DRAIN} to the appropriate motor phase output, V_{SX}, is examined. If the motor lead is shorted to ground before the high side is turned on, the measured voltage will exceed the threshold and the FAULT\ pin will be go "Low". Similarly, when a low-side MOSFET is turned on, the differential voltage between the motor phase (drain) and the LSS pin (source) is monitored. The V_{DSTH} voltage is set by a resistor divider to V_{DD}.

Pin V_{DRAIN} is intended to be a Kelvin connection for the high-side, drain-source monitor circuit. Voltage drops across the power bus are eliminated by connecting a private PCB trace from the V_{DRAIN} pin to the drain of the MOSFET bridge. This allows improved accuracy in setting the V_{DSTH} threshold voltage. The low-side, drain-source monitor uses the LSS pin, rather than V_{DRAIN} pin, in comparing against the V_{DSTH} voltage.

The A3935 merely reports these motor faults.

Fault Outputs. Transient faults on any of the fault outputs are to be expected during switching and will not disable the gate drive outputs. External circuitry or controller logic must determine if the faults represent a hazardous condition.

FAULT\. The FAULT\ terminal will go active "Low" when any of the following conditions occur:

- V_{BAT} Overvoltage
- V_{BAT} Undervoltage
- V_{REG} Undervoltage
- Motor Lead Short-to-Ground
- Motor Lead Short-to-Supply (or Battery).
- Bridge (or V_{DRAIN}) Open
- V_{DD} Undervoltage
- Thermal Shutdown

OVFLT. Asserts "High" when a V_{BAT} Overvoltage fault occurs and resets after a recovery hysteresis. It has a Hi-Z state when a thermal shutdown or V_{DD} undervoltage occurs. The voltage at the OVSET pin, V_{OVSET}, controls the V_{BAT} overvoltage set point V_{OVBAT}, i.e.,

$$V_{OVBAT} = (K_{OVBAT} * V_{OVSET}) + V_{OVBAT}[0],$$

where K_{OVBAT} is the gain and $V_{OVBAT}[0]$ is the value of V_{OVBAT} when V_{OVSET} is zero. For valid formula, all variables must be in range and below maximum operating spec.

UVFLT. Asserts "High" when a V_{BAT} undervoltage fault occurs and resets after a recovery hysteresis. It has a Hi-Z state when a thermal shutdown or V_{DD} undervoltage occurs. OVFLT and UVFLT are mutually exclusive by definition.

Current Sensing. A current sense amplifier is provided to allow system monitoring of the load current. The differential amplifier inputs are intended to be Kelvin connected across a low-value sense resistor or current shunt. The output voltage is represented by:

$$V_{CSOUT} = (I_{LOAD} * A_V * R_{SENSE}) + V_{OS}$$

Where V_{OS} is output voltage calibrated at zero load current and A_V = diff amp gain of about 19.

Shutdown. If a fault occurs because of excessive junction temperature or undervoltage on V_{DD} or V_{BAT}, all gate driver outputs are driven "Low" until the fault condition is removed. In addition, the boost supply switch and the VREG are turned "off" until those undervoltages and junction temperatures recover.

Boost Supply. The V_{BOOST} voltage is controlled by an inner current-control loop, and by an outer voltage-feedback loop. The current-control loop turns "off" the boost switch for 5 us whenever the voltage across the boost current-sense resistor exceeds 500 mV. A diode reverse-recovery current flows through the sense resistor whenever the boost switch turns "on" that could turn it "off", again, if not for the "blanking time" circuit. Adjustment of this external sense resistor determines the maximum current in the inductor. Whenever V_{BOOST} exceeds the predefined threshold, nominally 16 V, the boost switch is inhibited.

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Input Logic.

Enable	(x)LO	(x)HI	GL(x)	GH(x)	Mode of Operation
0	X	X	0	0	All gate-drive outputs Low
1	0	0	0	0	All gate drive outputs Low
1	0	1	0	1	High Side On
1	1	0	1	0	Low Side On
1	1	1	0	0	XOR feature prevents shoot-through.

Fault Responses.

FAULT MODE	ENABLE	FAULT\	OVFLT	UVFLT	BOOST REG.	VREG REG.	GH_X	GL_X
No Fault	X	1	0	0	ON	ON	-	-
Short-to-Battery	1*	0	0	0	ON	ON	-	-
Short-to-Ground	1*	0	0	0	ON	ON	-	-
V_{REG} Undervoltage	X	0	0	0	ON	ON	-	-
V_{DD} Undervoltage or Thermal Shutdown !	X	0	Z	Z	OFF	OFF	0	0
Bridge (V_{DRAIN}) Fault	1*	0	0	0	ON	ON	-	-
V_{BAT} Overvoltage	X	0	1	0	OFF*	ON	-	-
V_{BAT} Undervoltage !	X	0	0	1	O FF	OFF	0	0

Notes: OFF* = Off, only because $V_{BOOST} \sim V_{BAT}$ is above the voltage threshold of the regulator's voltage control loop.
x = "little x "indicates A, B, or C phase.
X = "Capital X " indicates a "don't care".
- = Depends on (x)LO, (x)HI inputs and ENABLE.
Z = Tri-stated output.
1* = Short-to-Battery can only be detected when the corresponding $GL_X = 1$. Similarly, Short-to-Ground can only be detected when the corresponding $GH_X = 1$. Bridge Fault appears as a Short-to-Ground Fault on all motor phases. These faults are not detected when ENABLE = 0
! = These Faults are not only reported but action is taken by the internal logic to protect the 3935 and the system.

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Terminal List

LQ pin #	Pin Name	Pin Description	*ED pin #*
1	CSP	Current-sense input, positive-side	*31*
2	VDSTH	DC Input, Drain-to-Source Monitor Threshold Voltage	*32*
3	LSS	Low-Side, Gate Drive Source returns	*33*
4	GLC	Low-Side C Gate Drive Output	*36*
5	SC	Motor Phase C Input	*37*
6	GHC	High-Side C Gate Drive Output	*38*
7	CC	Bootstrap C Cap	*39*
8	GLB	Low-Side B Gate Drive Output	*40*
9	SB	Motor Phase B Input	*41*
10	GHB	High-Side B Gate Drive Output	*42*
11	CB	Bootstrap B Cap	*43*
12	GLA	Low-Side A Gate Drive Output	*44*
13	SA	Motor Phase A Input	*3*
14	GHA	High-Side A Gate Drive Output	*4*
15	CA	Bootstrap A Cap	*5*
16	VREG	Gate Drive Supply, Positive	*6*
17	VDRAIN	Kelvin Connection to MOSFET High-Side Drain	*7*
18	VBOOST	Boost Supply Output	*8*
19	BOOSTS	Boost Switch, Source	*9*
20	BOOSTD	Boost Switch, Drain	*10*
21	GND	Ground, DC Supply Returns, Negative	*12*
22	VBAT	Battery Supply Connection, Positive	*13*
23	UVFLT	VBAT Undervoltage Fault	*14*
24	OVFLT	VBAT Overvoltage Fault	*15*
25	FAULT\	Fault Output, Primary	*16*
26	ALO	Gate Control Signal, A, Low-Side	*17*
27	AHI	Gate Control Signal, A, High-Side	*18*
28	BHI	Gate Control Signal, B, High-Side	*19*
29	BLO	Gate Control Signal, B, Low-Side	*20*
30	CLO	Gate Control Signal, C, Low-Side	*21*
31	CHI	Gate Control Signal, C, High-Side	*24*
32	ENABLE	Gate Output Enable	*25*
33	OVSET	DC Input, Overvoltage Threshold Setting for VBAT	*26*
-	*TP*	*Test Point for manufacturing test use, only.*	*27*
34	CSOUT	Current-Sense Amplifier Output	*28*
35	VDD	Logic Supply, Positive	*29*
36	CSN	Current-Sense Input, Negative-Side	*30*
-	*GND*	*GROUND, DC Supply Returns, Negative. Heat Path, Die Attach, Connected to Chip GND at Terminal 12.*	*1,2,11,12,22, 23,34,35*