CONEXANT™

CX72300

Spur-Free, 2.1 GHz Dual Fractional-N Frequency Synthesizer

Conexant's CX72300 direct digital modulation fractional-N frequency synthesizer provides ultra-fine frequency resolution, fast switching speed, and low phase-noise performance. This synthesizer is a key building block for high-performance radio system designs that require low power and fine step size.

The ultra-fine step size of less than 100 Hz allows this synthesizer to be used in very narrowband wireless applications. With proper temperature sensing or through control channels, the synthesizer's fine step size can compensate for crystal oscillator or Intermediate Frequency (IF) filter drift. As a result, crystal oscillators or crystals can replace temperature-compensated or ovenized crystal oscillators, reducing parts count and associated component cost. The CX72300's fine step size can also be used for Doppler shift corrections.

The CX72300 has a phase noise floor of –90 dBc/Hz up to 2.1 GHz operation as measured inside the loop bandwidth. This is permitted by the on-chip low noise dividers and low divide ratios provided by the IC's high fractionality.

Reference crystals or oscillators up to 50 MHz can be used with the CX72300. The crystal frequency is divided down by independent programmable divider ratios of 1 to 32 for the main and auxiliary synthesizers. The phase detectors can operate at a maximum speed of 25 MHz, which allows better phase noise due to the lower division value. With a high reference frequency, the loop bandwidths can also be increased. Larger loop bandwidths improve the settling times and reduce in-band phase noise. Therefore, typical switching times of less than 100 µs can be achieved. The CX72300's lower in-band phase noise also permits the use of lower cost Voltage Controlled Oscillators (VCOs) in customer applications.

The CX72300 has a frequency power steering circuit that helps the loop filter to steer the VCO when the frequency is too fast or too slow, further enhancing acquisition time.

The unit operates with a three-wire, high-speed serial interface. A combination of large bandwidth, fine resolution, and the three-wire, high-speed serial interface allows for a direct frequency modulation of the VCO. This supports any continuous phase, constant envelope modulation scheme such as Frequency Modulation, Frequency Shift Keying, Minimum Shift Keying, or Gaussian Minimum Shift Keying (FM, FSK, MSK, GMSK). This capability can eliminate the need for Intermediate and Quadrature Digital-to-Analog Converters (I and Q DACs), quadrature upconverters, and IF filters from the transmitter portion of the radio system.

Distinguishing Features

- Spur-free operation
- 2.1 GHz maximum operating frequency
- 500 MHz maximum auxiliary synthesizer
- Ultra-fine step size, 100 Hz or less
- High internal reference frequency, up to 25 MHz, which enables a larger loop bandwidth Phase Locked Loop (PLL)
- Very fast switching speed (for example, below 100 µs)
- Phase noise to –91 dBc/Hz inside the loop filter bandwidth @ 1800 MHz
- Software programmable power-down modes
- High-speed serial interface, up to 100 Mbps
- Three-wire programming
- Programmable division ratios on reference frequency
- Phase detectors with programmable gain, which provide a programmable loop bandwidth
- Frequency power steering further enhances rapid acquisition time
- On-chip crystal oscillator
- Frequency adjust for temperature compensation
- Direct digital modulation
- 3 V operation
- 5 V output to loop filter
- 28-pin Exposed Pad Thin Shrink Small Outline Package (EP-TSSOP)

Applications

- General purpose RF systems
- 2.5G and 3G wireless infrastructure
- Broadband wireless access
- Low bit rate wireless telemetry
- Instrumentation
- L-band receivers

Ordering Information

Model Number	Package	Ambient Temperature Range	Evaluation Kit Number
CX72300-11	28-Pin Exposed Pad TSSOP	–40 to +85 °C	PH00-D112

Revision History

Revision	Level	Date	Description
P2	Preliminary	May 2001	Revised schematic
P3		October 2001	Revised table.
P4		February 2002	Revisions.

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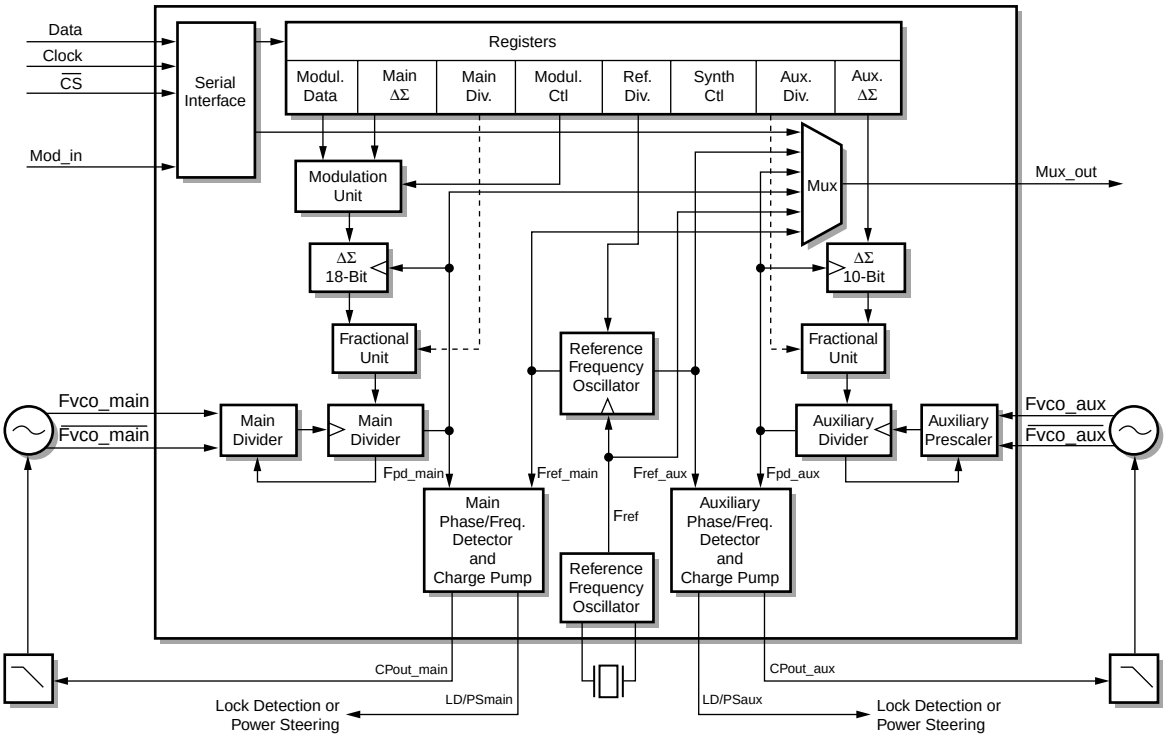
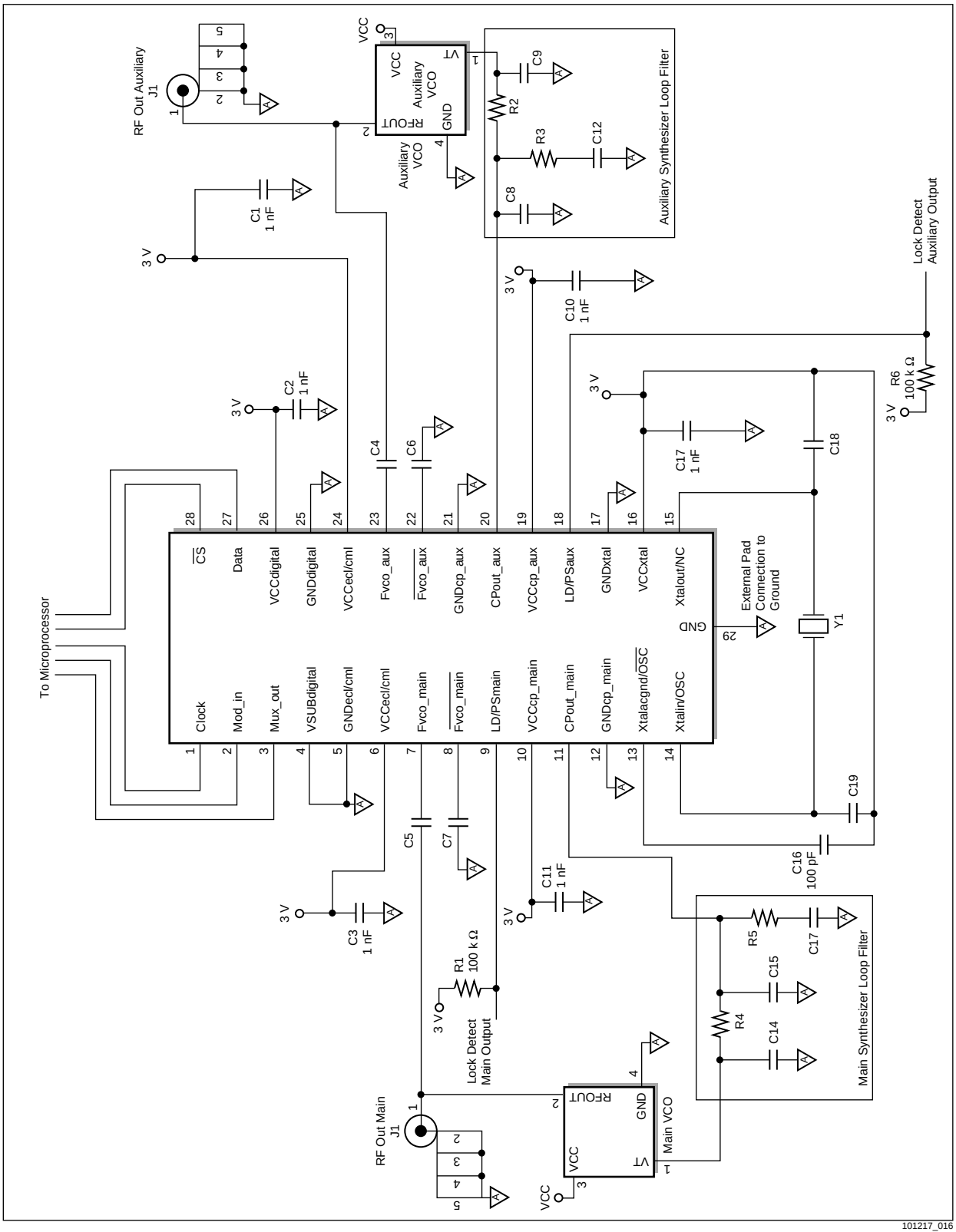
Functional Block Diagram



CX72300 Schematic Diagram



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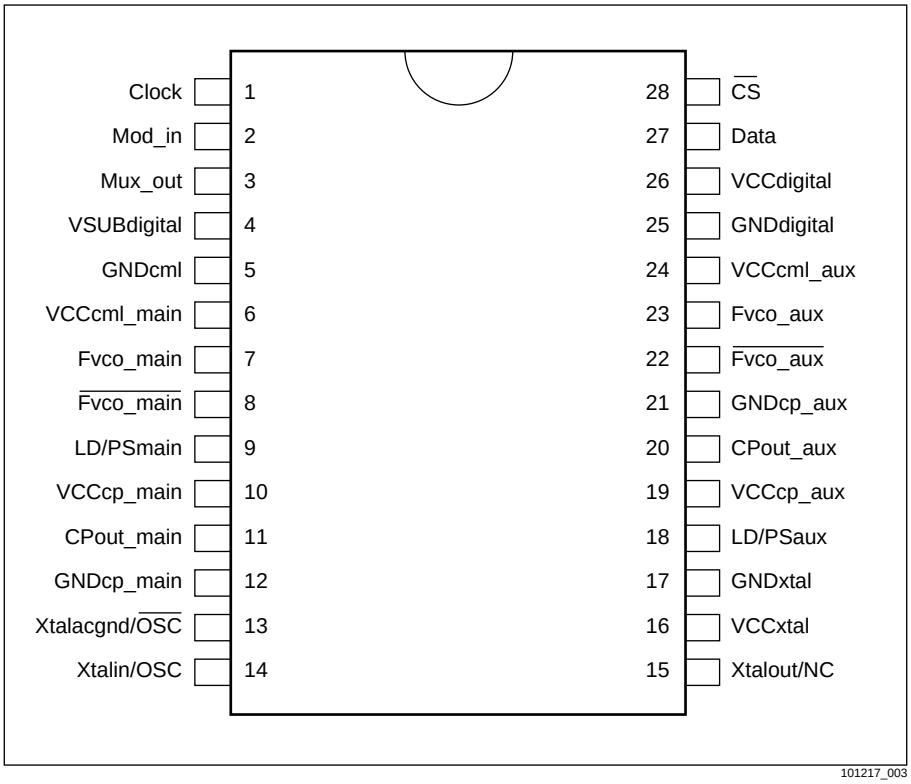
1.0 Technical Description

The CX72300 is supplied as a 28-pin EP-TSSOP. The exposed pad is located on the bottom side of the package and must be connected to ground for proper operation. The exposed pad should be soldered directly to the circuit board. The device pinout is shown in Figure 1-1.

The CX72300 is a fraction-N frequency synthesizer using a Δ–Σ modulation technique. The fractional-N implementation provides low in-band noise by having a low division ratio and fast frequency settling time. In addition, the CX72300 provides arbitrarily fine frequency resolution with a digital word, so that the frequency synthesizer can be used to compensate for crystal frequency drift in the RF transceiver.

Figure 1-1. CX72300 Pinout



1.1 Serial Interface

The serial interface is a versatile three-wire interface, consisting of three pins: serial clock (Clock), serial input (Data), and chip select ($\overline{CS}$). It enables the CX72300 to operate in a system with one or multiple masters and slaves. To perform a loopback test at startup and to check the integrity of the board and processor, the serial data is fed back to the master device (for example, a microcontroller or microprocessor unit) through a programmable multiplexer. This facilitates hardware and software debugging.

For more information, see Section 2.1.

1.2 Registers

There are ten 16-bit registers in the CX72300. For more information, see Chapter 3.0.

1.3 Main and Auxiliary ΔΣ Modulators

The fractionality of the CX72300 is accomplished by the use of a proprietary, configurable 10-bit or 18-bit ΔΣ modulator for the main synthesizer and 10-bit ΔΣ modulator for the auxiliary synthesizer.

1.4 Main and Auxiliary Fractional Units

The CX72300 provides fractionality through the use of main and auxiliary ΔΣ modulators. The output from the main and auxiliary modulators is combined with the main and auxiliary divider ratios through their respective fractional units.

1.5 VCO Prescalers

The VCO prescalers provide low-noise signal conditioning of the VCO signals. They translate from an off-chip single-ended or differential signal to an on-chip differential Current Mode Logic (CML) signal. The CX72300 has independent main and auxiliary VCO prescalers.

1.6 Main and Auxiliary VCO Dividers

The CX72300 provides programmable dividers that control the CML prescalers and supply the required signals to the charge pump phase detectors. Programmable divide ratios ranging from 38 to 537 are possible in fractional-N mode and from 32 to 543 in integer-N mode.

1.7 Reference Frequency Oscillator

The CX72300 has a self-contained, low-noise crystal oscillator. This crystal oscillator is followed by the clock generation circuitry that generates the required clock for the programmable reference frequency dividers.

1.8 Reference Frequency Dividers

The crystal oscillator signal can be divided by a ratio of 1 to 32 to create the reference frequencies for the phase detectors. The CX72300 has both a main and an auxiliary frequency synthesizer, and provides independently configurable dividers of the crystal oscillator frequency for both the main and auxiliary phase detectors. The divide ratios are programmed through the Reference Frequency Dividers Register.

NOTE: The divided crystal oscillator frequencies (which are the internal reference frequencies), F_{ref_main} and F_{ref_aux}, are referred to as the reference frequencies throughout this document.

1.9 Phase Detectors and Charge Pumps

The CX72300 uses a separate charge pump phase detector for each synthesizer which provides a programmable gain, Kd, from 31.25 through 1000 $\mu A/2\pi$ radians in 32 steps programmed via the Control Register.

1.10 Frequency Steering

When programmed for frequency power steering, the CX72300 has a circuit that helps the loop filter steer the VCO, through the LD/PSmain pin. In this configuration, the LD/PSmain pin can provide for more rapid acquisition.

When programmed for lock detection, internal frequency steering is implemented and provides frequency acquisition times comparable to conventional phase/frequency detectors.

1.11 Lock Detection

When programmed for lock detection, the CX72300 provides an active low, pulsing open collector output on the LD/PSmain pin to indicate the out-of-lock condition. When locked, the LD/PSmain pin is three-stated (high impedance).

1.12 Power Down

The CX72300 supports a number of power-down modes through the serial interface. For more information, see Section 3.2.3.

2.0 Operation

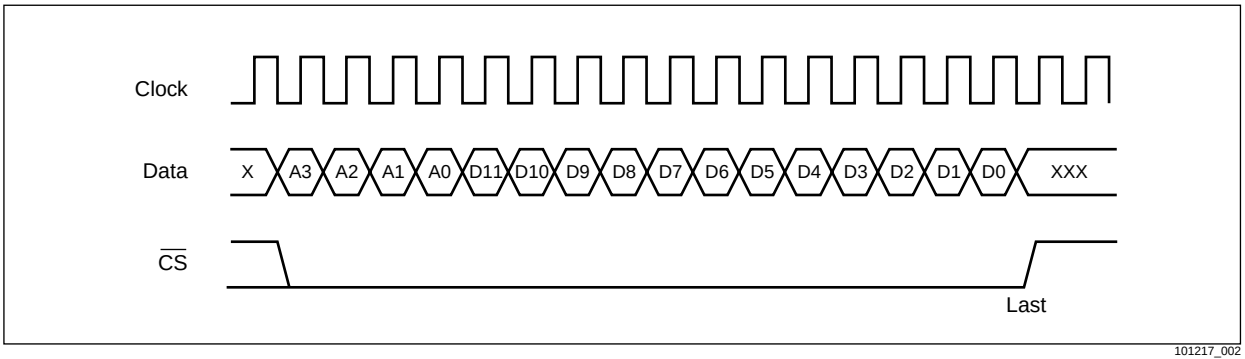
This section describes the operation of the CX72300. The serial interface is described first, followed by information on how to obtain values for the Divide Ratio Registers.

2.1 Serial Interface

The serial interface consists of three pins: Clock, Data, and $\overline{CS}$. The Clock signal controls data transfers that synchronize and sample the information on the two serial data lines (Data and $\overline{CS}$). The data pin bits shift into a temporary register on the rising edge of Clock. The $\overline{CS}$ line allows individual selection of slave devices on the same bus.

Figure 2-1 functionally depicts how a serial transfer takes place.

Figure 2-1. Serial Transfer Timing Diagram



A serial transfer is initiated when a microcontroller or microprocessor forces the $\overline{CS}$ line to a low state. This is immediately followed by an address/data stream sent to the Data pin that coincides with the rising edges of the clock presented on the Clock line. Each rising edge of the Clock signal shifts in one bit of data on the Data line into a shift register. At the same time, one bit of data is shifted out of the Mux_out pin (if the serial bit stream is selected) at each falling edge of Clock. To load any of the synthesizer registers, 16 bits of address or data must be presented to the Data line with the data LSB last while $\overline{CS}$ is low. If $\overline{CS}$ is low for more than 16 clock cycles, only the last address or data bits are used to load the synthesizer registers.

If the $\overline{CS}$ line is brought to a high state before the thirteenth clock edge on Clock, the bit stream is assumed to be modulation data samples. In this case, it is assumed that no address bits are present and that all the bits in the stream should be loaded into the Modulation Data Register.

2.2 Synthesizer Register Programming

Synthesizer register programming equations, described in this section, use the following variables and constants:

$N_{fractional}$	Desired VCO division ratio in fractional-N applications. This is a real number and can be interpreted as the reference frequency (F_{ref}) multiplying factor such that the resulting frequency is equal to the desired VCO frequency.
$N_{integer}$	Desired VCO division ratio in integer-N applications. This number is an integer and can be interpreted as the reference frequency (F_{ref}) multiplying factor such that the resulting frequency is equal to the desired VCO frequency.
N_{reg}	9-bit unsigned input value to the divider ranging from 0 to 511 (integer-N mode) and from 6 to 505 (fractional-N mode)
divider	This constant equals 262144 when the ΔΣ modulator is in 18-bit mode, and 1024 when the ΔΣ modulator is in 10-bit mode
dividend	When in 18-bit mode, this is the 18-bit signed input value to the ΔΣ modulator, ranging from –131072 to +131071 providing 262144 steps, each of $F_{div\_ref} / 2^{18}$ (Hz). When in 10-bit mode, this is the 10-bit signed input value to the ΔΣ modulator, ranging from –512 to +511 providing 1024 steps, each of $F_{div\_ref} / 2^{10}$ Hz.
F_{VCO}	Desired VCO frequency (either F_{vco_main} or F_{vco_aux}).
F_{div_ref}	Divided reference frequency presented to the phase detector (either F_{ref_main} or F_{ref_aux}).

2.2.1 Fractional-N Applications

The desired division ratio for the main and auxiliary synthesizers is given by:

$$N_{fractional} = \frac{F_{VCO}}{F_{div\_ref}}$$

where $N_{fractional}$ must be between 37.5 and 537.5 for the auxiliary synthesizer.

The value to be programmed in the Main or Auxiliary Divider Register is given by:

$$N_{reg} = Round(N_{fractional}) - 32$$

NOTE: The Round function rounds the number to the nearest integer.

When in fractional mode, allowed values for N_{reg} are from 6 to 505 inclusive. The value to be programmed in the Main or Auxiliary Dividend Register is given by:

$$dividend = Round[divider \times (N_{fractional} - N_{reg} - 32)]$$

where the divider is either 1024 in 10-bit mode or 262144 in 18-bit mode. Therefore, the dividend is a signed binary value either 10 or 18 bits long.

NOTE: Because of the high fractionality of the CX72300, there is no practical need for any integer relationship between the reference frequency and the channel spacing or desired VCO frequencies.

2.2.1.1 Fractional-N Example

Case 1: To achieve a desired Fvco_main frequency of 902.4530 MHz using a crystal frequency of 40 MHz with operation of the synthesizer in 18-bit mode. Since the maximum internal reference frequency (F_{div_ref}) is 25 MHz, the crystal frequency is divided by 2 to obtain a F_{div_ref} of 20 MHz. Therefore:

$$N_{fractional} = \frac{F_{vco\_main}}{F_{div\_ref}}$$

$$= \frac{902.4530}{20}$$

$$= 45.12265$$

The value to be programmed in the Main Divider Register is:

$$Nreg = Round[N_{fractional}] - 32$$

$$= Round[45.12265] - 32$$

$$= 45 - 32$$

$$= 13 \text{ (decimal)}$$

$$= 000001101 \text{ (binary)}$$

With the modulator in 18-bit mode, the value to be programmed in the Main Dividend Registers is:

$$dividend = Round[divider \times (N_{fractional} - N_{reg} - 32)]$$

$$= Round[262144 \times (45.12265 - 13 - 32)]$$

$$= Round[262144 \times (0.12265)]$$

$$= Round[32151.9616]$$

$$= 32152 \text{ (decimal)}$$

$$= 0001111101100111000 \text{ (binary)}$$

where 00 0111 1101 is loaded in the MSB of the Main Dividend Register and 1001 1000 is loaded in the LSB of the Main Dividend Register.

Summary:

- Main Divider Register = 0 0000 1101
- Main Dividend LSB Register = 1001 1000
- Main Dividend MSB Register = 00 0111 1101
- The resulting main VCO frequency is 902.453
- Step size is 76.3 Hz

NOTE: The frequency step size for this case is 20 MHz divided by 2^{18} giving 76.3 Hz.

Case 2: Assuming a desired Fvco_main frequency of 917.7786 MHz and a crystal frequency of 19.2 MHz with operation of the synthesizer in 10-bit mode. Since the maximum internal reference frequency (F_{div_ref}) is 25 MHz, the crystal frequency does not require the internal division to be greater than 1, which makes F_{div_ref} = 19.2 MHz. Therefore:

$$N_{fractional} = \frac{F_{vco\_main}}{F_{div\_ref}}$$

$$= \frac{917.7786}{19.2}$$

$$= 47.80097$$

The value to be programmed in the Main Divider Register is:

$$N_{reg} = Round[N_{fractional}] - 32$$

$$= Round[47.80139] - 32$$

$$= 48 - 32$$

$$= 16 \text{ (decimal)}$$

$$= 000010000 \text{ (binary)}$$

With the modulator in 10-bit mode, the value to be programmed in the Main Dividend Registers is:

$$dividend = Round[divider \times (N_{fractional} - N_{reg} - 32)]$$

$$= Round[1024 \times (47.80139 - 16 - 32)]$$

$$= Round[1024 \times (-0.19861)]$$

$$= Round[-203.38133]$$

$$= -203 \text{ (decimal)}$$

$$= 1100110101 \text{ (binary)}$$

where 11 0011 0101 is loaded in the MSB of the Main Dividend Register.

Summary:

- Main Divider Register = 0 0001 0000
- Main Dividend MSB Register = 11 0011 0101
- The resulting VCO frequency is 917.7938 MHz
- Step size is 18.75 kHz

NOTE: The frequency step size for this case is 19.2 MHz divided by 2^{10} giving 18.75 kHz.

2.2.2 Integer-N Applications

The desired division ratio for the main or auxiliary synthesizer is given by:

$$N_{integer} = \frac{F_{vco\_main}}{F_{div\_ref}}$$

where $N_{integer}$ is an integer number from 32 to 543 for both the main and auxiliary synthesizers.
The value to be programmed in the Main or Auxiliary Divider Register is given by:

$$N_{reg} = N_{integer} - 32$$

When in integer mode, allowed values for N_{reg} are from 0 to 511 for both the main and auxiliary synthesizers.

NOTE: As with all integer-N synthesizers, the minimum step size is related to the crystal frequency and reference frequency division ratio.

2.2.2.1 Integer-N Example

Case 1: To achieve a desired Fvco_aux frequency of 400 MHz using a crystal frequency of 16 MHz. Since the minimum divide ratio is 32, the reference frequency must be a maximum of 12.5 MHz. Choosing a reference frequency divide ratio of 2 provides a reference frequency (F_{div_ref}) of 8 MHz. Therefore:

$$N_{integer} = \frac{F_{vco\_aux}}{F_{div\_ref}}$$

$$= \frac{400}{8}$$

$$= 50$$

The value to be programmed in the Auxiliary Divider Register is:

$$N_{reg} = N_{integer} - 32$$

$$= 50 - 32$$

$$= 18 \text{ (decimal)}$$

$$= 000010010 \text{ (binary)}$$

Summary:

- Auxiliary Divider Register = 0 0001 0010

2.2.2.2 Register Loading Order

In applications where the main synthesizer is in 18-bit mode, the Main Dividend MSB Register holds the 10 MSBs of the dividend and the Main Dividend LSB Register holds the 8 LSBs of the dividend. The registers that control the main synthesizer's divide ratio are to be loaded in the following order:

- Main Divider Register
- Main Dividend LSB Register
- Main Dividend MSB Register (at which point the new divide ratio takes effect)

In applications where the main synthesizer is in 10-bit mode, the Main Dividend MSB Register holds the 10 bits of the dividend. The registers that control the main synthesizer's divide ratio are to be loaded in the following order:

- Main Divider Register
- Main Dividend MSB Register (at which point the new divide ratio takes effect)

For the auxiliary synthesizer, the Auxiliary Dividend Register holds the 10 bits of the dividend. The registers that control the auxiliary synthesizer's divide ratio are to be loaded in the following order:

- Auxiliary Divider Register
- Auxiliary Dividend Register (at which point the new divide ratio takes effect)

NOTE: When in integer mode, the new divide ratios take effect as soon as the Main or Auxiliary Divider Register is loaded.

2.3 Direct Digital Modulation

The high fractionality and small step size of the CX72300 allow the user to tune to practically any frequency in the VCO's operating range. This frequency tuning allows direct digital modulation by programming the different desired frequencies at precise instants. Typically, the channel frequency is selected through the Main Divider and Dividend Register and the instantaneous frequency offset from the carrier is entered through the Modulation Data Register.

The Modulation Data Register can be accessed in three ways, which are defined in the following subsections.

2.3.1 Normal Register Write

A normal 16-bit serial interface write occurs when $\overline{CS}$ is 16 clock cycles wide. The corresponding 16-bit modulation data is simultaneously presented to the Data pin. The content of the Modulation Data Register is passed to the modulation unit at the next falling edge of the divided main VCO frequency (F_{pd_main}).

2.3.2 Short $\overline{CS}$ Through Data Pin (No Address Bits Required)

A shortened serial interface write occurs when $\overline{CS}$ is from 2 to 12 clock cycles wide. The corresponding modulation data (2 to 12 bits) is simultaneously presented to the Data pin. The Data pin is the default pin used to enter modulation data directly in the Modulation Data Register with shortened $\overline{CS}$ strobes. This method of data entry eliminates the register address overhead on the serial interface. All serial interface bits are re-synchronized internally at the reference oscillator frequency. The content of the Modulation Data Register is passed to the modulation unit at the next falling edge of the divided main VCO frequency (F_{pd_main}).

2.3.3 Short $\overline{CS}$ Through Mod_in Pin (No Address Bits Required)

A shortened serial interface write occurs when $\overline{CS}$ is from 2 to 12 clock cycles wide. The corresponding modulation data (2 to 12 bits) is simultaneously presented on the Mod_in pin. The Mod_in pin is the alternate pin used to enter modulation data directly into the Modulation Data Register with shortened $\overline{CS}$ strobes. This mode is selected through the Modulation Control Register. This method of data entry also eliminates the register address overhead on the serial interface and allows a different device than the one controlling the channel selection to enter the modulation data (e.g., a microcontroller for channel selection and a digital signal processor for modulation data). All serial interface bits are re-synchronized internally at the reference oscillator frequency and the content of the Modulation Data Register is passed to the modulation unit at the next falling edge of the divided main VCO frequency (F_{pd_main}).

Modulation data samples in the Modulation Data Register can be from 2 to 12 bits long, and enable the user to select how many distinct frequency steps are to be used for the desired modulation scheme.

The user can also control the frequency deviation through the modulation data magnitude offset in the Modulation Control Register. This allows shifting of the modulation data to accomplish a 2^m multiplication of frequency deviation.

The programmable range of –0.5 to +0.5 of the main ΔΣ modulator can be exceeded up to the condition where the sum of the dividend and the modulation data conform to:

$$-0.5625 \leq (N_{mod} + dividend) \leq +0.5625$$

NOTE: When the sum of the dividend and modulation data lie outside this range, the value of $N_{integer}$ must be changed.

For a more detailed description of direct digital modulation functionality, refer to the Conexant document *CX72300/1/2 Direct Digital Modulation Application Note*, document number 101349.

3.0 Registers

This section describes the CX72300 registers. All register writes are programmed address first, followed directly with data. MSBs are entered first. On power-up, all registers are reset to 0x000 except registers at addresses 0x0 and 0x3, which are set to 0x006.

3.1 Register Map

Table 3-1 provides a description for each of the CX72300 device registers.

Table 3-1. CX72300 Register Map

Address (hexadecimal)	Register(1)	Length Bits	Address Bits
0	Main Divider Register	12	4
1	Main Dividend MSB Register	12	4
2	Main Dividend LSB Register	12	4
3	Auxiliary Divider Register	12	4
4	Auxiliary Dividend Register	12	4
5	Reference Frequency Dividers Register	12	4
6	Control Register—phase detector/charge pumps	12	4
7	Control Register—power down/multiplexer output select	12	4
8	Modulation Control Register	12	4
9	Modulation Data Register Modulation Data Register(2)—direct input	12 2 ≤ length ≤ 12	4 0

NOTES:
(1) All registers are write only.
(2) No address bits are required for modulation data. Any serial data between 2 and 12 bits long is considered modulation data.

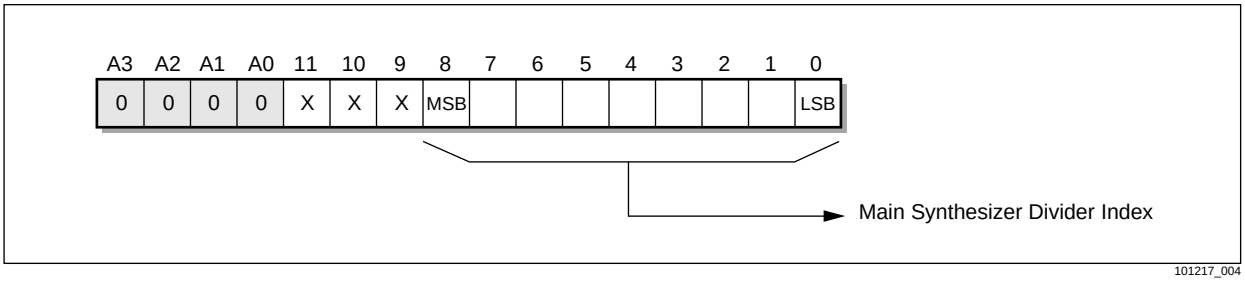
3.1.1 Register Descriptions

For more information on register loading order, see Section 2.2.2.2.

3.2 Synthesizer Registers

3.2.1 Main Synthesizer Registers

Figure 3-1. Main Divider Register (Write Only)



The Main Divider Register contains the integer portion closest to the desired fractional-N (or the integer-N) value minus 32 for the main synthesizer. This register, in conjunction with the Main Dividend Registers (which control the fraction offset from –0.5 to +0.5), allows selection of a precise frequency.

As shown in Figure 3-1, the value to be loaded is:

- Main Synthesizer Divider Index = 9-bit value for the integer portion of the main synthesizer dividers. Valid values for this register are from 6 to 505 (fractional-N) or from 0 to 511 (integer-N).

The Main Dividend MSB and LSB Registers control the fraction part of the desired fractional-N value and allow an offset of –0.5 to +0.5 to the main integer selected through the Main Divider Register.

As shown in Figures 3-2 and 3-3, values to be loaded are:

- Main Synthesizer Dividend (MSBs) = 10-bit value for the MSBs of the 18-bit dividend for the main synthesizer.
- Main Synthesizer Dividend (LSBs) = 8-bit value for the LSBs of the 18-bit dividend for the main synthesizer.

The Main Dividend Register MSB and LSB values are 2's complement format.

NOTE: When in 10-bit mode, the Main Synthesizer Dividend (LSBs) is not required.

For information on programming and loading order for these registers, see Chapter 2.0.

Figure 3-2. Main Dividend MSB Register (Write Only)

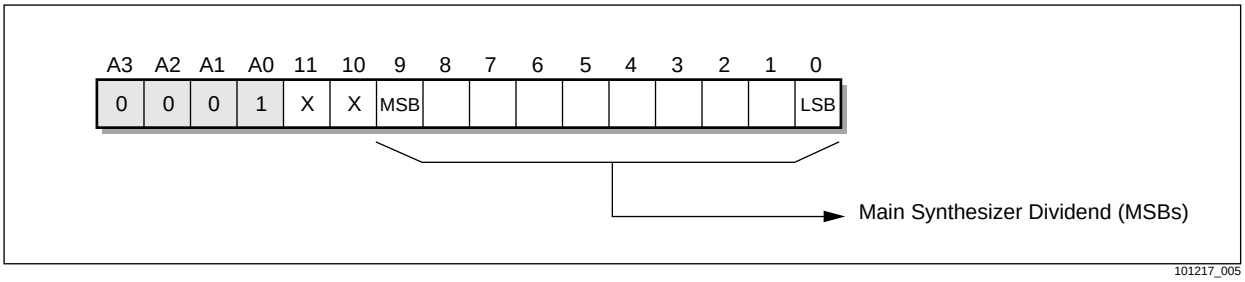
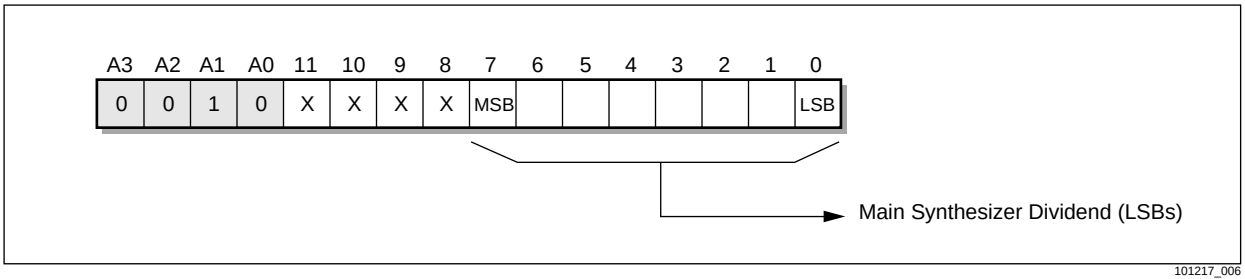


Figure 3-3. Main Dividend LSB Register (Write Only)



3.2.2 Auxiliary Synthesizer Registers

The Auxiliary Divider Register contains the integer portion closest to the desired fractional-N (or integer-N) value minus 32 for the auxiliary synthesizer. This register, in conjunction with the Auxiliary Dividend Register, which controls the fraction offset (from –0.5 to +0.5), allows selection of a precise frequency.

As shown in Figure 3-4, the value to be loaded is:

- Auxiliary Synthesizer Divider Index = 9-bit value for the integer portion of the auxiliary synthesizer dividers. Valid values for this register are from 6 to 505 (fractional-N) or from 0 to 511 (integer-N).

The Auxiliary Dividend Register controls the fraction part of the desired fractional-N value and allows an offset of –0.5 to +0.5 to the auxiliary integer selected through the Auxiliary Divider Register.

As shown in Figure 3-5, the value to be loaded is:

- Auxiliary Synthesizer Dividend = 10-bit value for the dividend for the auxiliary synthesizer.

For information on programming and loading order for these registers, see Chapter 2.0.

Figure 3-4. Auxiliary Divider Register (Write Only)

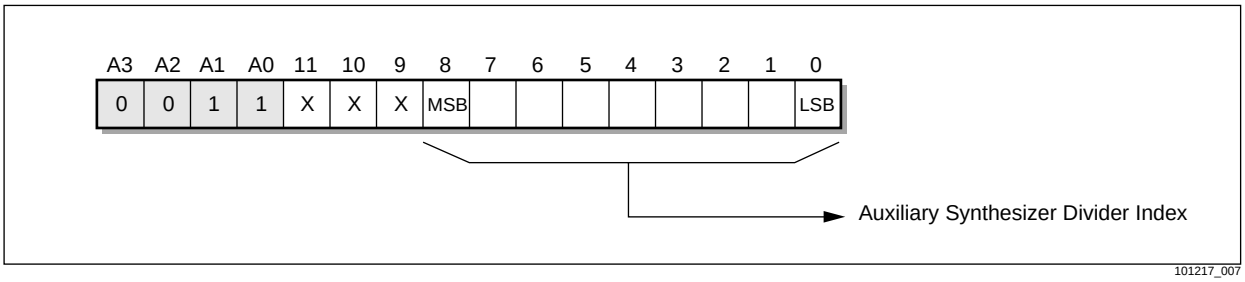
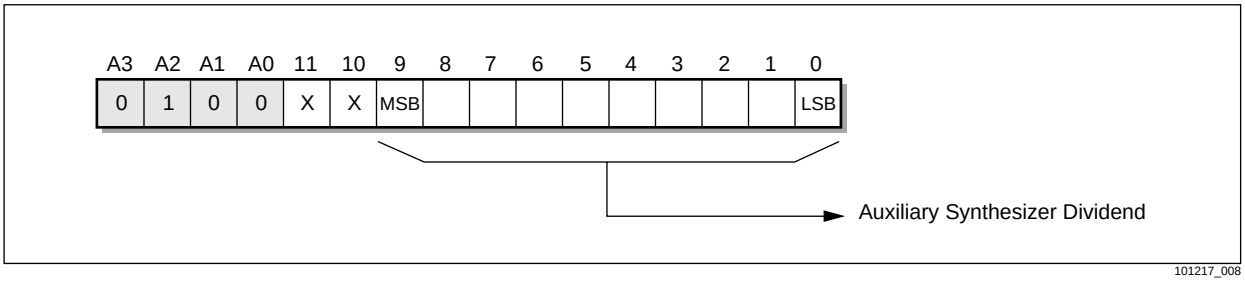
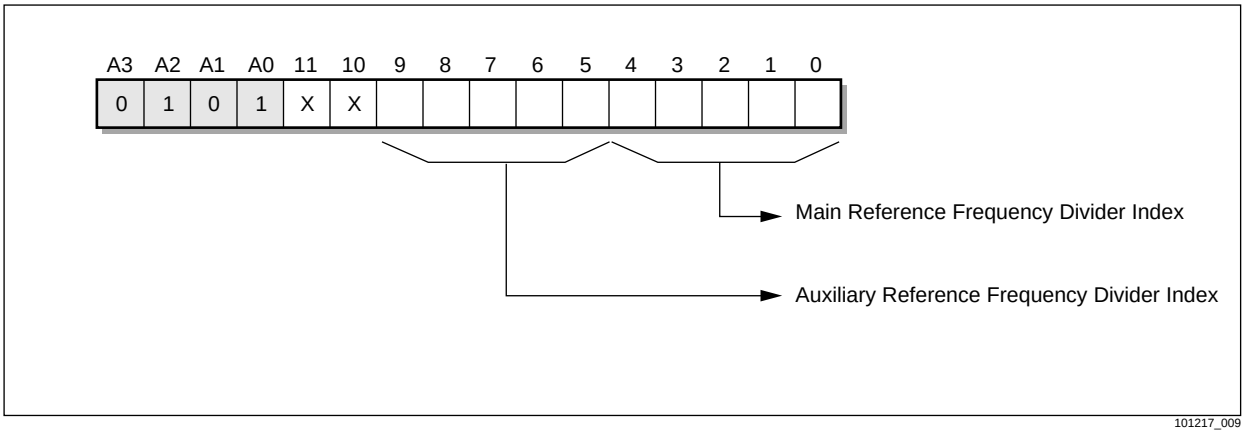


Figure 3-5. Auxiliary Dividend Register (Write Only)



3.2.3 General Synthesizer Registers

Figure 3-6. Reference Frequency Dividers Register (Write Only)



The Reference Frequency Dividers Register configures the dual-programmable reference frequency dividers for the main and auxiliary synthesizers.

The dual-programmable reference frequency dividers provide the reference frequencies to the phase detectors by dividing the crystal oscillator frequency. The lower five bits hold the reference frequency divide index for the main phase detector. The next five bits hold the reference frequency divide index for the auxiliary phase detector. Divide ratios from 1 to 32 are possible for each reference frequency divider.

As shown in Figure 3-6, the values to be loaded are:

- Main Reference Frequency Divider Index = Desired main oscillator frequency division ratio –1. Default value on power-up is 0, signifying that the reference frequency is not divided for the main phase detector. See Table 3-2 for other programming values.
- Auxiliary Reference Frequency Divider Index = Desired auxiliary oscillator frequency division ratio –1. Default value on power-up is 0, signifying that the reference frequency is not divided for the auxiliary phase detector. See Table 3-3 for other programming values.

Table 3-2. Programming the Main Reference Frequency Divider

Decimal	Bit 4 (MSB)	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Reference Divider Ratio
0	0	0	0	0	0	1
1	0	0	0	0	1	2
2	0	0	0	1	0	3
—	—	—	—	—	—	—
—	—	—	—	—	—	—
—	—	—	—	—	—	—
31	1	1	1	1	1	32

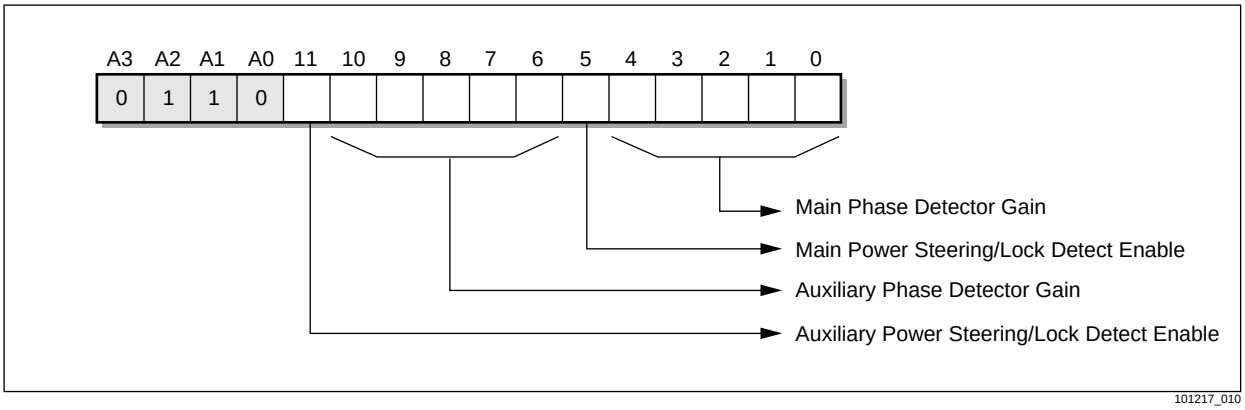
Table 3-3. Programming the Auxiliary Reference Frequency Divider

Decimal	Bit 9 (MSB)	Bit 8	Bit 7	Bit 6	Bit 5 (LSB)	Reference Divider Ratio
0	0	0	0	0	0	1
1	0	0	0	0	1	2
2	0	0	0	1	0	3
—	—	—	—	—	—	—
—	—	—	—	—	—	—
—	—	—	—	—	—	—
31	1	1	1	1	1	32

The Control Register allows control of the gain for both phase detectors and configuration of the LD/PSmain and LD/PSaux pins for frequency power steering or lock detection.
As shown in Figure 3-7, the values to be loaded are:

- Main Phase Detector Gain = 5-bit value for programmable main phase detector gain. Range is from 0 to 31 decimal for 31.25 to 1000 µA/ 2π radian, respectively.
- Main Power Steering Enable = 1-bit value to enable the frequency power steering circuitry of the main phase detector. When this bit is a 0, the LD/PSmain pin is configured to be a lock detect, active low, open collector pin. When this bit is a 1, the LD/PSmain pin is configured to be a frequency power steering pin and can be used to bypass the external main loop filter to provide faster frequency acquisition.
- Auxiliary Phase Detector Gain = 5-bit value for programmable auxiliary phase detector gain. Range is from 0 to 31 decimal for 31.25 to 1000 µA/radian, respectively.
- Auxiliary Power Steering Enable = 1-bit value to enable the frequency power steering circuitry of the auxiliary phase detector. When this bit is a 0, the LD/PSaux pin is configured to be a lock detect, active low, open collector pin. When this bit is a 1, the LD/PSaux is configured to be a frequency power steering pin and may be used to bypass the external auxiliary loop filter to provide faster frequency acquisition.

Figure 3-7. Control Register (Write Only)



The Power Down and Multiplexer Output Register allows control of the power-down modes, internal multiplexer output, and main ΔΣ synthesizer fractionality.

As shown in Figure 3-8, the values to be loaded are:

- Full Power Down = 1-bit value that powers down the CX72300 except for the reference oscillator and the serial interface. When this bit is 0, the CX72300 is powered up. When this bit is 1, the CX72300 is in full power-down mode excluding the Mux_out pin.
- Main Synthesizer Power Down = 1-bit value that powers down the main synthesizer. When this bit is 0, the main synthesizer is powered up. When this bit is 1, the main synthesizer is in power-down mode.
- Main Synthesizer Mode = 1-bit value that powers down the main synthesizer's ΔΣ modulator and fractional unit to operate as an integer-N synthesizer. When this bit is 0, the main synthesizer is in fractional-N mode. When this bit is 1, the main synthesizer is in integer-N mode.
- Main Synthesizer ΔΣ Fractionality = 1-bit value that configures the size of the main ΔΣ modulator. This has a direct effect on power consumption and on the level of fractionality and step size. When this bit is 0, the main ΔΣ modulator is 18-bit with a fractionality of 2^{18} and a step size of $F_{ref\_main}/262144$. When this bit is 1, the main ΔΣ modulator is 10-bit with a fractionality of 2^{10} and a step size of $F_{ref\_main}/1024$.
- Auxiliary Synthesizer Power Down = 1-bit value that powers down the auxiliary synthesizer. When this bit is 0, the auxiliary synthesizer is powered up. When this bit is 1, the auxiliary synthesizer is in power-down mode.
- Auxiliary Synthesizer Mode = 1-bit value that powers down the auxiliary synthesizer's ΔΣ modulator and fractional unit to operate as an integer-N synthesizer. When this bit is 0, the auxiliary synthesizer is in fractional-N mode. When this bit is 1, the auxiliary synthesizer is in integer-N mode.

NOTE: There are no special power-up sequences required for the CX72300.

- Multiplexer Output Selection = 3-bit value that selects which internal signal is output to the Mux_out pin. The following internal signals are available on this pin:
  - Reference Oscillator: F_{ref}
  - Main or auxiliary divided reference (post reference frequency main or auxiliary dividers): F_{ref_main} or F_{ref_aux}
  - Main or auxiliary phase detector frequency (post main and auxiliary frequency dividers): F_{pd_main} or F_{pd_aux}
  - Serial data out for loop-back and test purposes
- Mux_out Pin Three-State Enable = 1-bit value to three-state the Mux_out pin. When this bit is 0, the Mux_out pin is enabled. When this bit is 1, the Mux_out pin is three-stated.

Refer to Table 3-4 for more information.

Figure 3-8. Power Down and Multiplexer Output Register (Write Only)

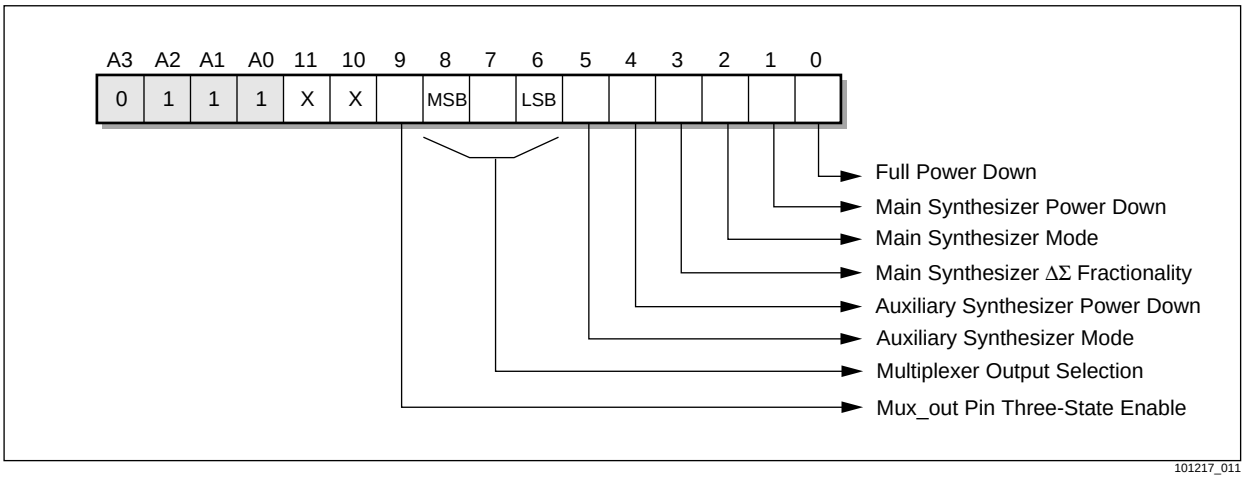


Table 3-4. Multiplexer Output

Multiplexer Output Select bit 8	Multiplexer Output Select bit 7	Multiplexer Output Select bit 6	Multiplexer Output (Mux_out)
0	0	0	Reference Oscillator
0	0	1	Auxiliary Reference Frequency (F_{ref_aux})
0	1	0	Main Reference Frequency (F_{ref_main})
0	1	1	Auxiliary Phase Detector Frequency (F_{pd_aux})
1	0	0	Main Phase Detector Frequency (F_{pd_main})
1	0	1	Serial data out
1	1	0	Serial Interface Register test output

The Modulation Control Register is used to configure the modulation unit of the main synthesizer.

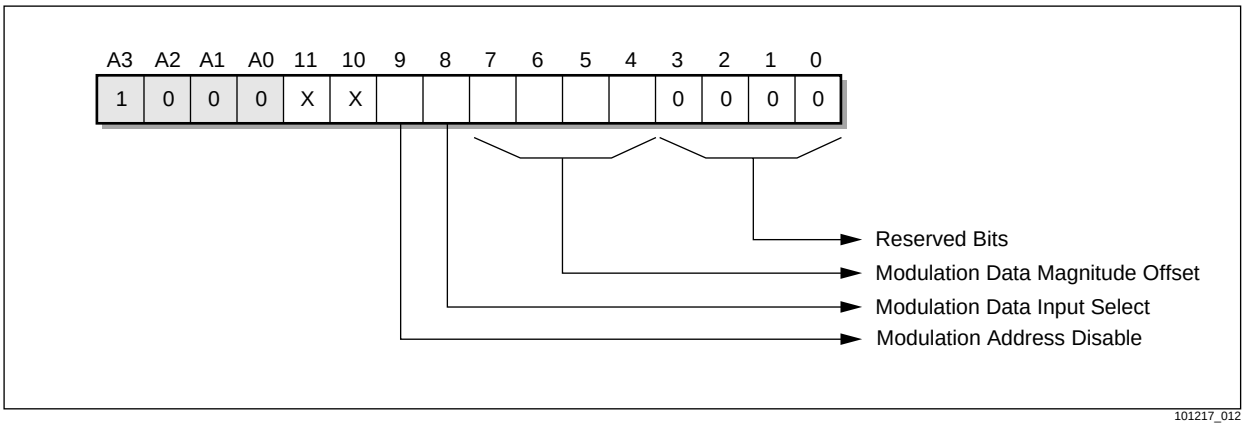
The modulation unit adds or subtracts a frequency offset to the selected center frequency at which the main synthesizer operates. The size of the modulation data sample, controlled by the duration of the $\overline{CS}$ pin, can be from 2 to 12 bits wide, to provide from 4 to 4096 selectable frequency offset steps.

The modulation data magnitude offset selects the magnitude multiplier for the modulation data and can be from 0 to 8.

As shown in Figure 3-9, the values to be loaded are:

- Modulation Data Magnitude Offset = 4-bit value that indicates the magnitude multiplier (m) for the modulation data samples. Valid values range from 0 to 13, effectively providing a 2^m multiplication of the modulation data sample.
- Modulation Data Input Select = 1-bit value that indicates the pin on which modulation data samples are serially input when the $\overline{CS}$ signal is between 2 and 12 bits long. When this bit is 0, modulation data samples are to be presented on the Data pin. When this bit is 1, modulation data samples are to be presented on the Mod_in pin. For more details, refer to Section 2.3.
- Modulation Address Disable = 1-bit value that indicates the presence of the address as modulation data samples are presented on either the Mod_in or Data pins. When this bit is 0, the address is presented with the modulation data samples (i.e., all transfers are 16 bits long). When this bit is 1, no address is presented with the modulation data samples (i.e., all transfers are 2 to 12 bits long). For more details, refer to Section 2.3.

Figure 3-9. Modulation Control Register (Write Only)

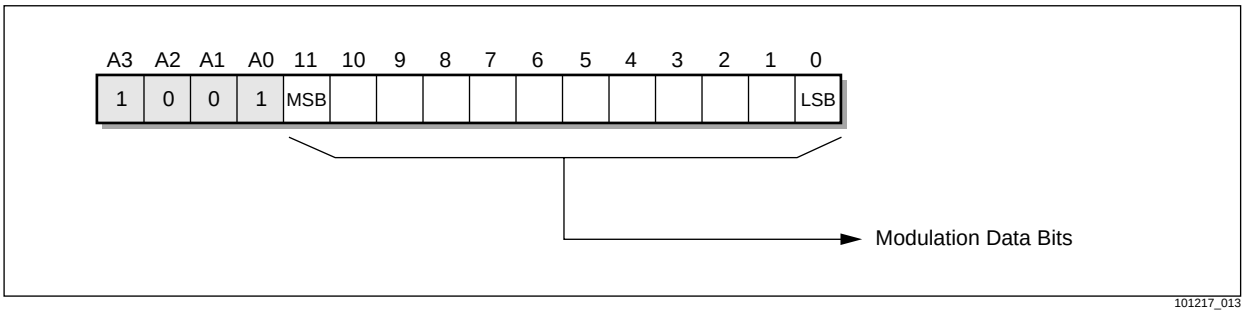


The Modulation Data Register loads the modulation data samples to the modulation unit. This value is transferred to the modulation unit on the falling edge of F_{pd_main} where it is passed to the main ΔΣ modulator at the selected magnitude offset on the next falling edge of F_{pd_main}. Modulation Data Register values are 2's complement format.

As shown in Figure 3-10, the value to be loaded is:

- Modulation Data Bits = Modulation data samples that represent the instantaneous frequency offset to the selected main synthesizer frequency (selected channel) before being affected by the modulation data magnitude offset.

Figure 3-10. Modulation Data Register (Write Only)



4.0 Electrical/Mechanical

4.1 Signal Pin Assignments

Signal pin assignments and functional pin descriptions are specified in Table 4-1.

Table 4-1. CX72300 Pin Description *(1 of 2)*

Pin Label	Pin #	Type	Description
Clock	1	Digital input	Clock signal pin. When $\overline{CS}$ is low, the register address and data is shifted in address bits first on the Data pin on the rising edge of Clock. For more information, see Section 2.1.
Data	27	Digital input	Serial address and data input pin. Address bits are followed by data bits. For more information, see Section 2.1.
$\overline{CS}$	28	Digital input	Active low enable pin. Enables loading of address and data on the Data pin on the rising edge of Clock. When $\overline{CS}$ goes high, data is transferred to the register indicated by the address. Subsequent clock edges are ignored. For more information, see Section 2.1.
Mod_in	2	Digital input	Alternate serial modulation data input pin. Address bits are followed by data bits.
Mux_out	3	Digital output	Internal multiplexer output. Selects from oscillator frequency, main or auxiliary reference frequency, main or auxiliary divided VCO frequency, serial data out or testability signals. This pin can be three-stated from the general synthesizer registers. For more information, see Section 3.2.3.
Xtalacgnd/$\overline{OSC}$	13	Ground/Input	Reference crystal AC ground, or external oscillator complementary input.
Xtalin/OSC	14	Input	Reference crystal input, or external oscillator differential input.
Xtalout/NC	15	Input	Reference crystal output, or no connect.
Fvco_main	7	Input	Main VCO differential input.
$\overline{Fvco\_main}$	8	Input	Main VCO complimentary differential input.
Fvco_aux	23	Input	Auxiliary VCO differential input.
$\overline{Fvco\_aux}$	22	Input	Auxiliary VCO complimentary differential input.
CPout_main	11	Analog output	Main charge pump output. The gain of the main charge pump phase detector can be controlled from the general synthesizer registers.

Table 4-1. CX72300 Pin Description *(2 of 2)*

Pin Label	Pin #	Type	Description
LD/PSmain	9	Analog output	Programmable output pin. Indicates main phase detector out-of-lock as an active low pulsing open collector output (high impedance when lock is detected), or helps the loop filter steer the main VCO. This pin is configured from the general synthesizer registers.
CPout_aux	20	Analog output	Auxiliary charge pump output. The gain of the auxiliary charge pump phase detector can be controlled from the general synthesizer registers.
LD/PSaux	18	Analog output	Programmable output pin. Indicates auxiliary phase detector out-of-lock as an active low pulsing open collector output (high impedance when lock is detected), or helps the loop filter steer the auxiliary VCO. This pin is configured from the general synthesizer registers.
VCCdigital(1)	26	Power and ground	Digital 3 V.
GNDdigital(1)	25	Power and ground	Digital ground.
VCCxtal	16	Power and ground	Crystal oscillator Emitter Coupled Logic (ECL)/Current Mode Logic (CML) 3 V.
GNDxtal	17	Power and ground	Crystal oscillator ground.
VCCcml/main(1) VCCcml_aux(1)	6 24	Power and ground	ECL/CML 3 V. Removing power safely powers down the associated divider chain and charge pump.
GNDecl/cml(1)	5	Power and ground	ECL/CML ground.
VCCcp_main(1) VCCcp_aux(1)	10 19	Power and ground	Main and auxiliary charge pump 3 to 5 V. Removing power safely powers down the associated divider chain and charge pump.
GNDcp_main(1) GNDcp_aux(1)	12 21	Power and ground	Main and auxiliary charge pump ground.
VSUBdigital	4	—	Substrate isolation, connect to ground.

NOTE:
(1) Associated pairs of power and ground pins must be decoupled using 0.1 µF capacitors.

4.2 Specifications and Ratings

Table 4-2. Absolute Maximum Ratings

Parameter	Rating
Maximum analog RF supply voltage	3.6 VDC
Maximum digital supply voltage	3.6 VDC
Maximum charge pump supply voltage	5.25 VDC
Storage temperature	–65 °C to +150 °C
Operating temperature	–40 °C to +85 °C

Table 4-3. Recommended Operating Conditions

Parameter	Rating
Analog RF supplies	+2.7 to +3.3 VDC
Digital supply	+2.7 to +3.3 VDC
Charge pump supplies	+2.7 to +5.0 VDC
Operating temperature (T_A)	–40 °C to +85 °C

Table 4-4. Power Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_{total}	Total power consumption	Charge pump currents of 200 µA Both synthesizers fractional F_{ref_main} = 20 MHz F_{ref_aux} = 1 MHz	—	37.5	—	mW
		Auxiliary synthesizer power-down	—	27	—	—
$I_{CC-PWDN}$	Power-down current	—	—	10	—	µA

Table 4-5. Reference Oscillator

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{osc}	Reference oscillator frequency	—	—	—	50	MHz
V_{osc}	Oscillator sensitivity (as a buffer)	AC coupled, single-ended	0.1	—	2.0	V_{pp}
F_{shift_supply}	Frequency shift versus supply voltage	T = 25°C 2.7 V ≤ V_{xtal} ≤ 3.3 V	—	—	± 0.3	ppm

Table 4-6. VCOs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{vco_main}	Main synthesizer operating frequency	Sinusoidal	100*(1)*	—	2100	MHz
F_{vco_aux}	Auxiliary synthesizer operating frequency		100*(1)*	—	500	
V_{vco}	RF input sensitivity	AC Coupled	50	—	250	mV_{peak}
Z_{vco_in}	RF input impedance	—		94 – j140 @ 1200 MHz	—	Ω
ΔF_{step_main}	Main fractional-N tuning step size	—	$F_{ref\_main} / 2^{18}$ or $F_{ref\_main} / 2^{10}$			Hz
ΔF_{step_aux}	Auxiliary fractional-N tuning step size	—	$F_{ref\_aux} / 2^{10}$			

NOTE:
(1) When operating in fractional mode, minimum synthesizer frequency is 12x Fosc, where Fosc is the frequency at the Xtalin/OSC pin.

Table 4-7. Noise

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_{NF}	Phase noise floor	Measured inside the loop bandwidth using 25 MHz reference frequency.	—	–128 + 20 Log(N)	—	dBc/Hz

Table 4-8. Phase Detectors and Charge Pumps

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
F_{ref_main}	Main phase detector frequency		—	—	25	MHz
F_{ref_aux}	Auxiliary phase detector frequency					
$I_{cp\text{-}source}$	Charge pump output source current	V_{cp} = 0.5 VCC_{cp}	125	—	1000	µA
$I_{cp\text{-}sink}$	Charge pump output sink current		–125	—	–1000	
$I_{cp\text{-}accuracy}$	—	—	—	± 20	—	%
I_{cp} vs. V_{cp}	Charge pump output voltage linearity range	0.5 V ≤ V_{cp}≤ (VCC_{cp} –0.5 V) T = 25°C	Gnd + 400	—	VCC_{cp} – 400	mV
I_{cp} vs. T	Charge pump current versus temperature	V_{cp} = 0.5 VCC_{cp} –40 °C < T < +85 °C	—	—	5	%
I_{cp} vs. V_{cp}	Charge pump current versus voltage	0.5 V ≤ V_{cp}≤ (VCC_{cp} –0.5 V) T = 25 °C	—	—	8	

Table 4-9. Digital Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIH	High level input voltage	—	0.7 $V_{digital}$	—	—	V
VIL	Low level input voltage	—	—	—	0.3 $V_{digital}$	
VOH	High level output voltage	I_{OH} = –2 mA	$V_{digital}$ – 0.2	—	—	
VOL	Low level output voltage	I_{OL} = 2 mA	—	—	Gnd + 0.2	

Table 4-10. Timing—Serial Interface

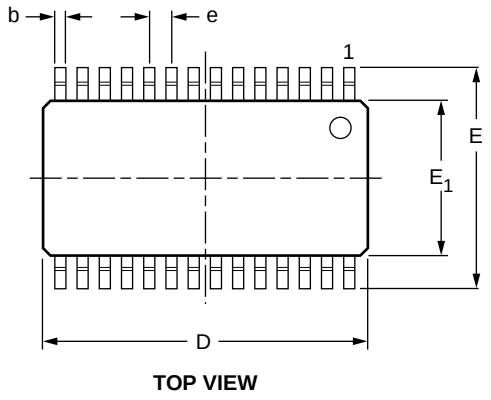
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{clock}	Clock frequency	—	—	—	100	MHz
t_{su}	Data and $\overline{CS}$ set up time to Clock rising	—	3	—	—	ns
t_{hold}	Data and $\overline{CS}$ hold time after Clock rising	—	0	—	—	ns

4.3 Electrostatic Discharge Information

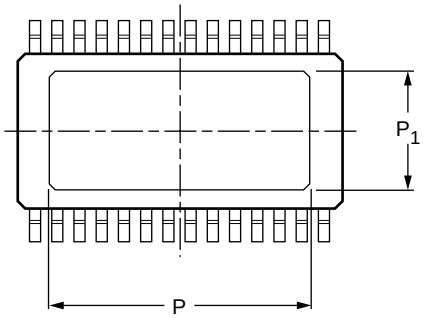
The CX72300 device is an electrostatic sensitive device. Observe precautions when handling.

4.4 Package Information

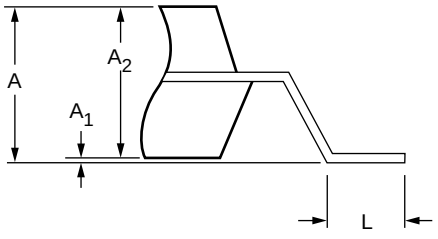
Figure 4-1. 28-Pin EP-TSSOP



TOP VIEW



EXPOSED PAD BOTTOM VIEW



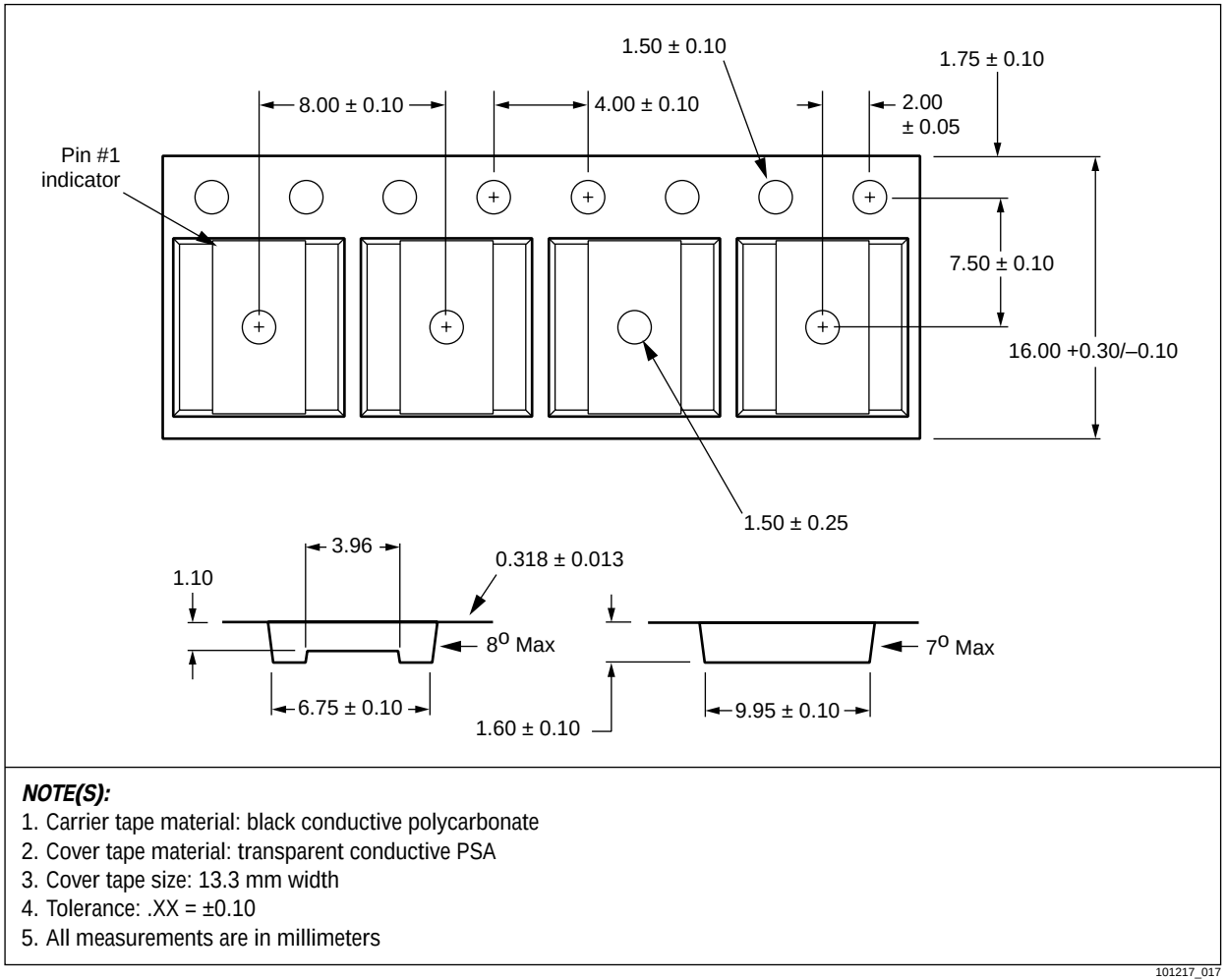
SIDE VIEW DETAIL

Dim.	Millimeters	
	MIN.	MAX.
A		1.10
A_1	0.05	0.15
A_2	0.85	0.95
D	9.70 BSC	
E	6.40 BSC	
E_1	4.30	4.50
L	0.50	0.70
P		3.50
P_1		3.00
e	0.65 BSC	
b	0.19	0.30

101217_014

4.5 Tape and Reel

Figure 4-2. Tape and Reel Drawing



NOTE(S):

1. Carrier tape material: black conductive polycarbonate
2. Cover tape material: transparent conductive PSA
3. Cover tape size: 13.3 mm width
4. Tolerance: .XX = ±0.10
5. All measurements are in millimeters

101217_017

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