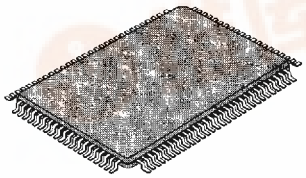
80-CHANNEL SEGMENT DRIVER FOR DOT MATRIX LCD

The KS0063 is a LCD driver LSI which is fabricated by low power CMOS technology. Basically this LSI consists of 40×2 bit bidrectional shift register, 40×2 bit data latch and 40×2 bit LCD driver (refer to Fig 1) This LSI can be used segment driver.

100 QFP



FUNCTION

- Dot matrix LCD driver with 80 channel output.
- Input/Output signal
  - — output: 40 × 2 channel waveform for LCD driving
  - — Input : - Serial display data and control pulse from the controller LSI.
    - Bais voltage (V_1-V_4)

FEATURES

- Display driving bias; static-1/5
- Power supply voltage; +5V ±10%
- Supply voltage for display: 0~-5V(VEE)
- interface

driver (cascade connection)	controller
KS0065, Other KS0063	KS0066

- CMOS Process
- 100QFP and bare chip available

BLOCK DIAGRAM

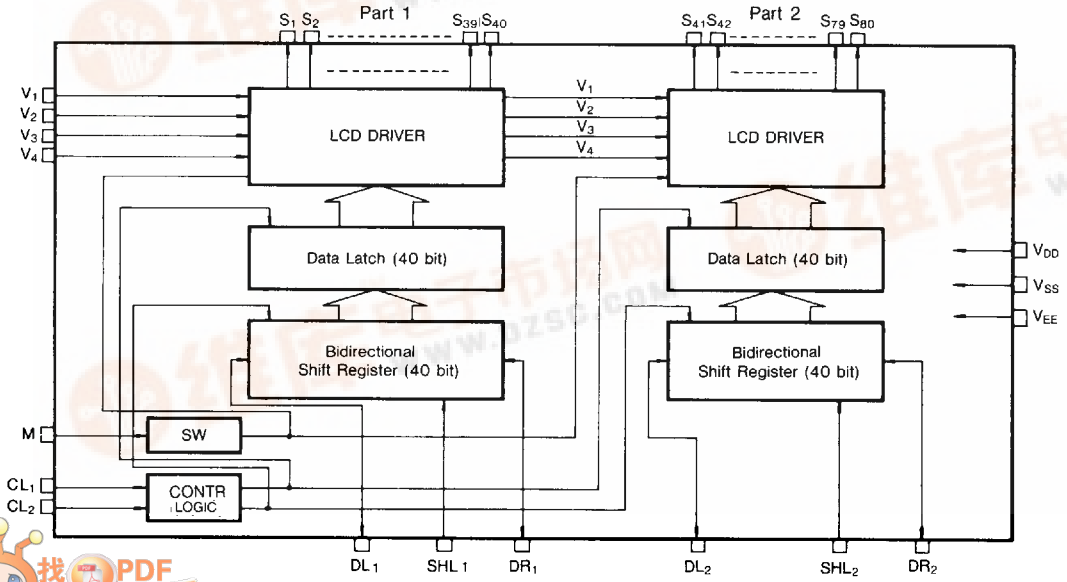


Fig. 1. KS0063 functional block diagram

PIN CONFIGURATION

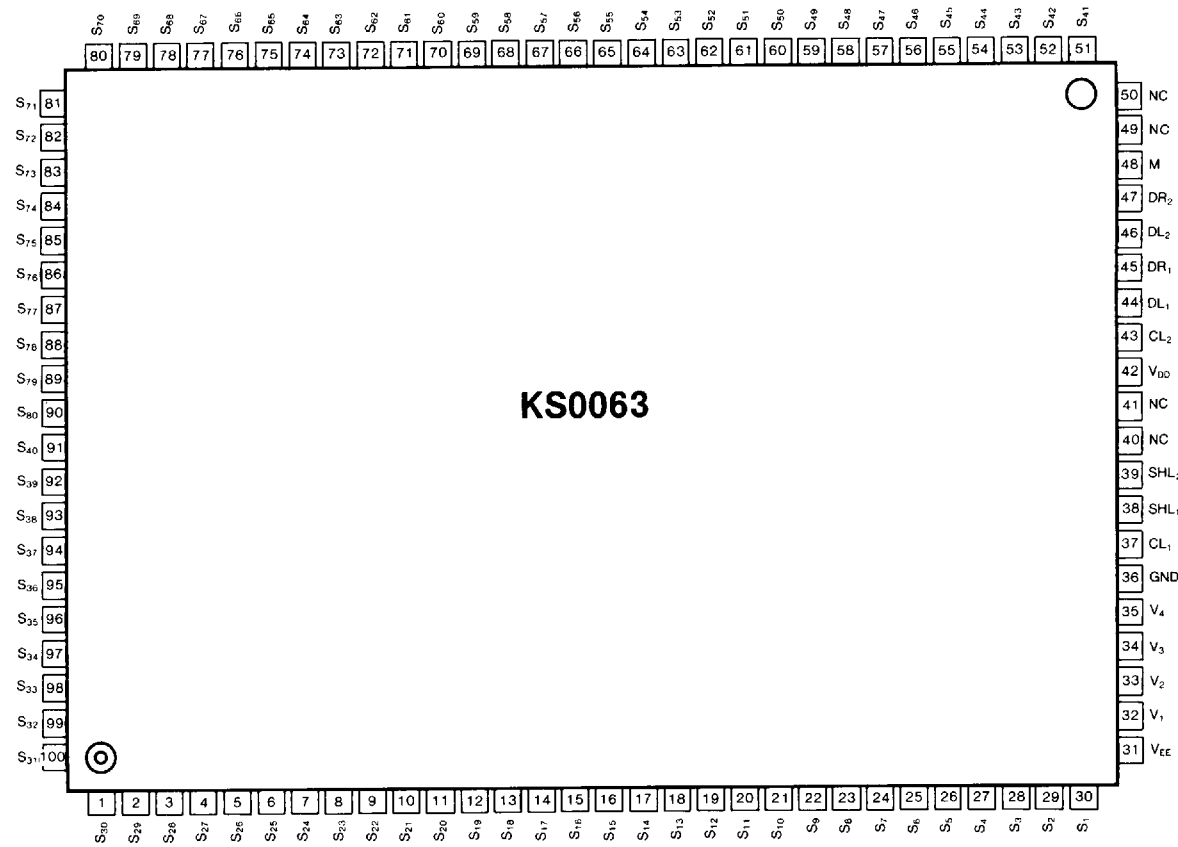


Fig. 2. 100 QFP Top View

PIN DESCRIPTION

<table>
<tr><th>PIN (NO.)</th><th>INPUT OUTPUT</th><th colspan="2">NAME</th><th>DESCRIPTION</th><th>INTERFACE</th></tr>
<tr><td>V_{DD}(42)</td><td rowspan="3"></td><td colspan="2" rowspan="3">Power Supply</td><td>For logical circuit (+5V±10%)</td><td rowspan="3">Power Supply</td></tr>
<tr><td>GND(36)</td><td>0V (GND)</td></tr>
<tr><td>V_{EE}(31)</td><td>For LCD driver circuit (−5V)</td></tr>
<tr><td>V1, V2 (32,33)</td><td>Input</td><td colspan="2" rowspan="2">LCD drive</td><td>Bias voltage level for LCD drive (Select level)</td><td rowspan="2">Power</td></tr>
<tr><td>V3, V4 (34,35)</td><td>Input</td><td>Bias voltage level for LCD drive (Nonselect level)</td></tr>
<tr><td>S1-S40</td><td>Output</td><td rowspan="3">Part 1</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>SHL1(38)</td><td>Input</td><td>Data Interface</td><td>Selection of the shift direction of shift register
<table><tr><th>SHL1</th><th>DL1</th><th>DR1</th></tr><tr><td>V_{DD}</td><td>OUT</td><td>IN</td></tr><tr><td>V_{SS}</td><td>IN</td><td>OUT</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL1, DR1 (44,45)</td><td>Input Output</td><td colspan="2">Data Input/output of shift register (part 1)</td><td>Controller or KS0063</td></tr>
<tr><td>S41-S80</td><td>Output</td><td rowspan="3">Part 2</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>SHL2 (39)</td><td>Input</td><td>Data Interface</td><td>Selection of the shift direction of shift register
<table><tr><th>SHL2</th><th>DL2</th><th>DR2</th></tr><tr><td>V_{DD}</td><td>OUT</td><td>IN</td></tr><tr><td>V_{SS}</td><td>IN</td><td>OUT</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL2, DR2 (46,47)</td><td>Input Output</td><td colspan="2">Data input/output of shift register (part 2)</td><td>Controller or KS0063</td></tr>
<tr><td>M(48)</td><td>Input</td><td colspan="2">Alternated signal for LCD driver output</td><td rowspan="2"></td><td rowspan="2">Controller</td></tr>
<tr><td>CL1, CL2 (37,43)</td><td>Input</td><td colspan="2">Data shift/ latch clock</td><td>CL1: Data latch clock
CL2: Data shift clock</td></tr>
<tr><td>NC (40,41,49,50)</td><td></td><td colspan="2"></td><td>No connection</td><td>NC</td></tr>
</table>

MAXIMUM ABSOLUTE LIMIT (Ta=25°C)

Characteristic	Symbol	Value	Unit
Power supply Voltage	V_{DD}	−0.3∼+7.0	V
Driver Supply Voltage	V_{LCD}	V_{DD}-13.5∼V_{DD}+0.3	V
Input Voltage 1	V_{IN1}	−0.3∼V_{DD}+0.3	V
Input Voltage 2 (V_1-V_4)	V_{IN2}	V_{DD}+0.3∼V_{EE}−0.3	V
Operating Temperature	T_{opr}	−20∼+75	°C
Storage temperature	T_{stg}	−55∼+125	°C

*Voltage greater than above may damage to the circuit
*V_{EE}: connect a protection resistor (220Ω ±5%)

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{DD}=+5V±10% V_{EE}=−5±10% V_{SS}=0V, T_a=25°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Supply current	I_{DD}	f_{CL2}=400kHz	—	1	mA	
	I_{EE}	f_{CL1}=1KHz	—	10	μA	
Input Voltage	V_{IH}	—	0.7V_{DD}	V_{DD}	V	CL1, CL2, DL1 DL2, DR1, DR2 SHL1, SHL2, M,
	V_{IL}		0	0.3V_{DD}		
Input leakage current	I_{IL}	V_{IN}=0∼V_{DD}	−5	5	μA	
Output Voltage	V_{OH}	I_{OH}=−0.4mA	V_{DD}−0.4	—	V	DL1, DL2, DR1, DR2
	V_{OL}	I_{OL}=+0.4mA	—	0.4		
Voltage descending	V_{d1}	I_{ON}=0.1mA for one of S_1-S_{80}	—	1.1		V(V_1-V_4)-S(S_1-S_{80})
	V_{d2}	I_{ON}=0.05mA for each S_1-S_{80}	—	1.5		
Leakage current	I_{V1}	V_{IN}=V_{DD}∼V_{EE} (Output S_1∼S_{80}; floating)	−10	10	μA	V_1-V_4

AC CHARACTERISTICS (V_{DD}=5V±10%, V_{EE}=−5V±10%, V_{SS}=0V, Ta=25°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data shift frequency	f_{CL}	—	—	400	KHz	CL2
Clock High level width	t_{CWH}	—	800	—	ns	CL1, CL2
Clock low level width	t_{CWL}	—	800	—		CL2
Clock set-up time	t_{SL}	from CL2 to CL1	500	—		CL1, CL2
	t_{LS}	from CL1 to CL2	500	—		
Clock rise/fall time	t_{CT}	—	—	200		
Data Set-up time	t_{SU}	—	300	—		DL1, DL2, DR1, DR2
Data hold time	t_{DH}	—	300	—		
Data delay time	t_{PD}	CL=15PF	—	500		DL1, DL2, DR1, DR2

TIMING CHARACTERISTICS

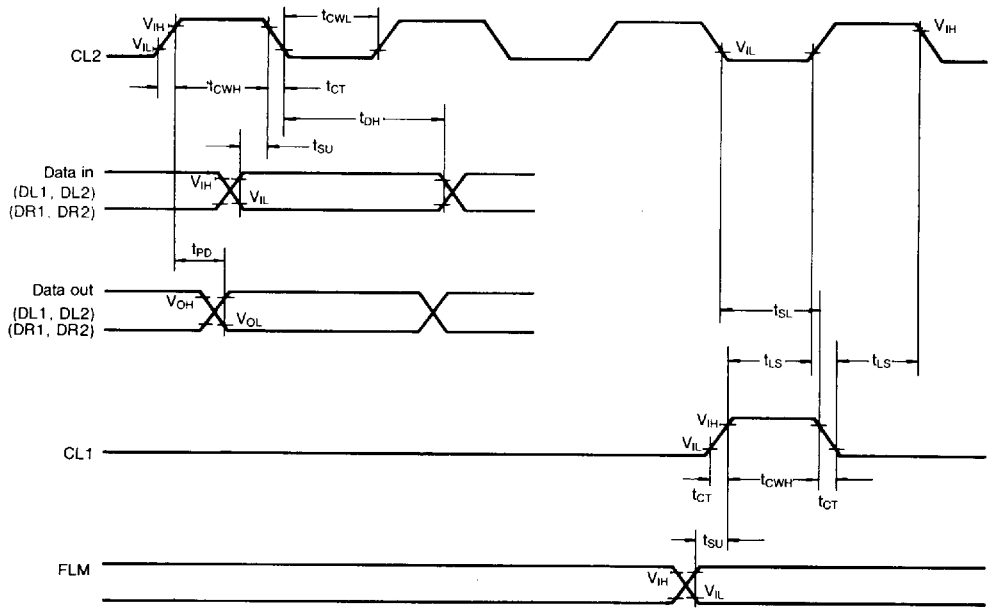
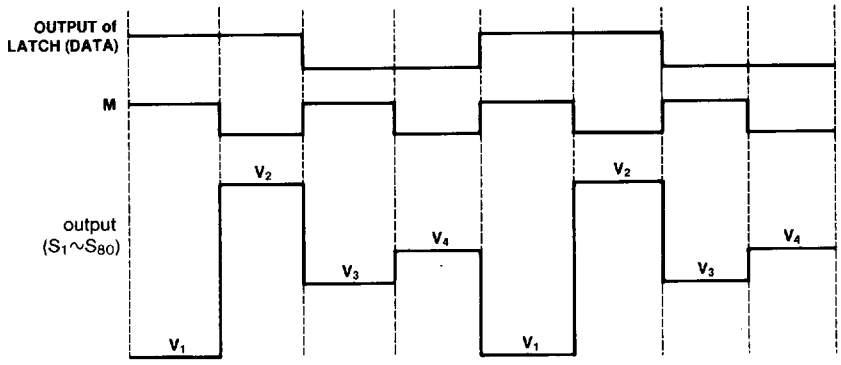
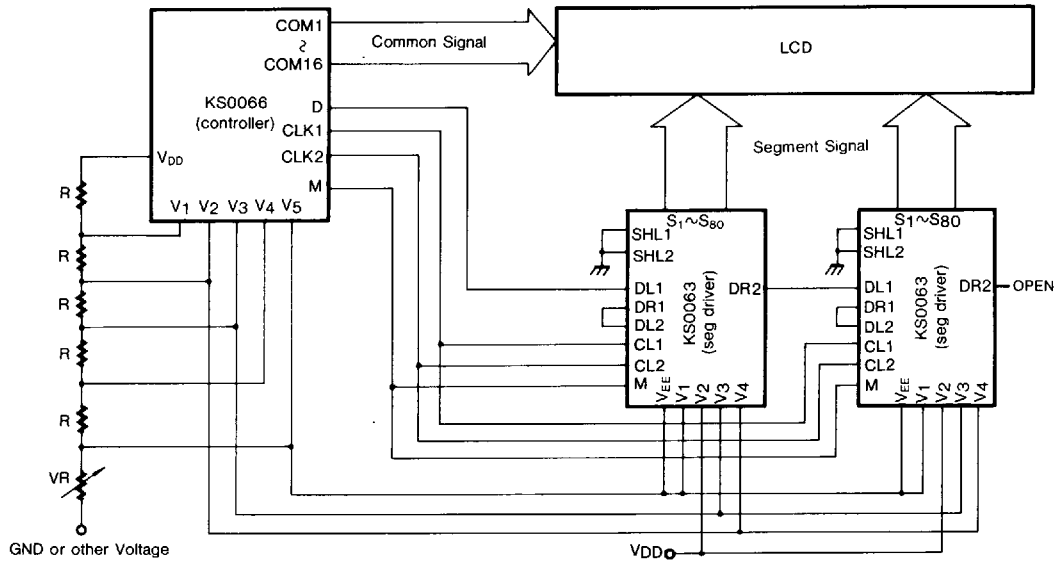


Fig. 3. AC characteristics

LCD OUTPUT WAVEFORMS



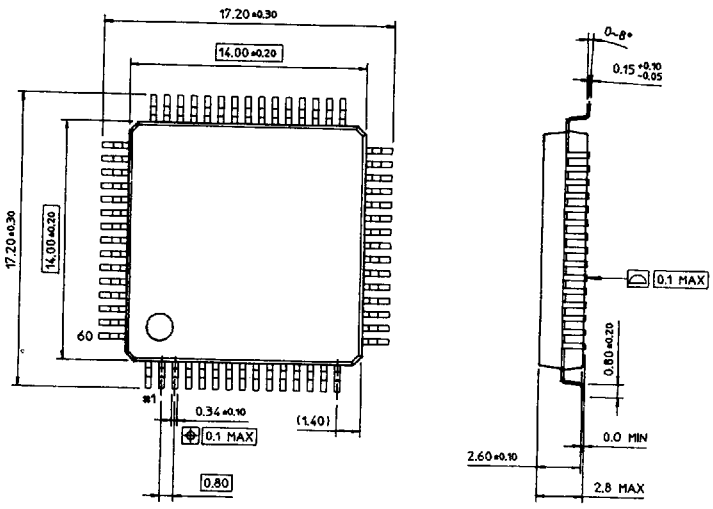
APPLICATION CIRCUIT



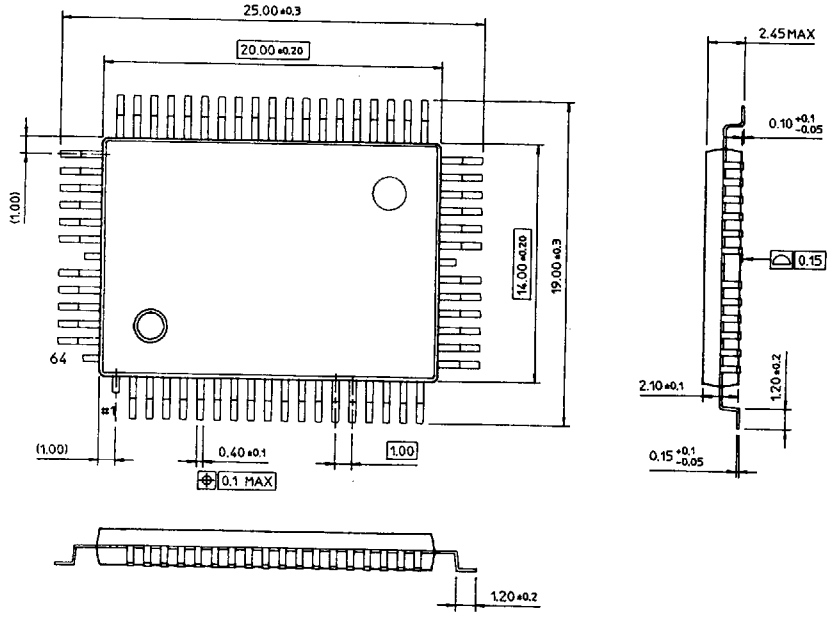
PACKAGE DIMENSIONS

Dimensions in Milimeters

60-QFP-1414A



64-QFP-1420D



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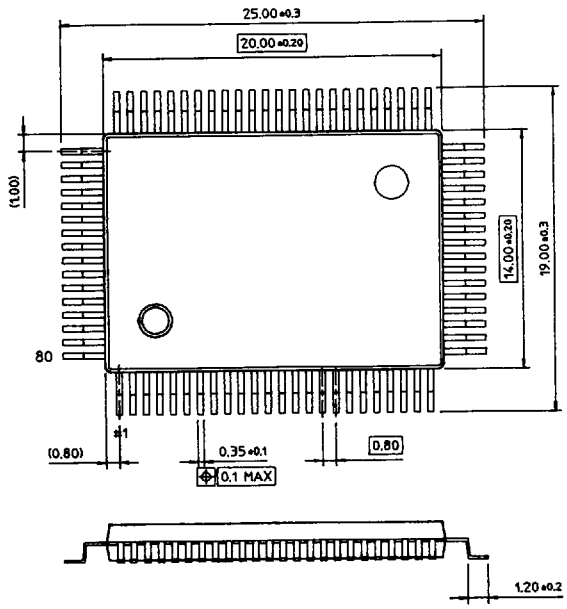
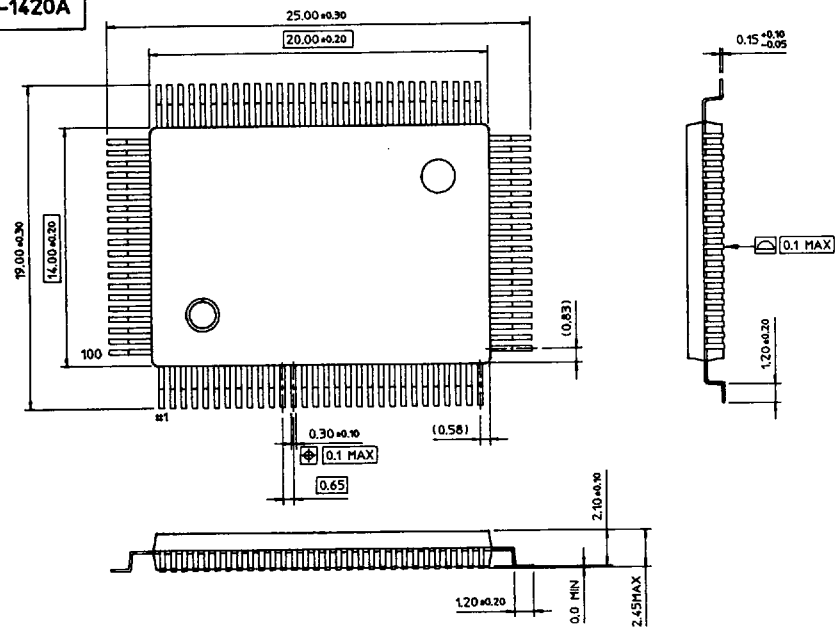
PACKAGE DIMENSIONS

Dimensions in Milimeters

80-QFP-1420A



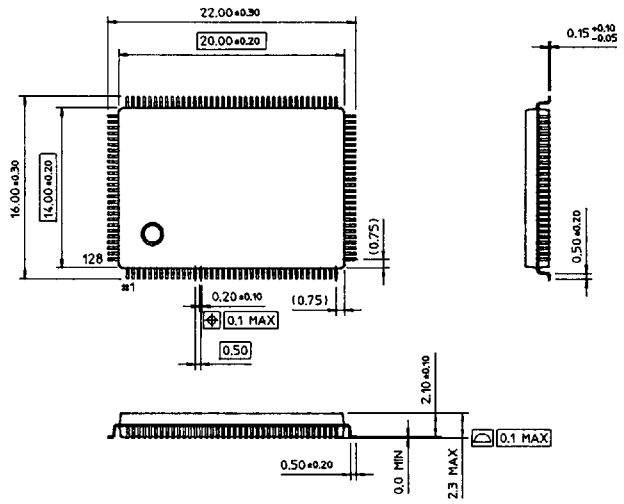
100-QFP-1420A



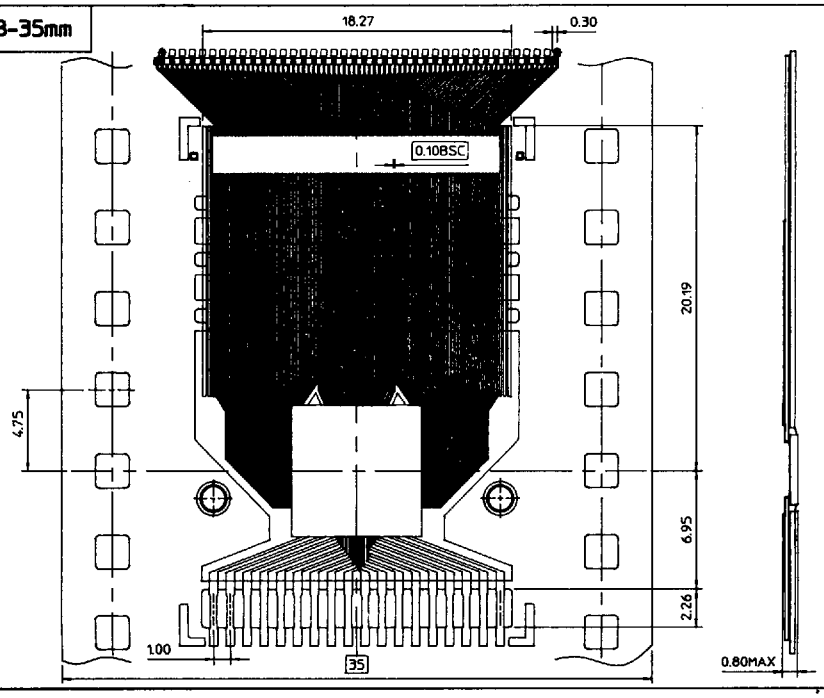
PACKAGE DIMENSIONS

Dimensions in Milimeters

128-QFP-1420



98-TAB-35mm

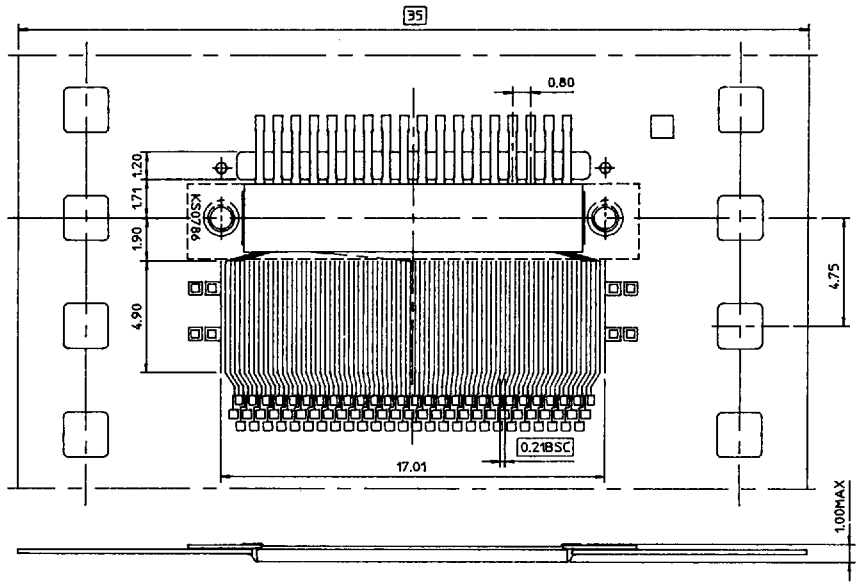


3

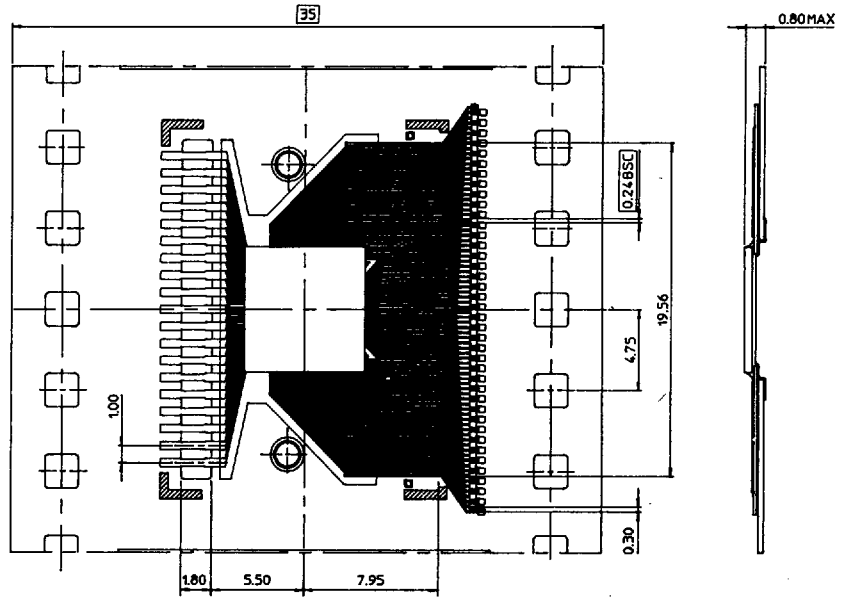
PACKAGE DIMENSIONS

Dimensions in Milimeters

98-STAB-35mm



99-TAB-35mm



PACKAGE DIMENSIONS

Dimensions in Milimeters

120-STAB-35mm