# CS8122

# 2.0% 5.0 V, 750 mA Low Dropout Linear Regulator with Delayed $\overline{\text{RESET}}$

The CS8122 is a precision 5.0 V linear regulator capable of sourcing in excess of 750 mA. The $\overline{\text{RESET}}$'s delay time is externally programmed using a discrete RC network. During power up, or when the output goes out of regulation, the $\overline{\text{RESET}}$ lead remains in the low state for the duration of the delay. This function is independent of the input voltage and will function correctly as long as the output voltage remains at or above 1.0 V. Hysteresis is included in the Delay and the $\overline{\text{RESET}}$ comparators to improve noise immunity. A latching discharge circuit is used to discharge the delay capacitor when it is triggered by a brief fault condition.

The regulator is protected against a variety of fault conditions: i.e. reverse battery, overvoltage, short circuit and thermal runaway conditions. The regulator is protected against voltage transients ranging from –50 V to +40 V. Short circuit current is limited to 1.2 A (typ).

The CS8122 is an improved replacement for the CS8126 and features a tighter tolerance on its output voltage (2.0% vs. 4.0%).

The CS8122 is packaged in a 5 lead TO–220 with copper tab. The copper tab can be connected to a heat sink if necessary.

### Features

- 5.0 V ±2.0% Regulated Output
- Low Dropout Voltage (0.6 V @ 0.5 A)
- 750 mA Output Current Capability
- Externally Programmed $\overline{\text{RESET}}$ Delay
- Fault Protection
  - Reverse Battery
  - 60 V Load Dump
  - –50 V Reverse Transient
  - Short Circuit
  - Thermal Shutdown

ON Semiconductor™

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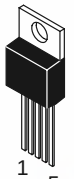
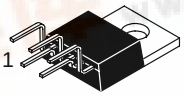
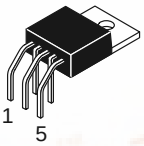



**TO–220**
**FIVE LEAD**
**T SUFFIX**
**CASE 314D**

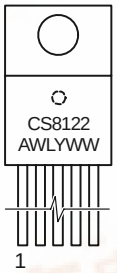



**TO–220**
**FIVE LEAD**
**TVA SUFFIX**
**CASE 314K**




**TO–220**
**FIVE LEAD**
**THA SUFFIX**
**CASE 314A**

### PIN CONNECTIONS AND MARKING INDIAGRAM




Pin 1. $V_{IN}$
2. $V_{OUT}$
3. GND
4. Delay
5. $\overline{\text{RESET}}$

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

### ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| CS8122YT5 | TO–220* STRAIGHT | 50 Units/Rail |
| CS8122YTVA5 | TO–220* VERTICAL | 50 Units/Rail |
| CS8122YTHA5 | TO–220* HORIZONTAL | 50 Units/Rail |

*Five lead.

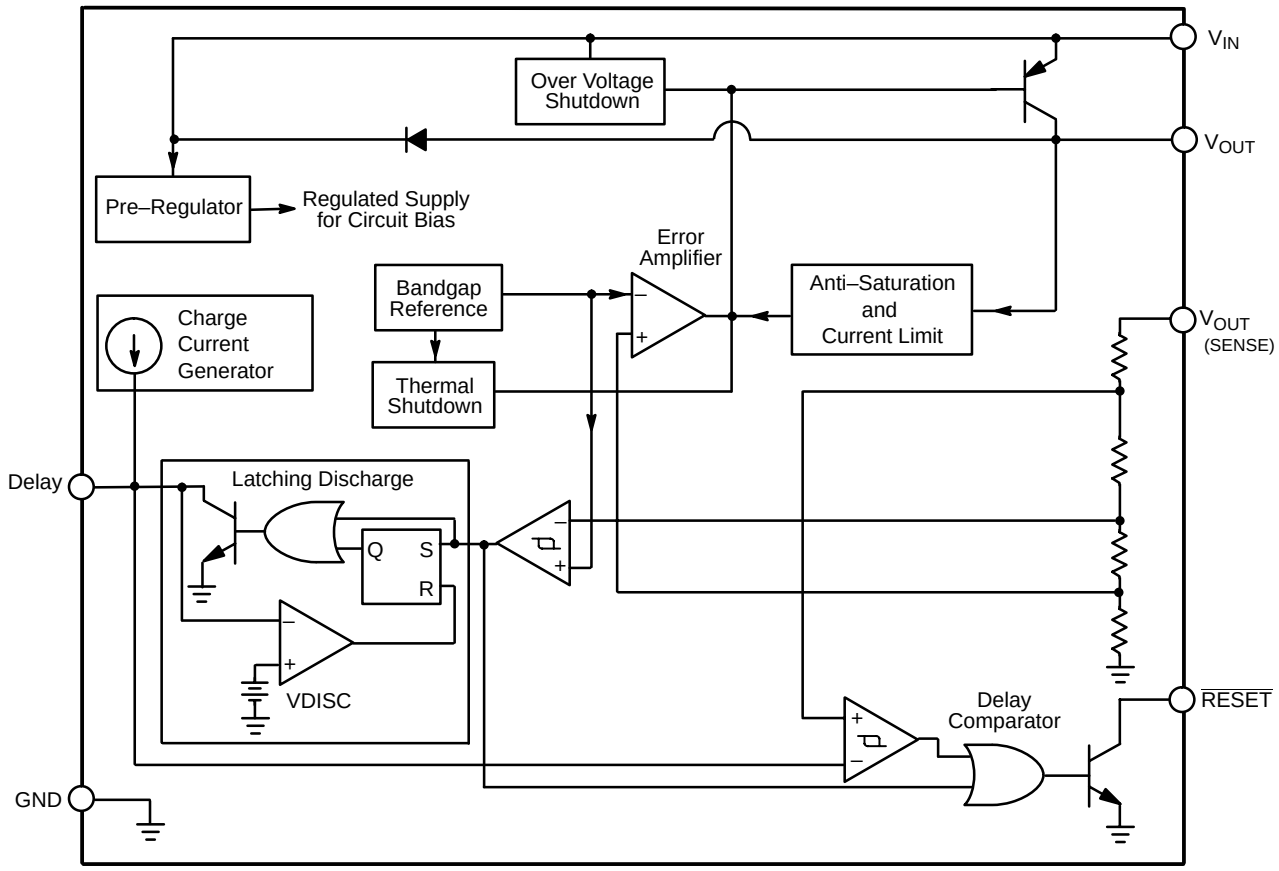



**Figure 1. Block Diagram**

**ABSOLUTE MAXIMUM RATINGS***

| Rating | Value | Unit |
|---|---|---|
| Input Operating Range | –0.5 to 26 | V |
| Power Dissipation | Internally Limited | – |
| Peak Transient Voltage (46 V Load Dump @ $V_{IN}$ = 14 V) | –50, 60 | V |
| Output Current | Internally Limited | – |
| Electrostatic Discharge (Human Body Model) | 4.0 | kV |
| Junction Temperature | –55 to +150 | °C |
| Storage Temperature Range | –55 to +150 | °C |
| Lead Temperature Soldering: Wave Solder (through hole styles only) (Note 1.) | 260 peak | °C |

1. 10 second maximum.

*The maximum package power dissipation must be observed.

**ELECTRICAL CHARACTERISTICS** (–40°C ≤ $T_A$ ≤ 125°C, –40 ≤ $T_J$ ≤ 150°C, 6.0 ≤ $V_{IN}$ ≤ 26 V, 5.0 mA ≤ $I_{OUT}$ ≤ 500 mA, $R_{\overline{RESET}}$ = 4.7 kΩ to $V_{CC}$ unless otherwise noted.) Note 2.

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Output Stage ($V_{OUT}$)** | | | | | |
| Output Voltage | – | 4.9 | 5.0 | 5.1 | V |
| Dropout Voltage | $I_{OUT}$ = 500 mA | – | 0.35 | 0.60 | V |
| Supply Current | $I_{OUT}$ ≤ 10 mA<br>$I_{OUT}$ ≤ 100 mA<br>$I_{OUT}$ ≤ 500 mA | –<br>–<br>– | 2.0<br>6.0<br>55 | 7.0<br>12<br>100 | mA<br>mA<br>mA |
| Line Regulation | 6.0 V ≤ $V_{IN}$ ≤ 26 V, $I_{OUT}$ = 50 mA | – | 5.0 | 50 | mV |
| Load Regulation | 50 mA ≤ $I_{OUT}$ ≤ 500 mA, $V_{IN}$ = 14 V | – | 10 | 50 | mV |
| Ripple Rejection | f = 120 Hz, 7.0 ≤ $V_{IN}$ ≤ 17 V, $I_{OUT}$ = 250 mA | 54 | 75 | – | dB |
| Current Limit | – | 0.75 | 1.20 | – | A |
| Overvoltage Shutdown | – | 32 | – | 40 | V |
| Maximum Line Transient | $V_{OUT}$ ≤ 5.5 V | 60 | 95 | – | V |
| Reverse Polarity Input Voltage DC | $V_{OUT}$ ≥ –0.6 V, 10 Ω Load | –15 | –30 | – | V |
| Reverse Polarity Input Voltage Transient | 1.0% Duty Cycle, T < 100 ms, 10 Ω Load | –50 | –80 | – | V |
| Thermal Shutdown | Guaranteed by Design | 150 | 180 | 210 | °C |
| **$\overline{RESET}$ and Delay Functions** | | | | | |
| Delay Charge Current | $V_{DELAY}$ = 2.0 V | 5.0 | 10 | 15 | μA |
| $\overline{RESET}$ Threshold | $V_{OUT}$ Increasing, $V_{RT(ON)}$<br>$V_{OUT}$ Decreasing, $V_{RT(OFF)}$ | 4.65<br>4.50 | 4.90<br>4.70 | $V_{OUT}$ – 0.01<br>$V_{OUT}$ – 0.16 | V<br>V |
| $\overline{RESET}$ Hysteresis | $V_{RH}$ = $V_{RT(ON)}$ – $V_{RT(OFF)}$ | 150 | 200 | 250 | mV |
| Delay Threshold | Charge, $V_{DC(HI)}$<br>Discharge, $V_{DC(L)}$ | 3.25<br>2.85 | 3.50<br>3.10 | 3.75<br>3.35 | V<br>V |
| Delay Hysteresis | – | 200 | 400 | 800 | mV |
| $\overline{RESET}$ Output Voltage Low | 1.0 V < $V_{OUT}$ < $V_{RT(L)}$, 3.0 kΩ to $V_{OUT}$ | – | 0.1 | 0.4 | V |
| $\overline{RESET}$ Output Leakage | $V_{OUT}$ > $V_{RT(H)}$ | 0 | – | 10 | μA |
| Delay Capacitor Discharge Voltage | Discharge Latched “ON”, $V_{OUT}$ > $V_{RT}$ | – | 0.2 | 0.5 | V |
| Delay Time | $C_{DELAY}$ = 0.1 μF | 16 | 32 | 48 | ms |

2. To observe safe operating junction temperatures, low duty cycle pulse testing is used in tests where applicable.

$$\text{DelayTime} = \frac{C_{Delay} \times V_{Delay\ Threshold\ Charge}}{I_{Charge}} = C_{Delay} \times 3.5 \times 10^5 (\text{typ})$$

**PACKAGE LEAD DESCRIPTION**

| PACKAGE LEAD # | | |
|---|---|---|
| TO–220 5 LEAD | LEAD SYMBOL | FUNCTION |
| 1 | $V_{IN}$ | Unregulated supply voltage to IC. |
| 2 | $V_{OUT}$ | Regulated 5.0 V output. |
| 3 | GND | Ground Connection. |
| 4 | Delay | Timing capacitor for $\overline{\text{RESET}}$ function. |
| 5 | $\overline{\text{RESET}}$ | CMOS/TTL compatible output lead. $\overline{\text{RESET}}$ goes low whenever $V_{OUT}$ drops below 6.0% of it's regulated value. |

## TYPICAL PERFORMANCE CHARACTERISTICS

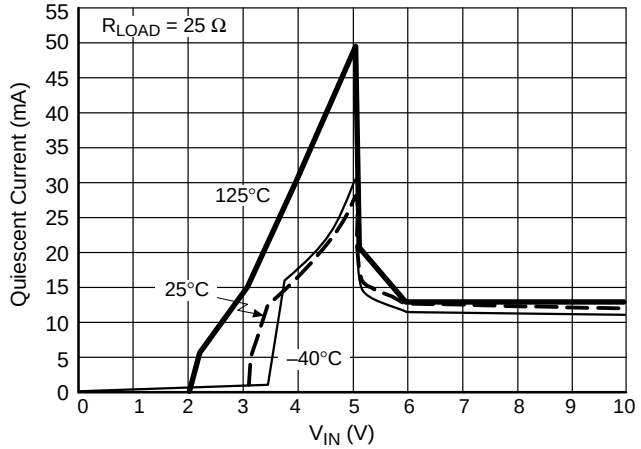



**Figure 2. Quiescent Current vs. Input Voltage Over Temperature**

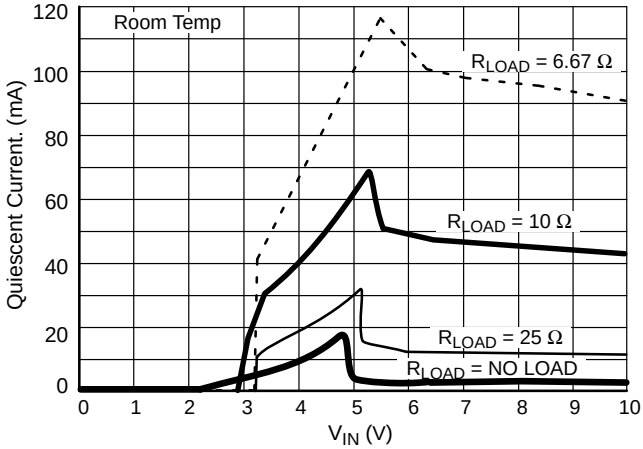



**Figure 3. Quiescent Current vs. Input Voltage Over Load Resistance**

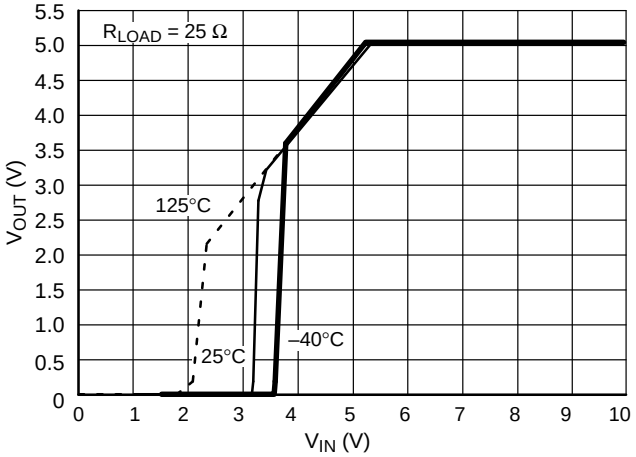



**Figure 4. Output Voltage vs. Input Voltage Over Temperature**

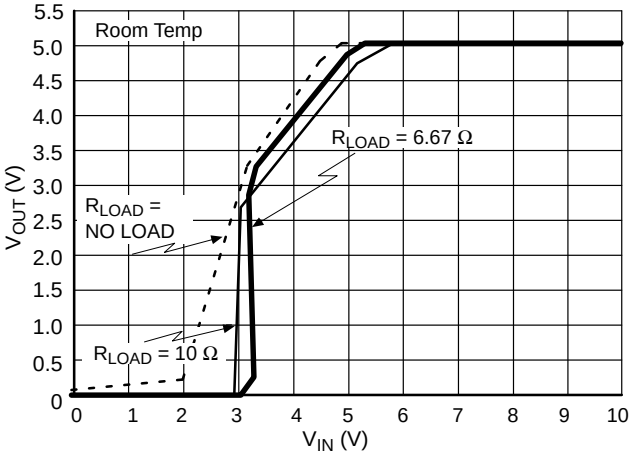



**Figure 5. $V_{OUT}$ vs. $V_{IN}$ Over $R_{LOAD}$**

## TYPICAL PERFORMANCE CHARACTERISTICS

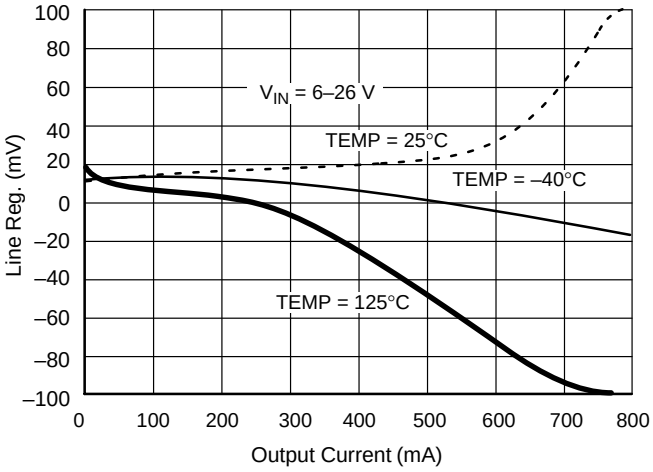



**Figure 6. Line Regulation vs. Output Current**

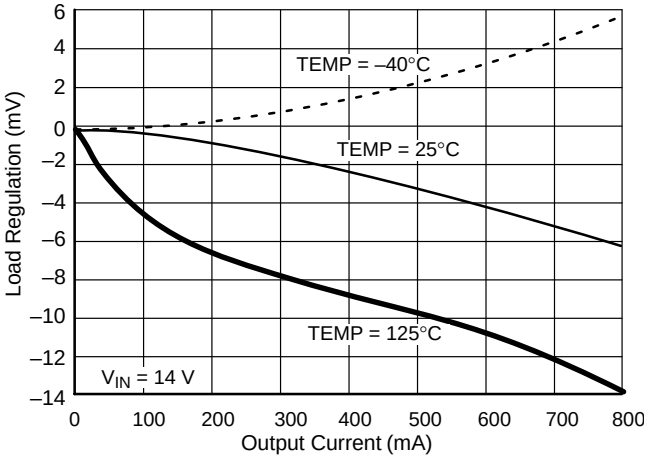



**Figure 7. Load Regulation vs. Output Current**

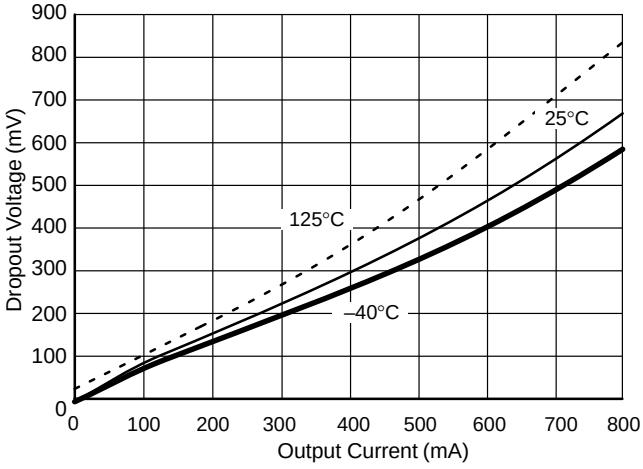



**Figure 8. Dropout Voltage vs. Output Current**

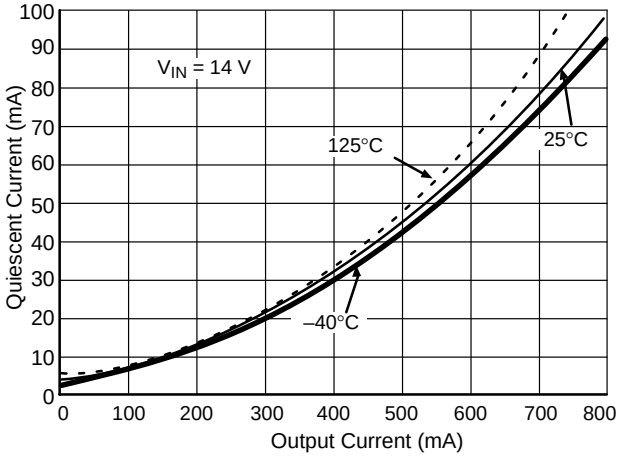



**Figure 9. Quiescent Current vs. Output Current**

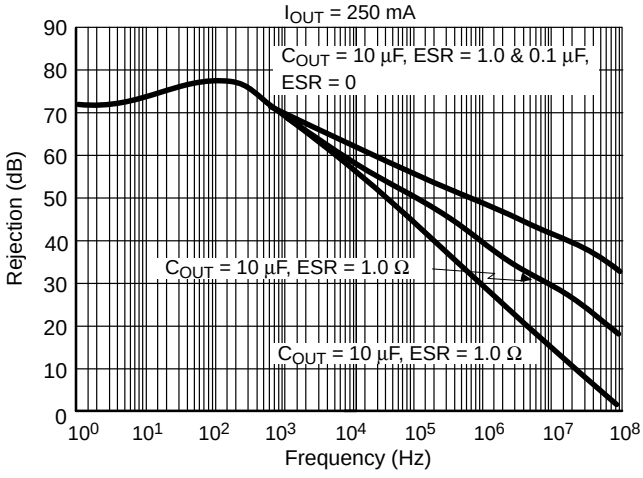



**Figure 10. Ripple Rejection**

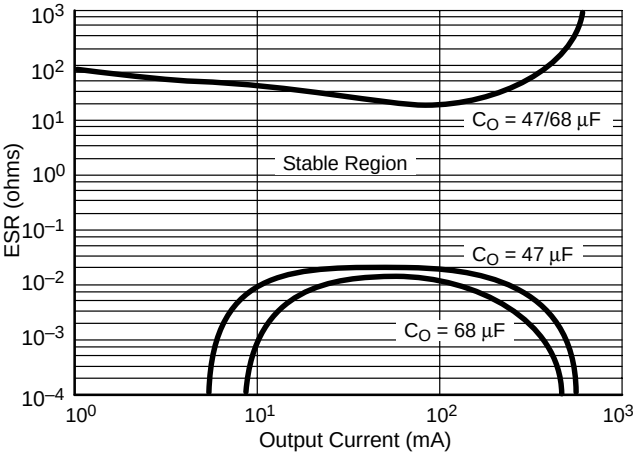



**Figure 11. Output Capacitor ESR**

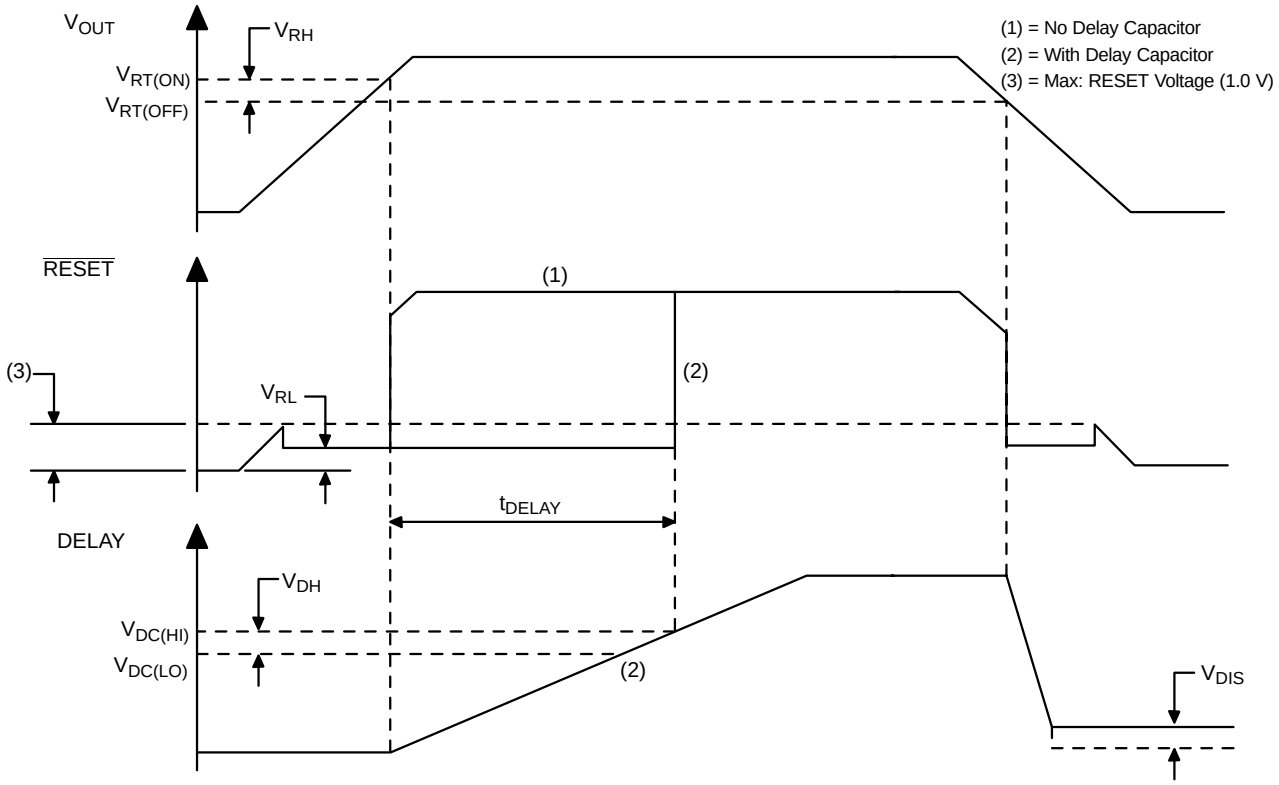



**Figure 12. $\overline{\text{RESET}}$ Circuit Waveform**

## CIRCUIT DESCRIPTION

The CS8122 $\overline{\text{RESET}}$ function, has hysteresis on both the reset and delay comparators, a latching Delay capacitor discharge circuit, and operates down to 1.0 V.

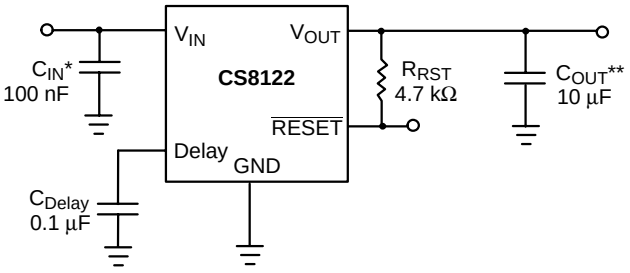
The $\overline{\text{RESET}}$ circuit output is an open collector type with ON and OFF parameters as specified. The $\overline{\text{RESET}}$ output NPN transistor is controlled by the two circuits described (see Block Diagram on page 2).

### Low Voltage Inhibit Circuit

The Low Voltage Inhibit Circuit monitors output voltage, and when output voltage is below the specified minimum, causes the $\overline{\text{RESET}}$ output transistor to be in the ON (saturation) state. When the output voltage is above the specified level, this circuit permits the $\overline{\text{RESET}}$ output transistor to go into the OFF state if allowed by the $\overline{\text{RESET}}$ Delay circuit.

### Reset Delay Circuit

The Reset Delay Circuit provides a programmable (by external capacitor) delay on the $\overline{\text{RESET}}$ output lead. The Delay lead provides source current to the external delay capacitor only when the Low Voltage Inhibit circuit indicates that output voltage is above $V_{RT(ON)}$. Otherwise, the Delay lead sinks current to ground (used to discharge the delay capacitor). The discharge current is latched ON when the output voltage is below $V_{RT(OFF)}$. The Delay capacitor is fully discharged anytime the output voltage falls out of regulation, even for a short period of time. This feature ensures that a controlled $\overline{\text{RESET}}$ pulse is generated following detection of an error condition. The circuit allows the $\overline{\text{RESET}}$ output transistor to go to the OFF (open) state only when the voltage on the Delay lead is higher than $V_{DC(HI)}$.




*$C_{IN}$ is required if regulator is far from the power source filter.

**$C_{OUT}$ is required for stability.

**Figure 13. Test Circuit**

## APPLICATION NOTES

### STABILITY CONSIDERATIONS

The output or compensation capacitor, $C_{OUT}$, helps determine three main characteristics of a linear regulator: start–up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (–25°C to –40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor $C_{OUT}$ shown in Figure 13 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for $C_{OUT}$ for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

**Step 1:** Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

**Step 2:** With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

**Step 3:** Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

**Step 4:** Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

**Step 5:** If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

**Step 6:** Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

**Step 7:** Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ± 20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

### CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 14) is:

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT(min)}\}I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

$I_Q$ is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

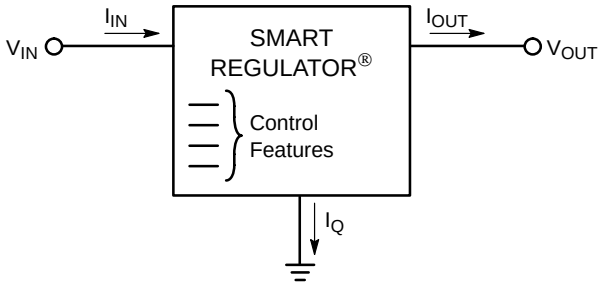



**Figure 14. Single Output Regulator With Key Performance Parameters Labeled**

## HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$.

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\Theta JC}$ = the junction–to–case thermal resistance,

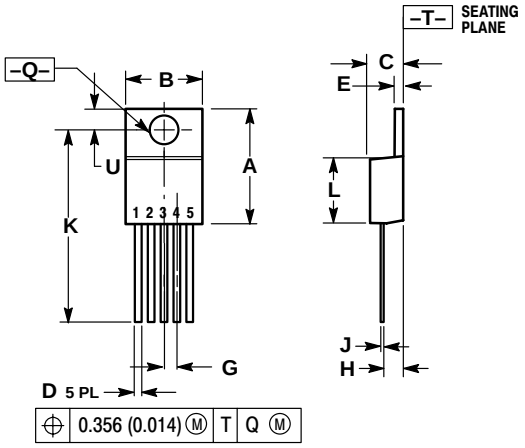
$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and

$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it too is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## PACKAGE DIMENSIONS

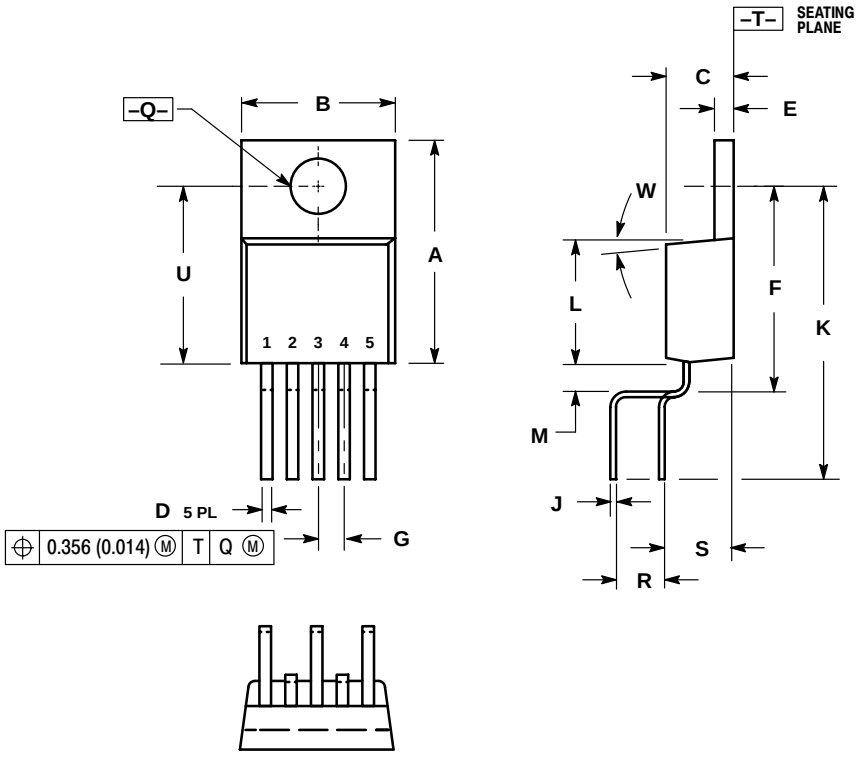
**TO–220**
**FIVE LEAD**
**T SUFFIX**
CASE 314D–04
ISSUE E




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.572 | 0.613 | 14.529 | 15.570 |
| B | 0.390 | 0.415 | 9.906 | 10.541 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.025 | 0.038 | 0.635 | 0.965 |
| E | 0.048 | 0.055 | 1.219 | 1.397 |
| G | 0.067 BSC | | 1.702 BSC | |
| H | 0.087 | 0.112 | 2.210 | 2.845 |
| J | 0.015 | 0.025 | 0.381 | 0.635 |
| K | 0.990 | 1.045 | 25.146 | 26.543 |
| L | 0.320 | 0.365 | 8.128 | 9.271 |
| Q | 0.140 | 0.153 | 3.556 | 3.886 |
| U | 0.105 | 0.117 | 2.667 | 2.972 |

**TO–220**
**FIVE LEAD**
**TVA SUFFIX**
CASE 314K–01
ISSUE O

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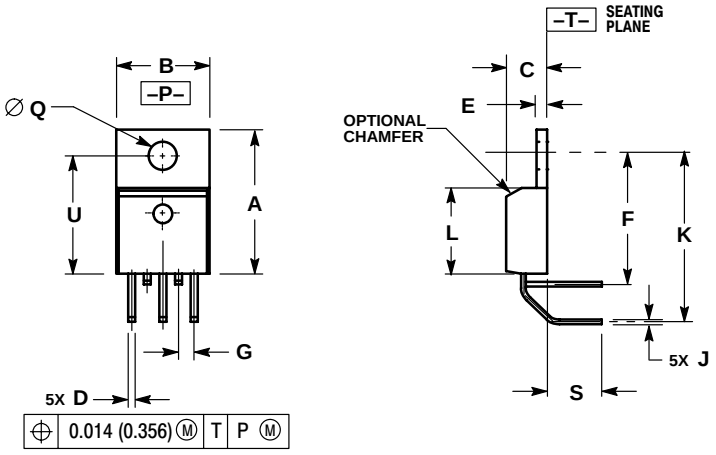
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.560 | 0.590 | 14.22 | 14.99 |
| B | 0.385 | 0.415 | 9.78 | 10.54 |
| C | 0.160 | 0.190 | 4.06 | 4.83 |
| D | 0.027 | 0.037 | 0.69 | 0.94 |
| E | 0.045 | 0.055 | 1.14 | 1.40 |
| F | 0.530 | 0.545 | 13.46 | 13.84 |
| G | 0.067 BSC | | 1.70 BSC | |
| J | 0.014 | 0.022 | 0.36 | 0.56 |
| K | 0.785 | 0.800 | 19.94 | 20.32 |
| L | 0.321 | 0.337 | 8.15 | 8.56 |
| M | 0.063 | 0.078 | 1.60 | 1.98 |
| Q | 0.146 | 0.156 | 3.71 | 3.96 |
| R | 0.271 | 0.321 | 6.88 | 8.15 |
| S | 0.146 | 0.196 | 3.71 | 4.98 |
| U | 0.460 | 0.475 | 11.68 | 12.07 |
| W | 5 ° | | 5 ° | |

# CS8122

**TO–220**
**FIVE LEAD**
**THA SUFFIX**
CASE 314A–03
ISSUE E

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| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.572 | 0.613 | 14.529 | 15.570 |
| B | 0.390 | 0.415 | 9.906 | 10.541 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.025 | 0.038 | 0.635 | 0.965 |
| E | 0.048 | 0.055 | 1.219 | 1.397 |
| F | 0.570 | 0.585 | 14.478 | 14.859 |
| G | 0.067 BSC | | 1.702 BSC | |
| J | 0.015 | 0.025 | 0.381 | 0.635 |
| K | 0.730 | 0.745 | 18.542 | 18.923 |
| L | 0.320 | 0.365 | 8.128 | 9.271 |
| Q | 0.140 | 0.153 | 3.556 | 3.886 |
| S | 0.210 | 0.260 | 5.334 | 6.604 |
| U | 0.468 | 0.505 | 11.888 | 12.827 |

**PACKAGE THERMAL DATA**

| Parameter | | TO–220 FIVE LEAD | Unit |
|---|---|---|---|
| $R_{\Theta JC}$ | Typical | 2.1 | °C/W |
| $R_{\Theta JA}$ | Typical | 50 | °C/W |

# Notes

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