CS8271

Adjustable Micropower Low Dropout Linear Regulator with $\overline{\text{ENABLE}}$

The CS8271 is an adjustable micropower voltage regulator with very low quiescent current (60 µA typical at 100 µA load). The output supplies 100 mA of load current with a maximum dropout voltage of only 600 mV. Control logic includes $\overline{\text{ENABLE}}$. The combination of low quiescent current, outstanding regulator performance and control logic makes the CS8271 ideal for any battery operated equipment.

The logic level $\overline{\text{ENABLE}}$ compatible pin allows the user to put the regulator into a shutdown mode where it draws only 50 µA of quiescent current.

The regulator is protected against reverse battery, short circuit, over voltage, and over temperature conditions. The device can withstand 60 V load dump transients making it suitable for use in automotive environments.

The CS8271 is pin compatible with the National Semiconductor LM2931.

Features

- Low Quiescent Current
- Adjustable Output: 5.0 V to 12 V
- $\overline{\text{ENABLE}}$ for Sleep Mode Control
- 100 mA Output Current Capability
- Fault Protection
  - +60 V Load Dump
  - –15 V Reverse Voltage Short Circuit
  - Thermal Shutdown
- Low Reverse Current (Output to Input)

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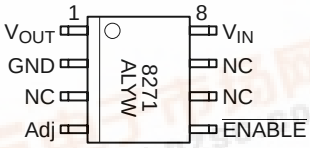
SO–8
D SUFFIX
CASE 751

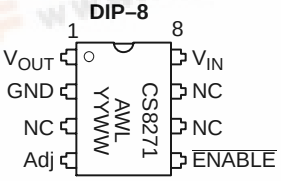
DIP–8
N SUFFIX
CASE 626

PIN CONNECTIONS AND MARKING DIAGRAM

SO–8



DIP–8



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION*

Device	Package	Shipping
CS8271YD8	SO–8	95 Units/Rail
CS8271YDR8	SO–8	2500 Tape & Reel
CS8271YN8	DIP–8	50 Units/Rail

*Consult your local sales representative for other package options.

Publication Order Number:

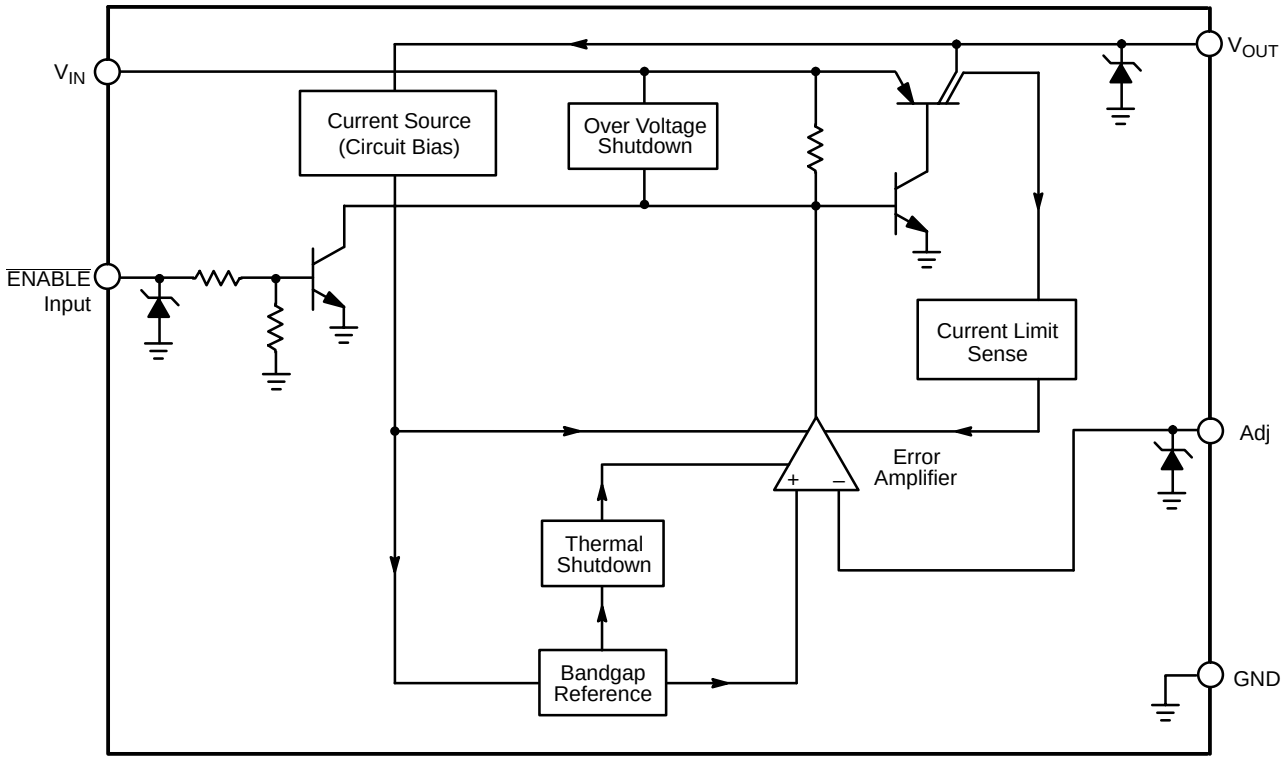


Figure 1. Block Diagram

MAXIMUM RATINGS*

Rating		Value	Unit
Power Dissipation		Internally Limited	–
Peak Transient Voltage (46 V Load Dump @ V_{IN} = 14 V)		–50, 60	V
Reverse Battery		–15	V
Output Current		Internally Limited	–
ESD Susceptibility (Human Body Model)		2.0	kV
Junction Temperature		–40 to +150	°C
Storage Temperature		–55 to +150	°C
Lead Temperature Soldering:	Wave Solder (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2)	260 peak 230 peak	°C °C
Adj, $\overline{\text{ENABLE}}$		–0.3, 10	V
V_{OUT}		–0.3, 20	V

1. 10 second maximum.
2. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (V_{OUT} + 1.0 V ≤ V_{IN} ≤ 30 V, 5.0 V ≤ V_{OUT} ≤ 12 V, I_{OUT} = 10 mA, –40°C ≤ T_A ≤ 125°C, –40°C ≤ T_J ≤ 150°C, V_{ENABLE} = 0 V; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Voltage					
Dropout Voltage	I_{OUT} = 100 μA, V_{DROP} = (V_{IN} – V_{OUT}) I_{OUT} = 100 mA, V_{DROP} = (V_{IN} – V_{OUT})	– –	100 400	150 600	mV mV
Load Regulation	Measure V_{OUT} when I_{OUT} = 100 μA, 100 mA. LD_{REG} = ABS (ΔV_{OUT})	–	0.1	1.0	%V_{OUT}
Line Regulation	I_{OUT} = 1.0 mA. Measure V_{OUT} when V_{IN} = V_{OUT} + 1.0 V, 30 V, LN_{REG} = ABS (ΔV_{OUT})	–	0.1	0.5	%V_{OUT}
Quiescent Current, (I_Q) Active Mode	V_{IN} = 6.0 V, I_{OUT} = 100 μA, V_{OUT} setup for 5.0 V, I_Q = IV_{IN} – I_{OUT} V_{IN} = 13 V, I_{OUT} = 100 μA, V_{OUT} setup for 12 V, I_Q = IV_{IN} – 100 μA V_{IN} = 30 V, I_{OUT} = 100 μA, V_{OUT} setup for 5.0 V. I_Q = IV_{IN} – 100 μA V_{IN} = 30 V, I_{OUT} = 100 μA, V_{OUT} setup for 12 V. I_Q = IV_{IN} – 100 μA I_{OUT} = 50 mA, I_Q = IV_{IN} – 50 mA I_{OUT} = 100 mA, I_Q = IV_{IN} – 100 mA	– – – – – –	55 130 150 20 4.0 12	120 200 450 500 7.0 21	μA μA μA μA mA mA
Quiescent Current, (I_Q) Sleep Mode	V_{IN} = 6.0 V, $\overline{ENABLE}$ = 2.5 V, I_{QSLEEP} = IV_{IN} V_{IN} = 30 V, $\overline{ENABLE}$ = 2.5 V, I_{QSLEEP} = IV_{IN}	– –	20 75	50 350	μA μA
Ripple Rejection	f = 120 Hz, Note 3	60	75	–	dB
Current Limit	V_{OUT} = V_{OUT} – 500 mV, I_{LIM} = IV_{OUT}	105	200	300	mA
Short Circuit Output Current	V_{OUT} = 0 V, I_{SHRT} = IV_{OUT}	15	100	215	mA
Thermal Limit	Note 3	150	180	210	°C
Overvoltage Shutdown	Adjust V_{IN} from 28 V to 40 V until V_{OUT} ≤ 1.0 V	30	34	38	V
Reverse Current	V_{IN} = 0 V, I_{REV} = IV_{OUT}, V_{OUT} = 13.2 V	–	100	200	μA
$\overline{ENABLE}$					
Enable Threshold	–	1.15	2.0	2.6	V
Enable Input Current	$V_{\overline{ENABLE}}$ = 2.6 V $V_{\overline{ENABLE}}$ = 5.0 V	– –	10 35	20 50	μA μA
Adjustment Pin	**R1: Feedback resistor between V_{OUT} and Adjust, R2: Adjust resistor to ground.**				
Reference Voltage	100 μA ≤ I_{OUT} ≤ 100 mA	1.246	1.272	1.297	V
Adjustment Pin Current	I_{ADJ} = (V_{REF}/R2) – ((V_{OUT} – V_{REF})/R1)	–	20	500	nA

3. Guaranteed by design, not 100% tested in production.

PACKAGE LEAD DESCRIPTION

PACKAGE LEAD #		LEAD SYMBOL	FUNCTION
SO–8	DIP–8		
1	1	V_{OUT}	100 mA output; adjustable from 5.0 V to 12 V.
2	2	GND	Ground.
3, 6, 7	3, 6, 7	NC	No connection.
4	4	Adj	Resistor divider from V_{OUT} to Adj, sets output voltage.
5	5	$\overline{ENABLE}$	Logic level switch, when High, regulator is in sleep mode.
8	8	V_{IN}	Input voltage.

CIRCUIT DESCRIPTION

OUTPUT VOLTAGE ADJUSTMENT

The output voltage of the CS8271 is adjustable to any value between 5.0 V and the maximum input voltage minus the dropout voltage. To adjust the output voltage, a pair of external resistors R1 and R2 are connected as shown in Figure 2.

The equation for the output voltage is

$$V_{OUT} = V_{REF} \times \left(\frac{R1 + R2}{R2}\right) + I_{Adj} \times R1$$

where V_{REF} is the typical reference voltage and I_{Adj} is the adjust pin bias current. This is usually 500 nA maximum.

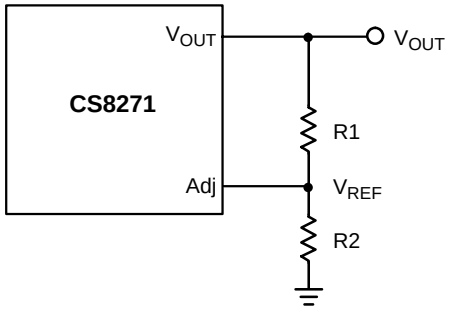


Figure 2. Output Voltage Adjustment

OUTPUT STAGE PROTECTION

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 3).

If the input voltage rises above 30 V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients up to 60 V in magnitude.

Short circuit protection limits the amount of current the output transistor can supply. In the case of a CS8271 under a short circuit condition, the output transistor current is limited to 100 mA.

Should the junction temperature of the power device exceed 180°C (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

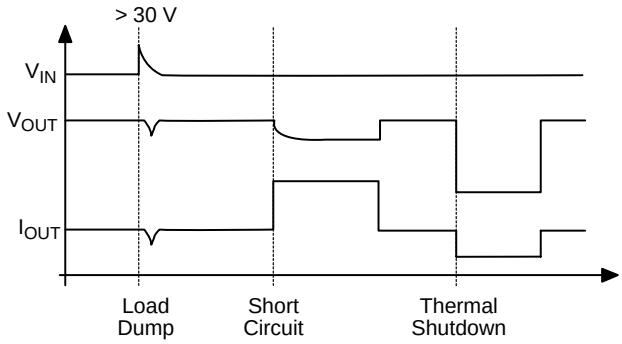


Figure 3. Typical Circuit Waveforms for Output Stage Protection

$\overline{\text{ENABLE}}$

The $\overline{\text{ENABLE}}$ function switches the output transistor. When the voltage on the $\overline{\text{ENABLE}}$ pin exceeds 2.0 V typ, the output pass transistor turns off, leaving a high impedance facing the load. The IC will remain in Sleep mode, drawing only 20 μA (typ), until the voltage on this input drops below the $\overline{\text{ENABLE}}$ threshold.

APPLICATION NOTES

SELECTING THE RIGHT CAPACITOR VALUE

The output compensation capacitor C_{OUT}, determines three main characteristics of a linear regulator: start–up delay, load transient response and loop stability.

The selection of a capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (–25°C to –40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provide this information.

The value for the output compensation capacitor COUT shown in Figure 4 should work for most applications, but it is not necessarily the least expensive or the optimal solution.

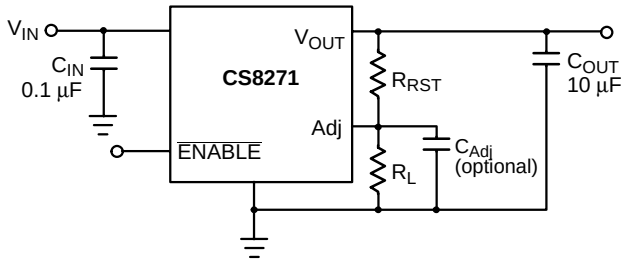


Figure 4. Test and Application Circuit Showing An Output Compensation Capacitor

To determine an acceptable value for C_{OUT} for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. (Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible).

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. (A smaller capacitor will usually cost less and occupy less board space.) If the capacitor oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real work environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ± 20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

Capacitance on the Adjust pin combined with the feedback resistors R1 and R2 can affect loop stability and should also be considered. The CS8271 internal circuitry produces about 5.0 pF to Ground on the Adjust pin. This capacitance, plus any additional external capacitance on the Adjust pin will create a pole when combined with the resistive feedback network. The effect can be significant when using large values for the feedback resistors to minimize quiescent current.

A capacitor connected from the Adjust pin to Ground provides additional means to compensate the regulator by creating a pole. Alternately, a capacitor can be connected from the Adjust pin to V_{OUT} to create a zero.

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 5) is:

$$P_{D(max)} = |V_{IN(max)} - V_{OUT(min)}|I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

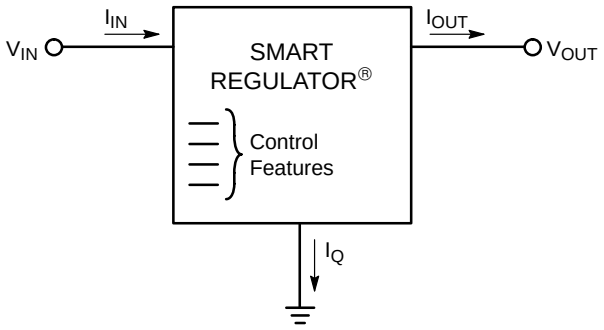
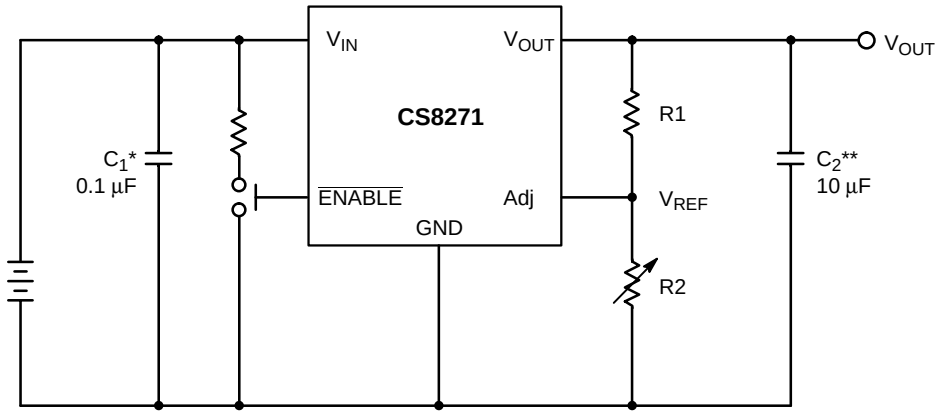


Figure 5. Single Output Regulator With Key Performance Parameters Labeled



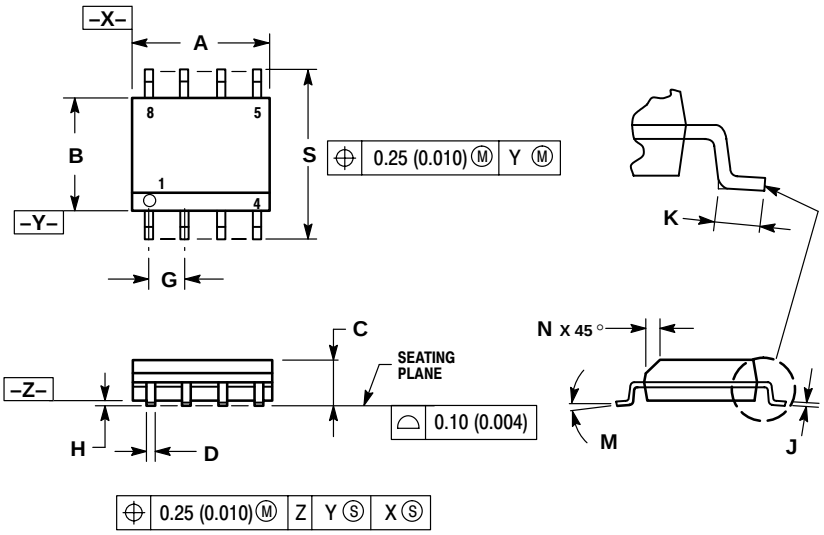
C_1* Required if regulator is away from power supply filter.
C_2** Required for output stability.

$$V_{OUT} = V_{REF} \times \left(\frac{R1 + R2}{R2}\right) + I_{Adj} \times R1$$

Figure 6. Application Diagram

PACKAGE DIMENSIONS

SO–8
D SUFFIX
CASE 751–07
ISSUE W



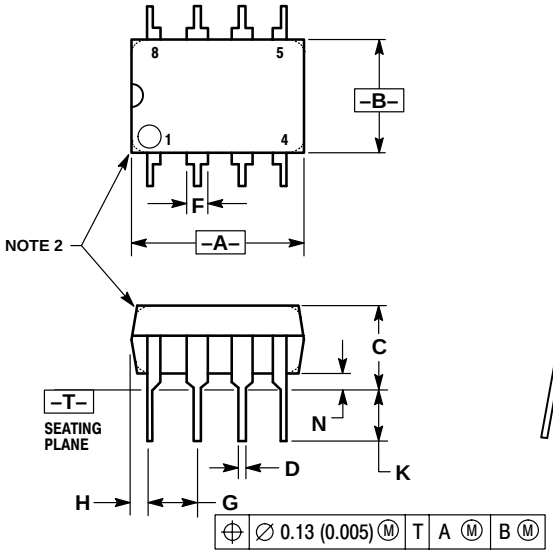
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

CS8271

PACKAGE DIMENSIONS

DIP–8
N SUFFIX
CASE 626–05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

PACKAGE THERMAL DATA

Parameter		SO–8	DIP–8	Unit
$R_{\Theta JC}$	Typical	45	52	°C/W
$R_{\Theta JA}$	Typical	165	100	°C/W

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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