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PMC-Sierra

Preliminary

# PM7341 S/UNI®-IMA-84

## 84 Link Inverse Multiplexer for ATM (IMA) / UNI PHY

## FEATURES

### IMA

- Supports up to 84 T1 or 63 E1 links and up to 42 IMA groups with 1 to 32 links/group.
- Link and Group State Machines implemented on-chip requiring no real time software in the data path.
- Fully compliant with the ATM Forum Inverse Multiplexer for ATM (IMA) 1.1 specification and backward compatible to IMA 1.0.
- Supports both independent transmit clock (ITC) and common transmit clock (CTC) modes.
- Supports all IMA Group Symmetry modes: Symmetric/Asymmetric configuration and operation.
- Differential delay tolerance of 279 ms (for T1 links) and 226 ms (for E1 links).
- Performs IMA differential delay calculation and synchronization.
- Provides programmable limit on allowable differential delay and minimum number of links per group.
- Performs ICP and stuff-cell insertion and removal.
- Supports IMA frame length (M) equal to 32, 64, 128, or 256.
- Provides IMA layer statistic counts and alarms for support of IMA Performance and Failure Alarm Monitoring and MIB support.
- Provides per link counters for statistics and performance monitoring.

### UNI

- Supports up to 84/63 ATM over T1/E1 UNIs or 3 ATM over DS3 UNIs.
- Each T1/E1 link is software configurable as either a UNI or part of an IMA group.
- Performs receive cell Header Error Check (HEC) checking and transmit cell HEC generation.
- Optionally supports receive cell payload unscrambling and transmit cell payload scrambling.
- Provides TC layer statistics counts and alarms for MIB support.

### ATM OVER FRACTIONAL T1/E1

- Supports up to 32 ATM over Fractional T1/E1 UNIs over the clock/data interface, compliant with the ATM Forum AF-PHY-0130.00 specification.

### LINE INTERFACE

- Supports a 19.44 MHz Scalable Bandwidth Interconnect (SBI) bus interface for seamless interconnect to the PM8315 TEMUX and PM8316 TEMUX-84.
- SBI supports three Synchronous Payload Envelopes (SPE) where each SPE can carry up to 28 T1s, 21 E1s, or one unchannelized DS3 stream.
- Supports up to 32 T1, E1, G.SHDSL or unchannelized links via 2-pin line interfaces.

### UTOPIA / ANY-PHY INTERFACE

- Supports 8- and 16-bit UTOPIA L2 and Any-PHY cell interfaces at clock rates up to 52 MHz.
- Any-PHY transmit slave appears as an 84 port multi-PHY. The PHY-ID of each cell is identified using in-band addressing.
- Any-PHY receive slave appears as a single device. The PHY-ID of each cell is identified using in-band addressing.
- UTOPIA L2 transmit and receive slave appears as a 31-port multi-PHY.
- UTOPIA L2 receive slave can also appear as a single port with the logical port provided as a prepend.

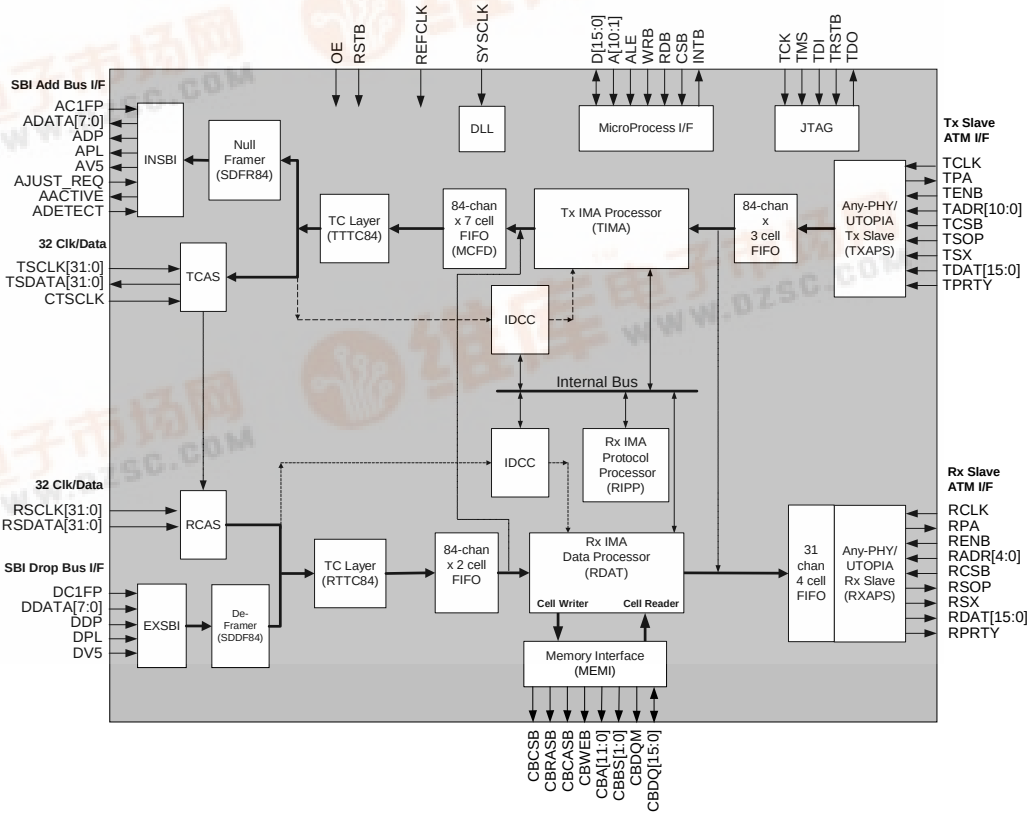
### LOOPBACK AND DIAGNOSTICS

- Supports UTOPIA Side Loopback.
- Supports Line Side Loopback.
- Supports per group ICP cell trace capability.

### SOFTWARE

- The S/UNI-IMA device driver, written in ANSI C, provides a well-defined API and low level utility functions for diagnostics and debugging purposes
- Software wrappers are used for RTOS-related functions making the S/UNI-IMA device driver portable to any Real Time Operating System (RTOS) environment.

## BLOCK DIAGRAM



# *Preliminary* PM7341 S/UNI®-IMA-84

## 84 Link Inverse Multiplexer for ATM (IMA) / UNI PHY

### *GENERAL*

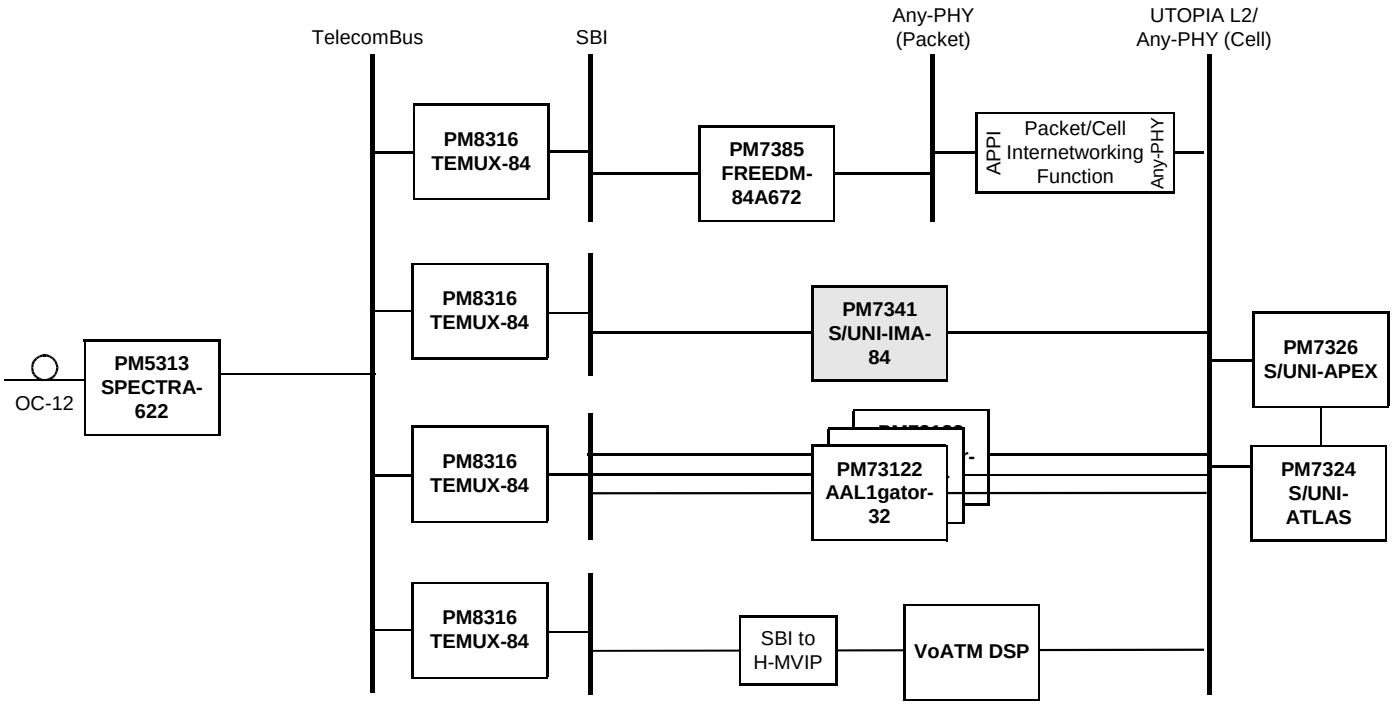
- 16-bit interface for 1M x 16 or 4M x 16 SDRAM, depending on the differential delay tolerance.
- Provides a 16-bit microprocessor interface for configuration, statistics gathering and Link and Unit Management.
- Provides a standard 5-pin P1149 JTAG port.
- Low-power 1.8 V CMOS with TTL-compatible I/O.
- 416-pin plastic ball grid array (PBGA) package.

## APPLICATIONS

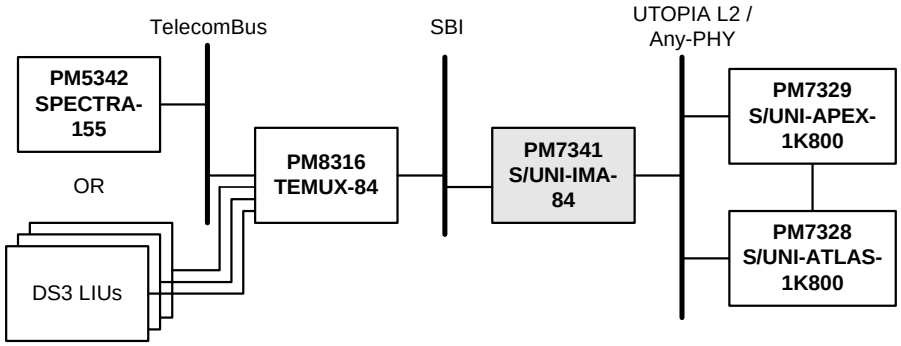
- Multiservice Switches.
- Optical Access Switches.
- Wireless Basestation Controllers.

## TYPICAL APPLICATIONS

### *ATM MULTISERVICE SWITCH*




### *WIRELESS BASESTATION CONTROLLER*





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