PM4354

COMET-QUAD

REVISION A DEVICE ERRATA

PRELIMINARY

ISSUE 2: SEPTEMBER 2000

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	April 2000	Document Created
2	June 2000	Updated Document. Sections 2.2, 2.3, 2.4, 2.6, 3.2 and 3.3 were added
3	Sept 2000	Updated Section 2.6.1 and 2.6.4. Added Sections 3.4 and 3.5.

CONTENTS

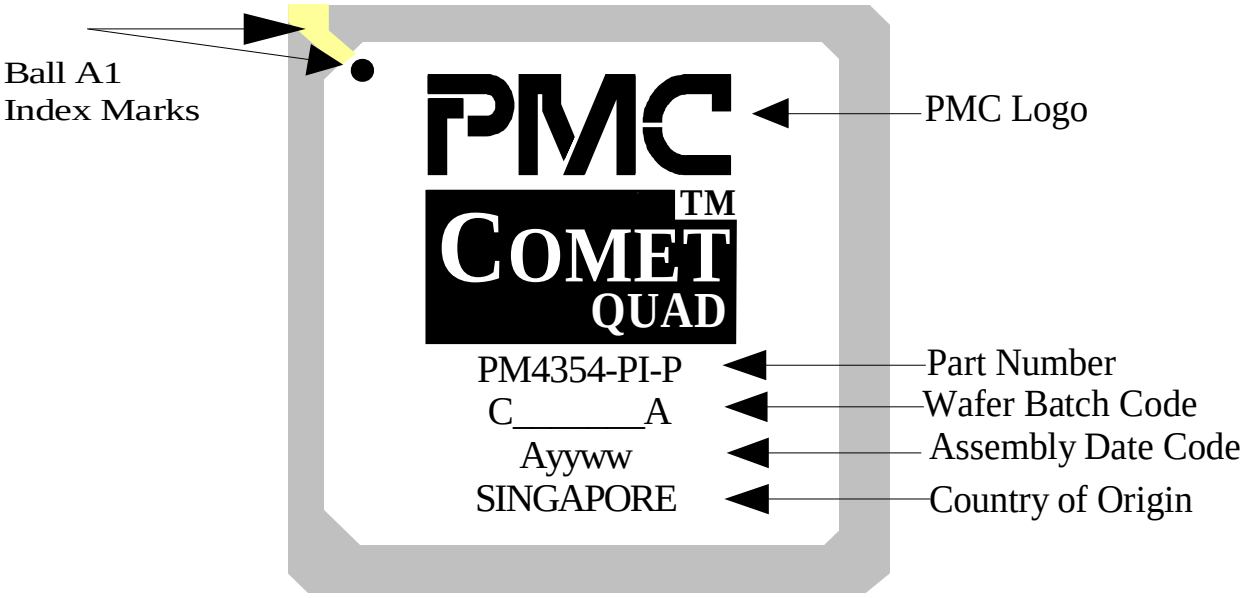
1 INTRODUCTION

In this document, Section 2 lists the known functional errata for revision A of PM4354 COMET-QUAD and Section 3 lists the documentation errors found in Issue 4 of the PM4354 COMET-QUAD Long Form Data Sheet (PMC-1990315).

1.1 Device Identification

The information contained in the Errata relates to Revision A of PM4354 COMET-QUAD only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1).

Figure 1 - PM4354 COMET-QUAD Branding Format.



1.2 Reference

- PMC-1990315, COMET-QUAD Long Form Data Sheet, Issue 4

2 COMET-QUAD REVISION A FUNCTIONAL DEFICIENCY LIST

This section lists the known functional deficiencies for Revision A of COMET-QUAD (as of the publication date of this document). For each deficiency, the known work-around and the operating constraints, with and without the work-around, are also described.

Please report any functional deficiencies not covered in this document to PMC-Sierra.

2.1 Transmit pulse template may not be met.

2.1.1 Description:

This item will be corrected in COMET-QUAD Rev. B.

COMET-QUAD Revision A prototype parts will produce analog transmit pulses between 4 Vpp to 6.8 Vpp. The devices have not been trimmed to ensure compliance to the shorthaul/longhaul T1 pulse templates specified in ANSI T1.102, ANSI T1.403 and the E1 pulse templates specified in G.703.

The next revision of the PM4354 COMET_QUAD will be trimmed to meet the T1 and E1 pulse templates over all specified temperature and voltage conditions.

2.1.2 Workarounds:

None

2.1.3 Performance with workaround:

N/A

2.1.4 Performance without workaround:

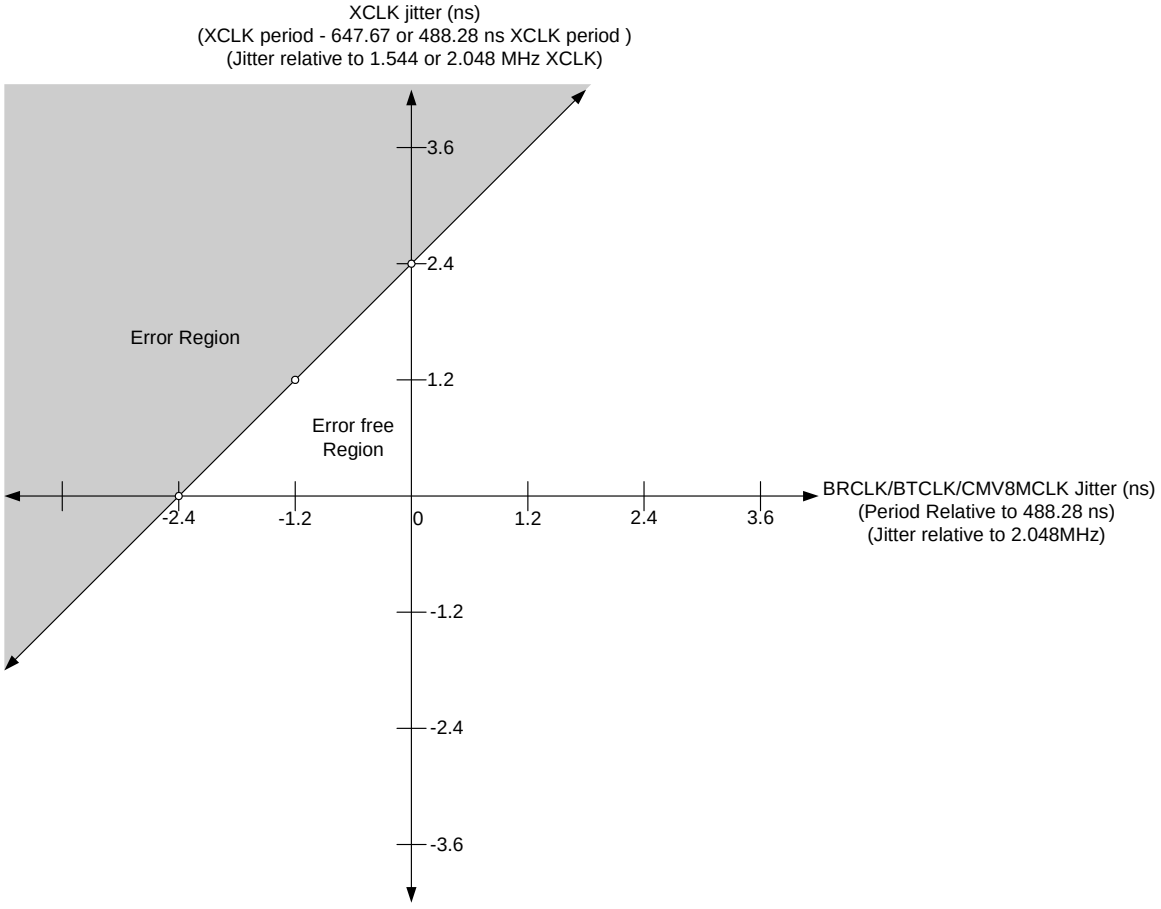
Testing to standard pulse masks may result in failure to meet pulse template amplitude.

2.2 T1 mode with a 2.048 MHz or greater backplane slave clock

2.2.1 Description:

This item will be corrected in COMET-QUAD Rev. B.

When the COMET-QUAD is configured for T1 mode with a slaved clock backplane (BRCLK[x], BTCLK[x] or CMV8MCLK (H-MVIP) are inputs) with a 2.048 MHz or greater backplane rate, the data and signaling information may be corrupted if the BRCLK[x], BTCLK[x], CMV8MCLK and XCLK jitter (defined as instantaneous worse case period) is not tightly controlled. The following diagram shows the error and error-free operating regions when in the presence BRCLK/BTCLK/CMV8MCLK and XCLK jitter.



The BRCLK/BTCLK/CMV8MCLK jitter is described as the worst case instantaneous peak jitter relative to a jitter-free BRCLK/BTCLK/CMV8MCLK. The XCLK jitter is described as the worst case instantaneous peak jitter relative to a jitter-free XCLK. The jitter for both XCLK and BRCLK/BTCLK/CMV8MCLK are described as positive and negative peak jitter in nanoseconds (ns). Positive peak jitter increases the instantaneous period while negative peak jitter shortens the instantaneous period.

When the COMET-QUAD is a backplane clock slave, BRCLK[x], BTCLK[x] and CMV8MCLK are inputs. BRCLK[x] and BTCLK[x] can be 1.544, 2.048, 3.088, or 4.096 MHz. When at 3.088 or 4.096MHz, the clocks are internally divided down by a factor of two. CMV8MCLK is internally divided down to 2.048MHz. The above diagram represents the internally divided down clocks.

2.2.2 Workarounds:

Proper operation is ensured when the worst case instantaneous XCLK jitter minus the worst case instantaneous BRCLK/BTCLK/CMV8MCLK jitter is less than 2.4ns through all valid voltage and temperature ranges (XCLK jitter – BRCLK/BTCLK/CMV8MCLK jitter < 2.4). The following are example configurations that allow the COMET-QUAD to operate error free.

Instantaneous XCLK			Instantaneous BRCLK/BTCLK/CMV8MCLK Range for proper T1 operation		
Frequency[1] (MHz)	Period (ns)	Jitter[2] (ns)	Frequency[3] (MHz)	Allowable Jitter (ns)	Allowable period (ns)
1.544	647.67	+0.6	1.544	> -100	>547.67
1.544	647.67	+0.6	2.048	> -1.8	>486.48
1.544	647.67	-0.6	2.048	> -3	>485.28
2.048	488.28	+0.6	1.544	> -100	>547.67
2.048	488.28	+0.6	2.048	> -1.8	>486.48
2.048	488.28	-0.6	2.048	> -3	>485.28

Notes:
1. The impact of XCLK jitter is relative to 1.544 or 2.048 MHz.
2. Worse case jitter is the sum of the worst case instantaneous jitter plus the worst case parts per million (ppm) drift from the exact 1.544 or 2.048 MHz XCLK.
3. These examples show that clock jitter is not a significant concern with 1.544 MHz backplane.

2.2.3 Performance with workaround:

Proper operation is ensured.

2.2.4 Performance without workaround:

Data and signaling information may be corrupted.

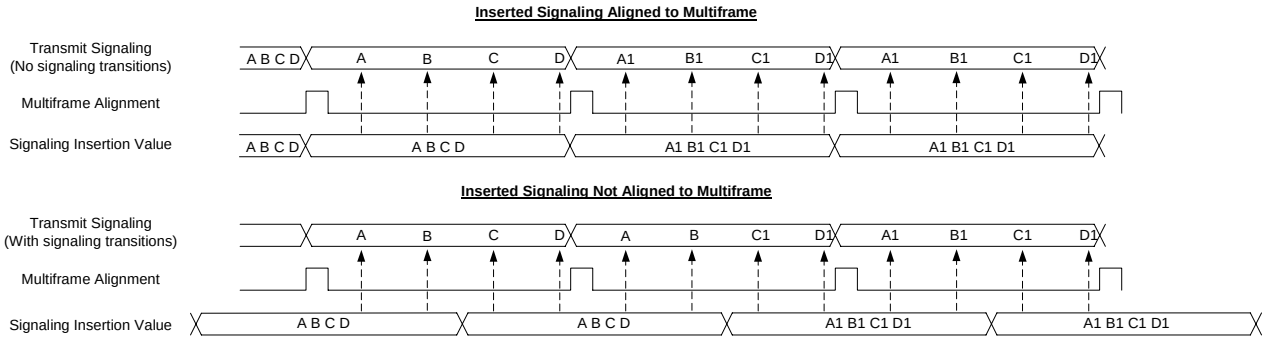
2.3 Signaling insertion

2.3.1 Description:

This item will be corrected in COMET-QUAD Rev. B for the BTSIG signaling stream.

Signaling insertion could have a transitional state when the signaling state changes.

T1 signaling on the COMET-QUAD is inserted relative to the multiframe alignment of the transmitted T1 signal. Signaling data is extracted bit by bit from the TPSC indirect register or the BTSIG pins. This means that each of the signaling bits (A, B for SF and A, B, C, and D for ESF) is taken from a different frame relative to the multiframe boundary. If the signaling data on the BTSIG pin (or the TPSC Indirect register) is used to insert signaling, but is not aligned to the multiframe boundary, then transitional signaling states might occur. Signaling data could change from the current signaling state to an intermediate signaling state (for 3ms or one multiframe) before changing to the correct signaling state, as shown below.



2.3.2 Workarounds:

When the transmit backplane is configured for basic frame mode, the COMET-QUAD assumes an arbitrary multiframe alignment. When configured for basic frame alignment, there is no way to align to the internal multiframe. Therefore transitional states for signaling might occur. Hence, it is necessary to configure the backplane for multiframe alignment to ensure signaling insertion occurs without transitional states.

2.3.3 Performance with workaround:

Signaling insertion via BTSIG[x] occurs without transitional states.

2.3.4 Performance without workaround:

Transitional states for signaling might occur.

2.4 FPTYP Bit Description

2.4.1 Description:

This item will be corrected in COMET-QUAD Rev. B.

The FPTYP bit in the Register 041H, 141H, 241H, 341H: BTIF Frame Pulse Configuration has limited functionality and the bit description is incorrectly stated.

In the Issue 4 Datasheet, the FPTYP description incorrectly reads, “When operating at T1 in 2MHz backplane mode, the framing pattern can be corrupted when FPTYP =1. In order to avoid corruption, toggle FPTYP high then low and keep it held low. The transmitter will maintain the multi-frame alignment provided on the BTFP. If BTFP loses multiframe alignment, FPTYP will have to be toggled again.”

2.4.2 Workarounds:

The following description corrects the description of the FPTYP bit:

“The COMET-QUAD will not operate correctly when the backplane is configured for T1 ESF mode with 2.048Mbit/s or greater backplane with master multiframe pulse (FMODE = 0 and FPTYP = 1). Slave mode (FMODE =1) should be used.

When operating at T1 ESF in 2.048 Mbit/s or greater backplane mode with slave multiframe pulse (FMODE =1), the framing pattern can be corrupted when FPTYP =1. In order to avoid corruption, toggle FPTYP high and then low within 2ms (16 frames) after the last BTFP active edge. Then keep FPTYP held low. This allows the COMET-QUAD’s internal multiframe alignment to synchronize with the BTFP multiframe pulse input. The transmitter will maintain the last multi-frame alignment captured from the BTFP input. If BTFP loses multiframe alignment, FPTYP will have to be toggled again.”

Failure to implement the corrected workaround stated above results in the transmitted multiframe boundary to be different than that indicated by the BTFP input. This could cause signaling transitional state corruption (as discussed in Errata item 2.3) and, Facility Data Link, CRC and F-bit misalignment when framing and signaling is taken from backplane data (BTPCM). The Facility Data Link, CRC and F-bit will not be misaligned when generated internally by the COMET-QUAD.

2.4.3 Performance with workaround:

Multiframe boundary will be correctly indicated by the BTFP input.

2.4.4 Performance without workaround:

The transmitted multiframe boundary may be different than that indicated from the BTFP input.

2.5 Analog Vdd power supply below 3.3 volts may affect pulse template

2.5.1 Description:

This item will be corrected in COMET-QUAD Rev. B.

If the analog Vdd power supply drops below 3.3 volts, the analog transmit pulse shape amplitude could decrease for the COMET-QUAD Revison A prototype parts.

2.5.2 Workarounds:

Keep the analog Vdd power supply between 3.3V to 3.3V + 5%.

2.5.3 Performance with workaround:

Transmit analog pulse amplitude will not be sensitive to analog Vdd.

2.5.4 Performance without workaround:

Transmit analog pulse shape amplitude may decrease.

2.6 Long Haul Equalization

2.6.1 Description:

This item will be corrected in COMET-QUAD Rev. B.

The COMET-QUAD Rev A prototype parts were tested to recover signals from 0 to 24dB of cable attenuation (long haul). Some COMET-QUAD Rev A devices may not be able to recover line signals beyond 15dB of cable attenuation.

2.6.2 Workarounds:

None

2.6.3 Performance with workarounds

N/A

2.6.4 Performance without workarounds

Using the COMET-QUAD Rev A prototype devices with long cables lengths that have larger than 15dB of cable attenuation could result in failure to recover signal from the line.

3 DOCUMENTATION ERRORS

This section lists the known documentation errors in Issue 4 of PMC-1990315 COMET-QUAD Datasheet.

Please report any documentation errors not covered in this document to PMC-Sierra.

3.1 Payload Loopback Description

3.1.1 Description:

The PAYLD bit description in the Master Diagnostic register (0x00A, 0x10A, 0x20A and 0x30A) should be changed to correctly describe the operation of the bit.

The following statement,

"During payload loopback, the data on BRPCM[x] is only valid when the quadrant is configured as a BRCLK[x] master, BRFP[x] master and the RX-ELST is bypassed. In all other modes, the BRPCM[x] or MVBRD output of the quadrant is forced to all-ones."

should be changed to,

"During payload loopback, the data on BRPCM[x] is only valid when the quadrant is configured as a BRCLK[x] master, BRFP[x] master and the RX-ELST is bypassed. When the RX-ELST is not bypassed, then the BRPCM[x] or MVBRD output of the quadrant is forced to all-ones."

3.2 TCCSEN Register Bit Description

3.2.1 Description:

The TCCSEN bit description in the Transmit H-MVIP/CCS Enable and Configuration register (0x0B9) should be changed to correctly describe the operation of the bit.

The following statement,

"In T1 mode, CCS is inserted into either timeslot 23 or timeslot 31, as determined by the MAP bit of the BTIF Frame Pulse Configuration Register. When MAP is

logic 0, CCS is inserted into timeslot 31. When MAP is a logic 1, CCS is inserted into timeslot 23."

should be changed to,

"In T1 mode CCS is inserted into timeslot 31."

3.3 CTCLK Pin Description

3.3.1 Description:

The CTCLK pin description in the Pin description section of the data sheet should be changed to correctly describe the operation of the pin.

The following statement,

"Depending on the configuration of the COMET-QUAD, CTCLK may be a 12.352 MHz or 16.384 MHz clock (so the transmit clock is generated by dividing CTCLK by 8), or a line rate clock (so the transmit clock is generated directly from CTCLK, or from CTCLK after jitter attenuation), or a multiple of 8kHz (Nx8khz, where $1 \leq N \leq 256$) so long as CTCLK is jitter-free when divided down to 8kHz (in which case the transmit clock is derived by the JAT PLL using CTCLK as a reference)."

should be changed to,

"CTCLK may be any multiple of 8 kHz (N x 8 kHz, where $1 \leq N \leq 256$) so long as CTCLK has low jitter when divided down to 8 kHz. CTCLK is optionally jitter attenuated by the transmit jitter attenuation block (TJAT). When CTCLK jitter attenuation is enabled, the CTCLK frequency should be programmed into the TJAT Jitter Attenuation Divider N1 Control register."

3.4 Thermal Information

3.4.1 Description:

The Ordering and Thermal Information section of the data sheet should be changed to correctly describe the COMET-QUAD thermal information. Also, a graph of Theta J-A with respect to Forced Air, should be added.

The following description,

Table 112: - Thermal Information

				Forced Air (Linear Feet per Minute)				
Part No.	**Case Temperature**	**Theta J-A at 1.43 Watts**	**Conv**	**100**	**200**	**300**	**400**	**500**
PM4354-PI	-40°C to 85°C	Dense Board[1]	40.3	36.0	32.9	30.9	29.5	28.6
		JEDEC Board[2]	22.9	21.2	20.0	19.2	18.7	18.2

1. - Dense Board is defined as a 3S3P board and consists of a 3x3 array of PM4354-PI devices located as close to each other as board design rules allow. All PM4354-PI devices are assumed to be dissipating 1.43 Watts. Theta J-A listed is for the device in the middle of the array.

2. - JEDEC Board Theta J-A is the measured value for a single thermal device in the same package on a 2S2P board following EIA/JESD 51-3.

should be changed to,

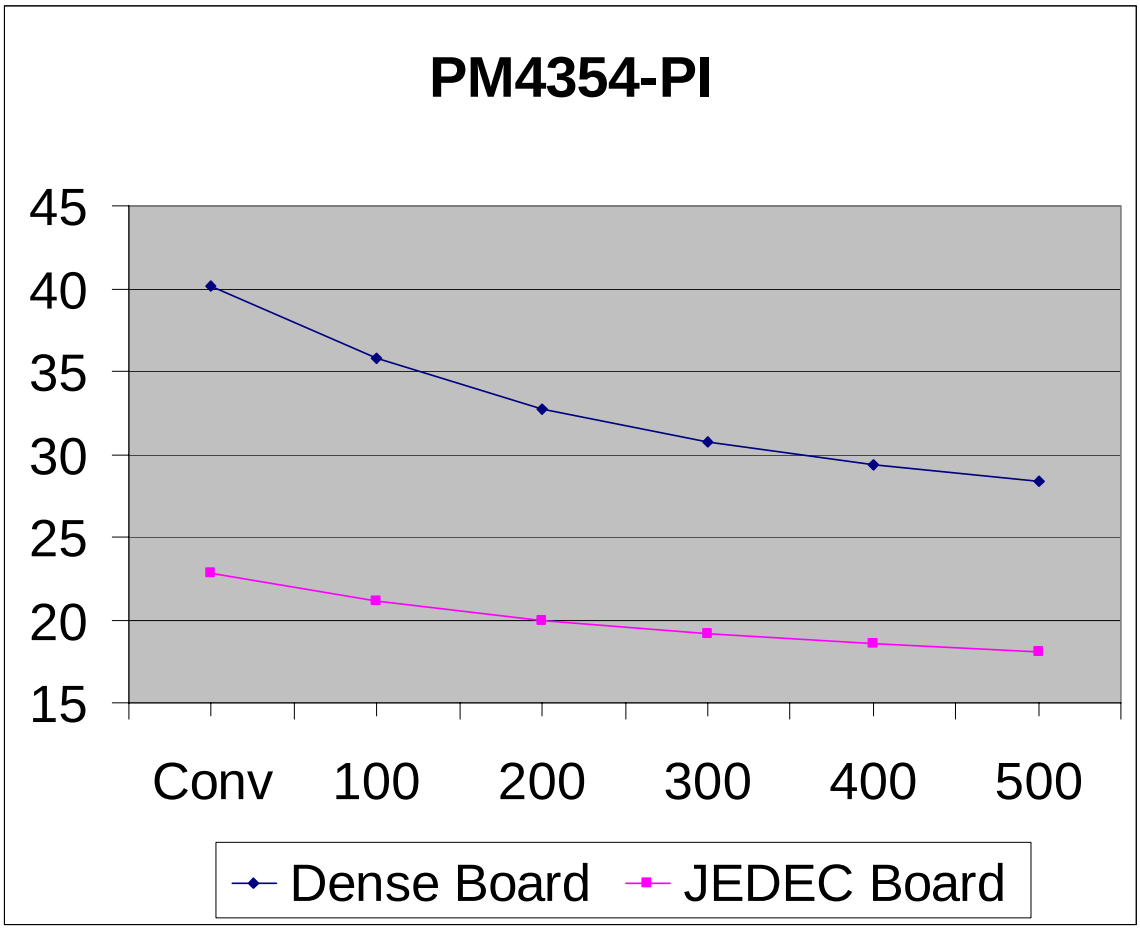
Table 112: - Thermal Information

				Forced Air (Linear Feet per Minute)				
Part No.	**Case Temperature**	**Theta J-A at 1.57 Watts**	**Conv**	**100**	**200**	**300**	**400**	**500**
PM4354-PI	-40°C to 85°C	Dense Board[1]	40.2	35.8	32.8	30.7	29.4	28.4
		JEDEC Board[2]	22.8	21.1	19.9	19.1	18.5	18.1

1. - Dense Board is defined as a 3S3P board and consists of a 3x3 array of PM4354-PI devices located as close to each other as board design rules allow. All PM4354-PI devices are assumed to be dissipating 1.57 Watts. Theta J-A listed is for the device in the middle of the array.

2. - JEDEC Board Theta J-A is the measured value for a single thermal device in the same package on a 2S2P board following EIA/JESD 51-3.

3. – For long-term reliability, it is recommended that the junction temperature should remain below 105 degrees Celsius.



3.5 D.C. Characteristics

3.5.1 Description:

The D.C. Characteristics section of the data sheet should be changed to add an additional row to the bottom of Table 100. The addition states the thermal power dissipation of the COMET-QUAD.

The additional row at the bottom of the table should read as follows

Table 100: - D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
PDISS	Thermal Power Dissipation		1.57		Watts	$V_{DDall33}$ = 3.465 V, VDDC25 = 2.7, 85°C case temperature, T1 mode, transmitting 50% ones density, short haul 550-660 ft, digital outputs unloaded.

CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
(604) 415-4533
Web Site: http://www.pmc-sierra.com