ATM Layer Cell Routing Control, Monitoring, and Policing 800 Mbit/s

FEATURES

- Monolithic single-chip device which handles ATM switch ingress VPI/VCI address translation, cell appending, cell rate policing, counting, and OAM requirements for 65,536 Virtual Circuits (VCs).
- Instantaneous transfer rate of 800 Mbit/s supports a cell transfer rate of 1.42 x 10^6 cells/s.
- 8- or16-bit PHY interface using direct addressing for up to four PHYs (UTOPIA Level 1) and Multi-PHY addressing for up to 32 PHYs (UTOPIA Level 2).
- 8- or 16-bit SCI-PHY™+ (53 -64 byte extended ATM cell with prepend/ postpend) interface at output to switch fabric.
- Compatible with wide range of switching fabrics and traffic management architectures including per-VC or per-PHY queuing.
- Provides identification/tagging of RM cells to support adjunct processing applications such as Virtual Source/ Virtual Destination (VS/VD) Available Bit Rate (ABR) service.
- Supports logical multicast.
- Extremely flexible CAM-type cell identification that uses arbitrary VPI/ VCI values and/or appended bytes for identification.
- Drops on command all low priority (CLP=1) cells to relieve switch congestion.
- Includes 16-bit FIFO buffered microprocessor bus interface for cell extraction and insertion (including OAM), VC table access, control and status monitoring, and configuration of the IC.
- Supports DMA access for cell extraction and insertion.
- Low power, 0.6 micron, +5 V CMOS technology.
- 240 copper slugged Plastic Quad Flat Pack (PQFP) package.

POLICING

- Policing performed for adherence to: Peak Cell Rate (PCR), Sustained Cell Rate (SCR), and Burst Tolerance (BT). Violating cells can be noted, dropped, or have Cell Loss Priority (CLP) bits set to 1.
- Policing done according to the Virtual Scheduling Algorithm (equivalent to Continuous-State Leaky Bucket Algorithm).
- Two instantiations of policing per VC.

CELL COUNTING

- Per-VC counts maintained for low priority cells, high priority cells, cells discarded due to policing/congestion, and cells with a reduced priority.
- Per-VC performance monitoring counts maintained include: lost cells, misinserted cells, BIP-16 errors, and Severely Errored Cell Blocks (SECB).
- Generates backwards reporting cells.
- Per-device counts maintained include: total cells input, total cells output, OAM cells, cells discarded due to congestion, corrupted OAM cells, and unassigned/invalid VPI/VCIs.

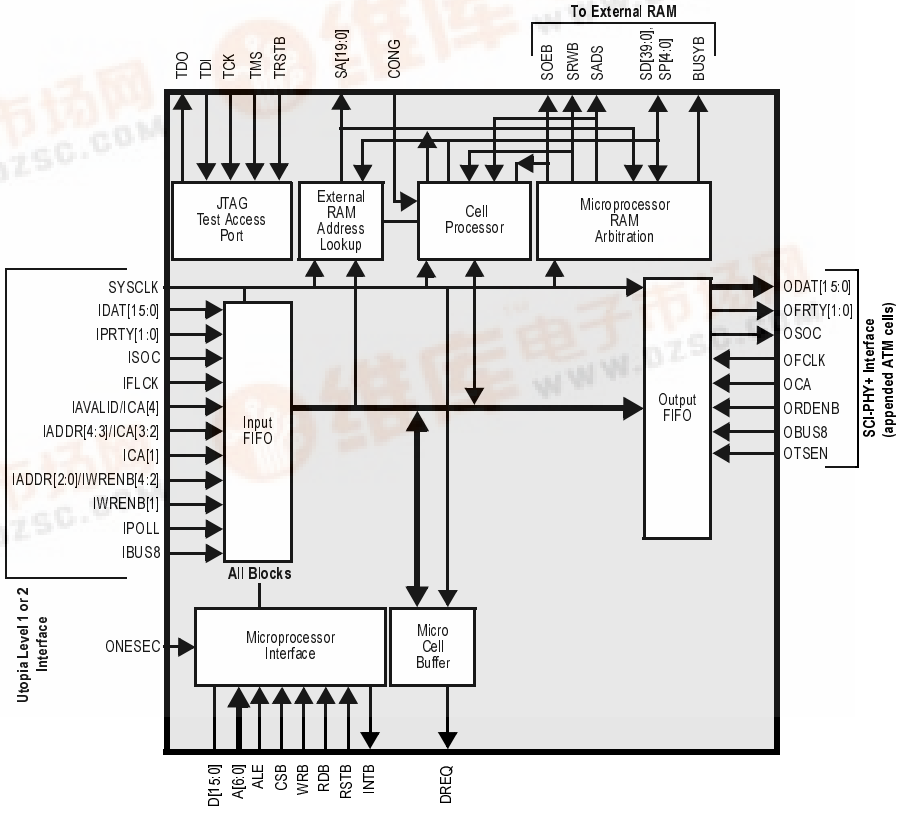
OAM HANDLING AND PERFORMANCE MONITORING

- VC OAM performance monitoring per ITU Recommendation I.610, Bellcore TR-1248, and Bellcore GR-1113-CORE.
- Automatic OAM handling includes: reception and generation of AIS and RDI cells.
- OAM cell identification/tagging provided to enable direct extraction by egress device, eliminating delays through switch core.
- Incoming OAM cells are terminated, passed to device output or microprocessor.
- Outgoing OAM cells sourced from automatic OAM generating circuitry, device input, or microprocessor.

APPLICATIONS

- ATM Hubs and Workgroup Switches
- ATM Enterprise and Edge Switches

BLOCK DIAGRAM



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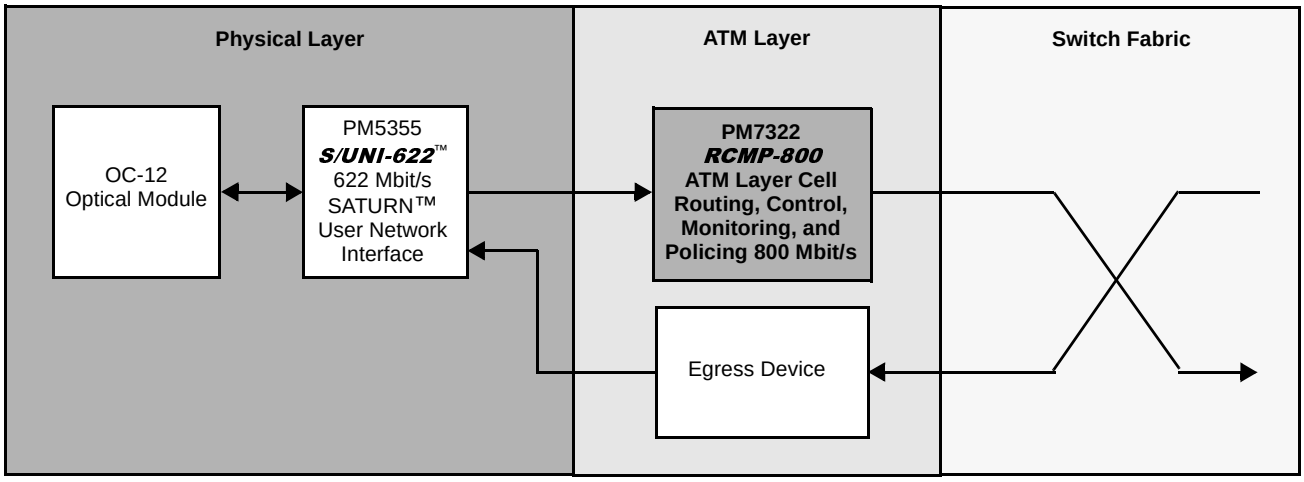
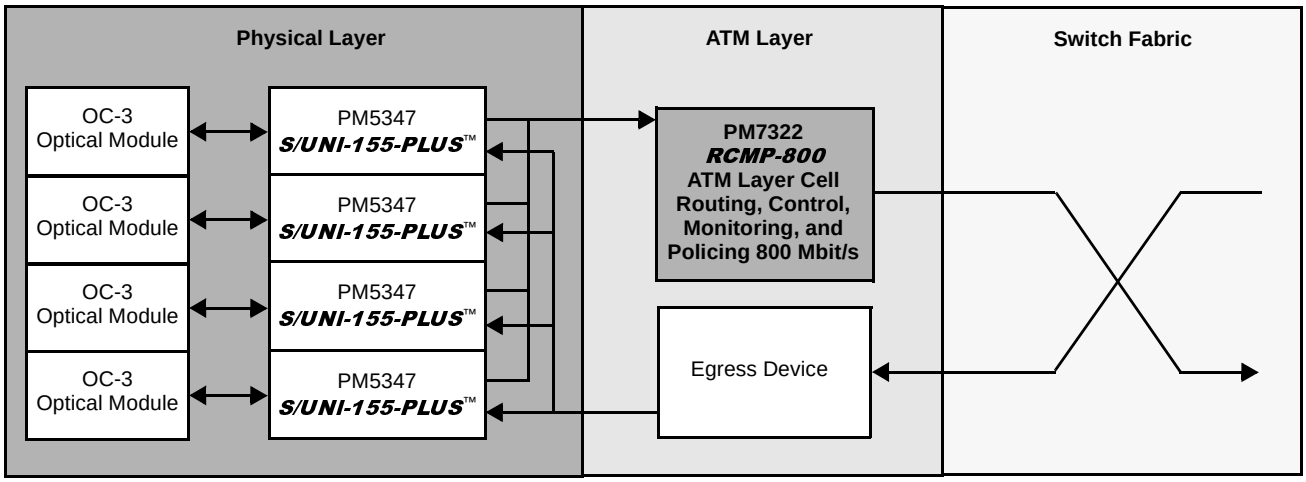
TYPICAL APPLICATIONS

SINGLE-PHY OC-12/STM-4 (622 Mbit/s) SWITCH PORT



MULTI-PHY OC-3/STM-1 (155 Mbit/s) SWITCH PORT



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PMC-941029 (R5)

September, 1998