

# UP01878

## Silicon N-channel MOSFET

For switching

### ■ Features

- Two elements incorporated into one package
- Reduction of the mounting area and assembly cost by one half

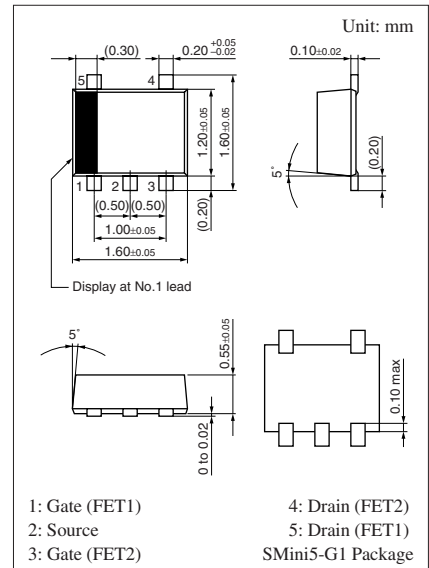
### ■ Basic Part Number of Element

- 2SK3539 × 2 elements

### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

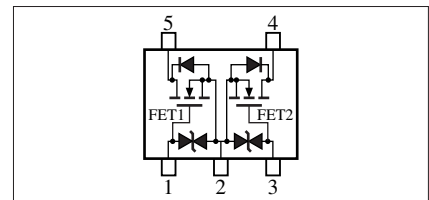
Parameter		Symbol	Rating	Unit
Rating of element	Drain to source voltage	$V_{DSS}$	50	V
	Gate to source voltage	$V_{GSO}$	$\pm 7$	V
	Drain current	$I_D$	100	mA
	Max drain current	$I_{DP}$	200	mA
Overall	Allowable power dissipation *	$P_D$	125	mW
	Channel temperature	$T_{ch}$	125	$^\circ\text{C}$
	Storage temperature	$T_{stg}$	-55 to +125	$^\circ\text{C}$

Note) \*: Total power dissipation



Marking Symbol: AL

Internal Connection

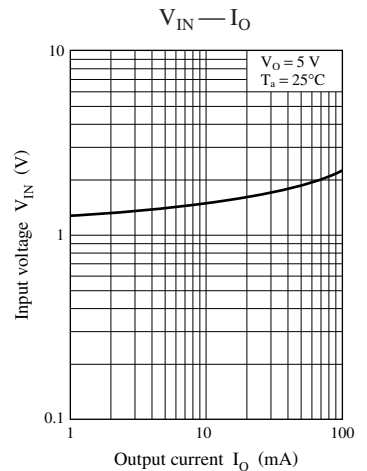
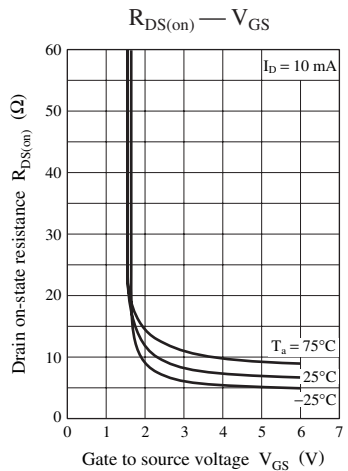
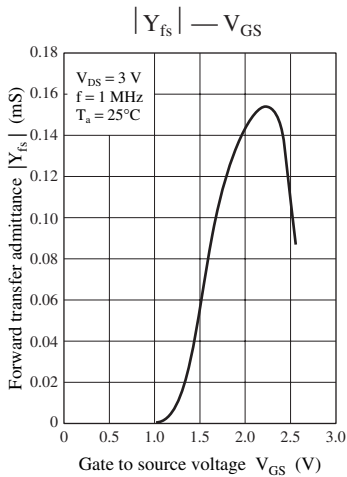
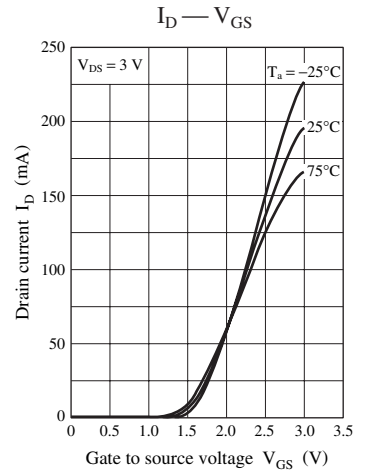
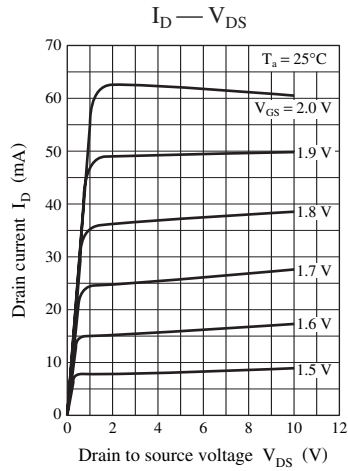
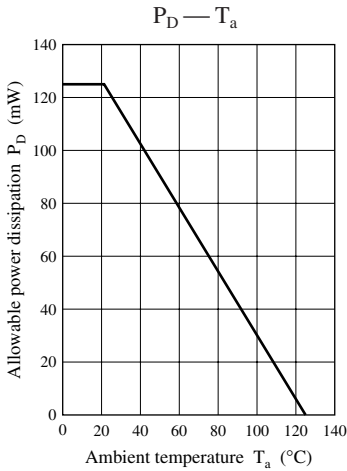
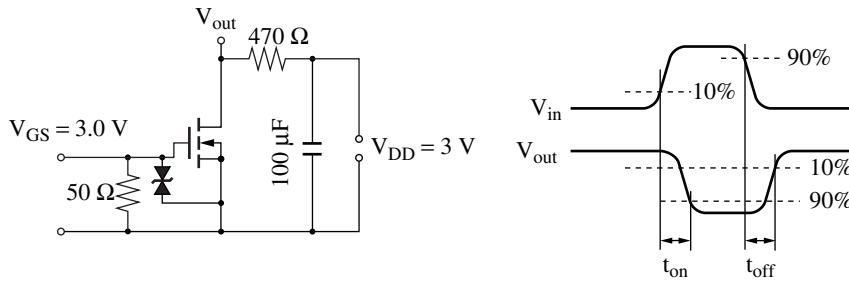


### ■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain to source voltage	$V_{DSS}$	$I_D = 10 \mu\text{A}, V_{GS} = 0$	50			V
Drain cut-off current	$I_{DSS}$	$V_{DS} = 50 \text{ V}, V_{GS} = 0$			1.0	$\mu\text{A}$
Gate cut-off current	$I_{GSS}$	$V_{GS} = \pm 7 \text{ V}, V_{DS} = 0$			$\pm 5$	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$I_D = 1 \mu\text{A}, V_{DS} = 3 \text{ V}$	0.9	1.2	1.5	V
Drain on-state resistance	$R_{DS(on)}$	$I_D = 10 \text{ mA}, V_{GS} = 2.5 \text{ V}$		8	15	$\Omega$
		$I_D = 10 \text{ mA}, V_{GS} = 4.0 \text{ V}$		6	12	
Forward transfer admittance	$ Y_{fs} $	$I_D = 10 \text{ mA}, V_{DS} = 4.0 \text{ V}$	20	60		mS
Input capacitance	$C_{iss}$	$V_{DS} = 3 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		12		pF
Output capacitance	$C_{oss}$			7		pF
Reverse transfer capacitance	$C_{rss}$			3		pF
Turn-on time *	$t_{on}$	$V_{DD} = 3 \text{ V}, V_{GS} = 0 \text{ V to } 3 \text{ V}, R_L = 470 \Omega$		200		ns
Turn-off time *	$t_{off}$	$V_{DD} = 3 \text{ V}, V_{GS} = 3 \text{ V to } 0 \text{ V}, R_L = 470 \Omega$		200		ns

Note) \*: Refer to  $t_{on}, t_{off}$  test circuit (next page)

$t_{on}, t_{off}$  Test circuit



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