Technical Brief

OKI ASIC PRODUCTS

W712
Universal Serial Bus Controller
0.5µm Technology
Mega Macrofunction

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Oki Semiconductor

Contents

Oki Semiconductor

W712 USB Device Controller

0.5μm Technology Mega Macrofunction

DESCRIPTION

The Universal Serial Bus (USB) Device Controller Mega Macrofunction is a featured element in Oki's 0.5μm Sea of Gates (SOG) and Customer Structured Array (CSA) families. Oki's USB mega macrofunction provides a USB interface, control/status block, FIFO control, and application interface in two highly integrated submodules for system design interfaces based on the USB protocol. The submodule partitioning allows custom configurations to be easily developed. The USB mega macrofunction connects an industry standard USB interface with a microprocessor-style parallel application interface. This straightforward interface permits easy integration of the USB mega macrofunction to the target application. Using Oki's USB mega macrofunction, designers can reduce development time, risk, and introduce their USB based products to market faster. Oki's W712 USB Device Controller mega macrofunction provides a complete USB device interface solution and is fully compliant with the Universal Serial Bus 1.0 specification. For more details on the Universal Serial Bus 1.0 specification, refer to www.usb.org.

FEATURES

- USB 1.0 compliant
- Full-speed (12 Mb/sec) and low-speed (1.5 Mb/sec) support
- Microprocessor-style parallel application interface
- Supports isochronous, control, interrupt and bulk transfers
- Supports four transmit FIFO's
  - Three 64 byte
  - One 2 Kbyte (2-level)
- Supports four receive FIFO's
  - Three 64 byte
  - One 2 Kbyte (2-level)
- Supports one control endpoint and six additional endpoint addresses
- Expandable up to 32 endpoint addresses
- Customizable to specific application requirements

Supported ASIC Families

Family Name	Family Type
MSM13R0000	Sea of Gates
MSM98R000	Customer Structured Array

Recommended Operating Conditions (V_{SS} = 0 V)

Parameter	Symbol	Min.	Typ.	Max	Unit
Power supply voltage	V_{DD}	2.7	3.3	3.6	V
Operating temperature	T_j	-40	+25	+85	° C

Mega Macrofunction Characteristics

Mega Macrofunction	Description	Logic Gate Count	Logic Pin Count
W712	USB Device Controller	15797	139

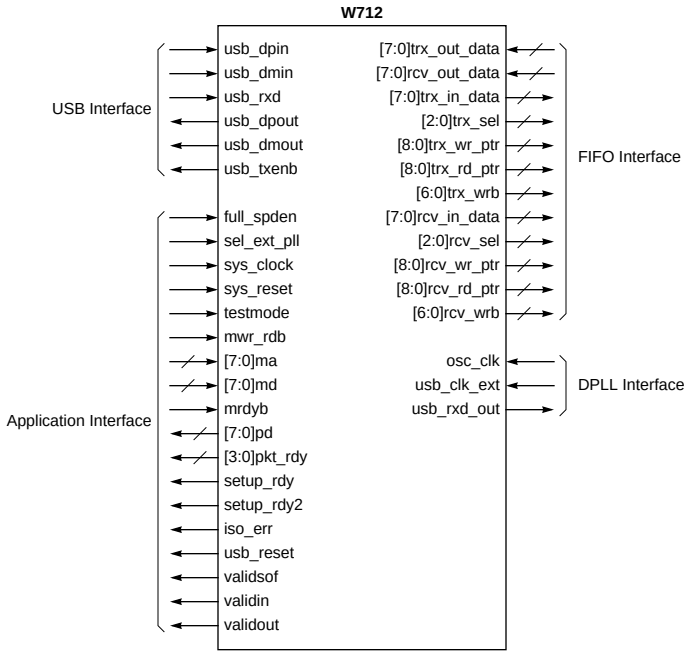

Figure 1. Logic Symbol

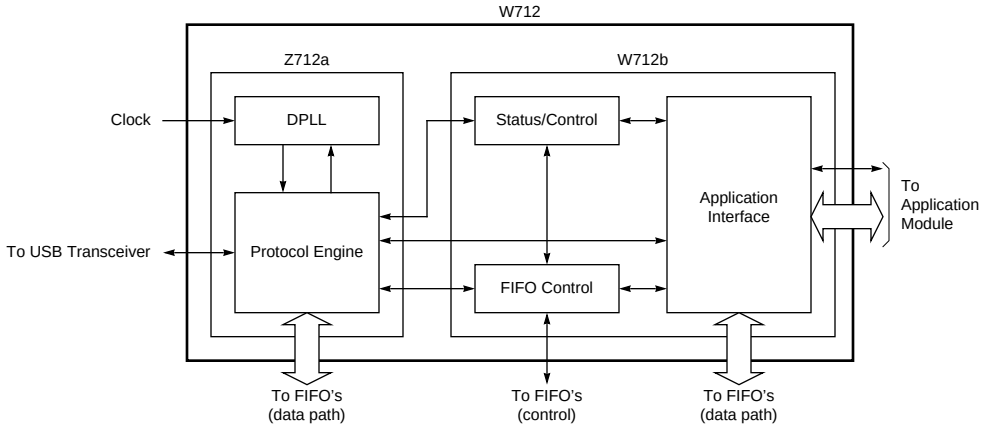

Figure 2. W712 Block Diagram

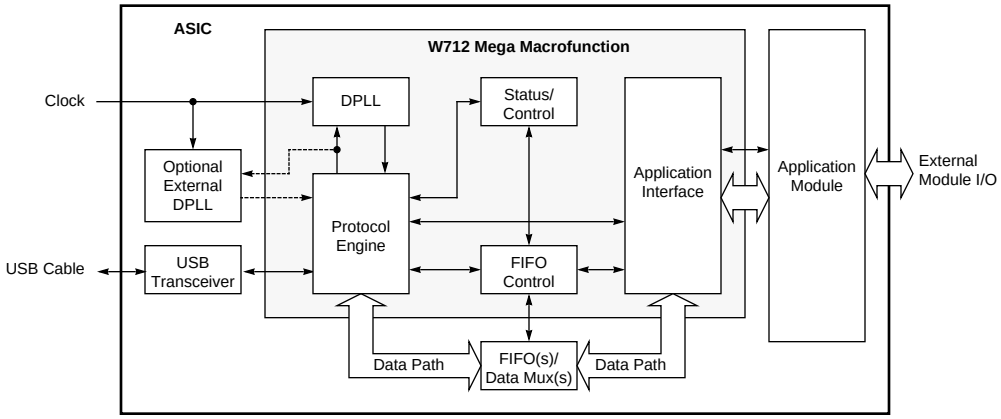

Figure 3. Example USB Mega Macrofunction Application

SIGNAL DESCRIPTIONS

USB Interface

<table>
<tr><th>Signal</th><th>Type</th><th>Assertion</th><th>Description</th></tr>
<tr><td>usb_dpin</td><td>Input</td><td>—</td><td>USB Data Plus In. This input and the usb_dmin input are the received single ended data from the USB transceiver. The table below shows values and results for these signals.
<table>
<tr><th>usb_dpin</th><th>usb_dmin</th><th>Result</th></tr>
<tr><td>0</td><td>0</td><td>SE0</td></tr>
<tr><td>0</td><td>1</td><td>Logic “0”</td></tr>
<tr><td>1</td><td>0</td><td>Logic “1”</td></tr>
<tr><td>1</td><td>1</td><td>Undefined</td></tr>
</table></td></tr>
<tr><td>usb_dmin</td><td>Input</td><td>—</td><td>USB Data Minus In. This input and the usb_dpin input are the received single ended data from the USB transceiver. See the table for the usb_dpin description, above, for values and results of these signals.</td></tr>
<tr><td>usb_dpout</td><td>Output</td><td>—</td><td>USB Data Plus Out. This output and the usb_dmout signal come from the USB transmit engine and drive the differential output buffers. The table below shows values and results for these signals.
<table>
<tr><th>usb_dpout</th><th>usb_dmout</th><th>Result</th></tr>
<tr><td>0</td><td>0</td><td>SE0</td></tr>
<tr><td>0</td><td>1</td><td>Logic “0”</td></tr>
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<tr><td>1</td><td>1</td><td>Undefined</td></tr>
</table></td></tr>
<tr><td>usb_dmout</td><td>Output</td><td>—</td><td>USB Data Minus Out. This output and the usb_dpout signal come from the USB transmit engine and drive the differential output buffers. See the signal description for usb_dpout, above, for a description of signal values and results.</td></tr>
<tr><td>usb_rxd</td><td>Input</td><td>—</td><td>USB Differential Received Data. This input comes from the USB differential receiver, and connects to the W712 mega macrofunction.</td></tr>
<tr><td>usb_txenb</td><td>Output</td><td>LOW</td><td>USB 3-State Output Enable. This signal connects to the transceiver EB input through an inverter gate. When the W712 mega macrofunction asserts this signal LOW, the transceiver transmits data on the USB bus. See Appendix for the USB transceiver Data Sheets.</td></tr>
</table>

Application Interface

Signal	Type	Assertion	Description
sys_clock	Input	—	**Clock**. Attach a 12-MHz clock signal to this input for full-speed operation and 1.5 MHz for low-speed operation.
sys_reset	Input	HIGH	**W712 Reset.** Asserting this signal HIGH resets the W712 mega macrofunction. The application module is required to assert this signal at power-on.
mwr_rdb	Input	—	**Write/Read Select.** When external application logic asserts this signal HIGH, the application is in WRITE mode. When asserted LOW, the application is in READ mode. External application logic asserts this signal HIGH when writing data to the transmit FIFOs or to the register files. External application logic asserts this signal LOW when reading data from the receiving FIFOs or from the register files. The register files contain information describing the function and transaction status.
usb_reset	Output	HIGH	**USB Reset**. This is the reset signal from the USB device controller.
[7:0]ma	Input	—	**Address Bus.** These eight inputs receive the address of the register files in the USB device controller.
[7:0]md	Input	—	**Input Data Bus.** These eight inputs receive the data to be stored in the register files or transmit FIFOs.
mrdyb	Input	LOW	**Data Strobe.** When asserted LOW and in WRITE mode, the data on the [7:0]md signal lines are valid for writing. When asserted LOW and in READ mode, the data on the [7:0]pd signals are valid for reading.
[7:0]pd	Output	—	**Output Data Bus**. These eight outputs transmit data received from either the register files or the receive FIFOs.
[3:0]pkt_rdy	Output	HIGH	**Packet Ready**. When the W712 asserts this signal, it indicates that one of the four receive FIFOs contains valid data. The application reads the data through the [7:0]pd bus.
full_spden	Input	—	**USB Full Speed Enable.** The application module sets this pin to “1” to select full-speed operation and “0” to select low-speed operation.
setup_rdy	Output	HIGH	**Setup Ready.** Asserting this signal HIGH indicates an 8-byte SETUP data has been received from the USB bus.
iso_err	Output	HIGH	**Isochronous Error.** Used for loopback testing or to indicate isochronous data has been received with DATA1 PID.
validsof	Output	HIGH	**Valid SOF**. This signal is asserted for two bit times, asynchronous to sys_clock, and indicates a valid SOF token is received when asserted HIGH.
sel_ext_pll	Input	HIGH	**Select External PLL**. Asserting this signal HIGH selects the external PLL option.
setup_rdy2	Output	HIGH	**Second Setup Ready**. Asserting this signal HIGH indicates a new 8-byte SETUP DATA has been received, while internally the device controller still sees the “setup_rdy” signal asserted. This signal will be asserted for two bit times, asynchronous to sys_clock.
testmode	Input	HIGH	**Testmode**. Asserting this signal invokes a loopback test mode.
validin	Output	HIGH	**Valid IN**. Asserted for two bit times, asynchronous to sys_clock, and indicates a valid IN token is received when asserted HIGH.
validout	Output	HIGH	**Valid OUT**. Asserted for two bit times, asynchronous to sys_clock, and indicates a valid OUT token is received when asserted HIGH.

FIFO Interface

Signal	Type	Assertion	Description
[7:0]trx_out_data	Input	—	**Transmit FIFO(s) data output**. Output data from the transmission RAM selected for reading.
[7:0]rcv_out_data	Input	—	**Receive FIFO(s) data output**. Output data from the receiving RAM selected for reading.
[7:0]trx_in_data	Output	—	**Transmit FIFO(s) data input**. Input data to all transmission RAMs.
[2:0]trx_sel	Output	HIGH	**Transmit FIFO(s) select**. Selects one of the seven transmission RAMs for reading.
[8:0]trx_wr_ptr	Output	—	**Transmit FIFO(s) write pointer**. Write address to all transmission RAMs.
[8:0]trx_rd_ptr	Output	—	**Transmit FIFO(s) read pointer**. Read address to all transmission RAMs.
[6:0]trx_wrb	Output	LOW	**Transmit FIFO(s) write strobe**. Write enable. One bit per transmission RAM.
[7:0]rcv_in_data	Output	—	**Receive FIFO(s) data input**. Input data to all receiving RAMs.
[2:0]rcv_sel	Output	HIGH	**Receive FIFO(s) select**. Selects one of the seven receiving RAMs for reading.
[8:0]rcv_wr_ptr	Output	—	**Receive FIFO(s) write pointer**. Write address to all receiving RAMs.
[8:0]rcv_rd_ptr	Output	—	**Receive FIFO(s) read pointer**. Read address to all receiving RAMs.
[6:0]rcv_wrb	Output	LOW	**Receive FIFO(s) write strobe**. Write enable. One bit per receiving RAM.

DPLL Interface

Signal	Type	Assertion	Description
osc_clk	Input	–	**Oscillator Clock**. Attach a 48 MHz clock signal for full-speed operation or a 6 MHz clock signal for low-speed operation.
usb_clk_ext	Input	–	**USB Clock External**. This is the output clock signal from an external DPLL. This clock should run at 12 MHz for full-speed operation or 1.5 MHz for low-speed operation. If an external DPLL is not used, this pin should be connected to VDD or GND.
usb_rxd_out	Output	–	**Synchronized USB Differential Received Data**. This signal comes from the USB differential receiver and is synchronized with the oscillator input. This signal connects to the external DPLL if it is used.

FUNCTIONAL DESCRIPTION

The W712 controller consists of two submodules, the Z712a hard macro, and the W712b soft macro, each containing multiple function blocks. The Z712a includes the Protocol Engine, DPLL, and Timer Blocks. The W712b includes the Status/Control, FIFO Control, Application Interface, Frame Timer Synthesizer, and remote wakeup blocks.

Protocol Engine

The Protocol Engine handles the USB communication protocol. It performs packet sequencing, signal generation/detection, CRC generation/checking, NRZI data encoding, bit-stuffing and packet ID (PID) generation/decoding.

DPLL

The Digital Phase Locked Loop extracts the clock and data from the USB differential received data.

Timer

The Timer block monitors idle time on the USB bus.

Status/Control

The Status/Control block uses transfer type and FIFO state information to manage the reception and transmission of USB data. It monitors the transaction status and communicates control events to the application via the Application Interface.

FIFO Control

The FIFO control block manages all FIFO operations for transmitting and receiving USB data sets. The W712 supports eight FIFOs (four transmit and four receive). They can be configured as described in the table below.

FIFO Configuration

FIFO Type	Endpoint Address	Programmable	Function
Transmit	0	64 bytes	Control Transfers
Transmit	5	64 bytes	Interrupt and Bulk Transfers
Transmit	6	64 bytes	Interrupt and Bulk Transfers
Transmit	7	2 Kbytes	Isochronous, Interrupt, and Bulk Transfers
Receive	0	64 bytes	Control Transfers
Receive	1	64 bytes	Bulk Transfers
Receive	2	64 bytes	Bulk Transfers
Receive	3	2 Kbytes	Isochronous and Bulk Transfers

Endpoints 3 and 7 are 2-level FIFOs which support up to two separate data sets of variable sizes. All FIFOs have flags that detect a full or empty FIFO and have the capability of re-transmitting or re-receiving the current data set.

Application Interface

The Application Interface uses an i486-like bus to interface between the customer's module and the W712. By using an i486-like bus protocol, the W712 can be easily integrated into any customer-designed module. The integration is limited only by the available gates and I/O pins in the array. The Customer Application Module may have its own external I/O, which do not interface with the W712. All application interface signals are unidirectional, and are either inputs or outputs of the W712.

Frame Timer Synthesizer

This block synthesizes the SOF signal in the event of a SOF token is lost.

Remote Wakeup

This block provides support for the remote wakeup function.

USB Transfers

The W712 supports all four transfer types defined by the USB specification. These are: Control, Isochronous, Interrupt, and Bulk.

- Control transfers must be supported by every peripheral for configuration, command and status information flow between the host and peripheral.
- Isochronous transfers provide guaranteed bus access and constant data rates for USB devices.
- Interrupt transfers support human input devices that need to communicate small amounts of data infrequently.
- Bulk transfers enable devices to transfer large amounts of data as bus bandwidth becomes available.

USB Interface

The W712 connects to the Universal Serial Bus via Oki's universal USB transceivers. The USB specific I/O converts the W712's internal unidirectional signals into compliant USB signals. The universal USB transceiver allows the designers' application module to interface with the physical layer of the Universal Serial Bus. It transmits and receives serial data at both full-speed (12Mb/s) and low-speed (1.5Mb/s) data rates. See Appendix for Oki's USB transceiver Data Sheets.

GLOSSARY

Term	Explanation
Bandwidth	The amount of data transmitted per unit of time, typically bits per second (bps) or bytes per second (Bps).
Bit	A unit of information used by digital computers. Represents the smallest piece of addressable memory within a computer. A bit expresses the choice between two possibilities and is typically represented by a logical one (1) or zero (0).
Bit Stuffing	Insertion of a "0" bit into a data stream to cause an electrical transition on the data wires allowing a PLL to remain locked.
Bulk Transfer	Nonperiodic, large burst communication typically used for a transfer that can use any available bandwidth and also be delayed until bandwidth is available.
Control Transfer	One of four Universal Serial Bus Transfer Types. Control transfers support configuration/command/status type communications between client and function.
CRC	See Cyclic Redundancy Check.
Cyclic Redundancy Check	A check performed on data to see if an error has occurred in transmitting, reading, or writing the data. The result of a CRC is typically stored or transmitted with the checked data. The stored or transmitted result is compared to a CRC calculated for the data to determine if an error has occurred.
Device Endpoint	A uniquely identifiable portion of a Universal Serial Bus device that is the source or sink of information in a communication flow between the host and device.
Endpoint	See Device Endpoint.
Interrupt Transfer	One of four Universal Serial Bus Transfer Types. Interrupt transfers characteristics are small data, non-periodic, low frequency, bounded latency, device initiated communication typically used to notify the host of device service needs.
Isochronous Transfer	One of four Universal Serial Bus Transfer Types. Isochronous transfers are used when working with isochronous data. Isochronous transfers provide periodic, continuous communication between host and device.
Non-Return-to-Zero-Invert	A method of encoding serial data in which ones and zeroes are represented by opposite and alternating high and low voltages where there is no return to zero (reference) voltage between encoded bits. Eliminates the need for clock pulses.
NRZI	See Non-Return-to-Zero-Invert.
PLL	Phase Locked Loop. A circuit that acts as a phase detector to keep an oscillator in phase with an incoming frequency.
Protocol	A specific set of rules, procedures, or conventions relating to format and timing of data transmission between two devices.
Transaction	The delivery of service to an endpoint. Consists of a token packet, optional data packet, and optional handshake packet. Specific packets are allowed/required based on the transaction type.
Transfer	One or more bus transactions to move information between a software client and its function.
Transfer Type	Determines the characteristics of the data flow between a software client and its function. Four Transfer types are defined: control, interrupt, bulk, and isochronous.
Universal Serial Bus	A collection of Universal Serial Bus devices and the software and hardware that allow them to connect the capabilities provided by functions to the host.
Universal Serial Bus Interface	The hardware interface between the Universal Serial Bus cable and a Universal Serial Bus device. This includes the protocol engine required for all Universal Serial Bus devices to be able to receive and send packets.
USB	See Universal Serial Bus.

APPENDIX

0.5μm MSM13R0000 SOG and MSM98R000 CSA USB I/O Library Data Sheets

The following section contains USB I/O library data sheets

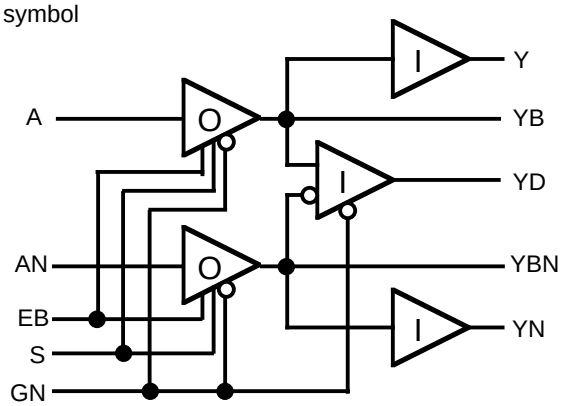
BUD2SLL

USB I/O Buffer with Full / Low Speed

Cell Count

4 I/O 2 PADs

Logic symbol



Pin Definition

Name	Type	Fan-in	Fan-out (MAX.)
A	In	2.9	-
AN	In	2.9	-
EB	In	3.0	-
GN	In	7.3	-
S	In	5.8	-
YB	I/O	-	-
YBN	I/O	-	-
YD	Out	-	43
Y	Out	-	40
YN	Out	-	40

Truth Table

Input							Output				
A	AN	EB	S	GN	YB	YBN	YB	YBN	YD	Y	YN
0	1	1	0	0	-	-	0	1	0	0	1
1	0	1	0	0	-	-	1	0	1	1	0
0	0	1	0	0	-	-	0	0	X	0	0
1	1	1	0	0	-	-	1	1	X	1	1
X	X	0	0	0	0	1	-	-	0	0	1
X	X	0	0	0	1	0	-	-	1	1	0
X	X	X	0	1	Z	Z	-	-	1	X	X
0	1	1	1	0	-	-	0	1	0	0	1
1	0	1	1	0	-	-	1	0	1	1	0
0	0	1	1	0	-	-	0	0	X	0	0
1	1	1	1	0	-	-	1	1	X	1	1
X	X	0	1	0	0	1	-	-	0	0	1
X	X	0	1	0	1	0	-	-	1	1	0
0	1	1	1	1	-	-	0	1	1	0	1
1	0	1	1	1	-	-	1	0	1	1	0
0	0	1	1	1	-	-	0	0	1	0	0
1	1	1	1	1	-	-	1	1	1	1	1
X	X	0	1	1	Z	Z	-	-	1	X	X

Note:
S=0: Low Speed Function
S=1: Full Speed Function

BUD2SLL

USB I/O Buffer with Full / Low Speed

Cell Count

4 I/O 2 PADs

Delay Parameters (VDD = 3.3V,Tj=25°C)

From	To	LH/HL	tpd0' (ns)	α (ns/FO)	γ (ns/pF)
YB	YD	LH	1.658	0.021	0.582
		HL	1.593	0.016	0.384
YBN	YD	LH	1.658	0.021	0.582
		HL	1.593	0.016	0.384
GN	YD	LH	0.668	0.021	0.582
		HL	1.230	0.016	0.378
YB	Y	LH	0.480	0.022	0.591
		HL	1.033	0.032	0.767
YBN	YN	LH	0.480	0.022	0.591
		HL	1.033	0.032	0.767

S=0: Low Speed

From	To	LH/HL	tpd0' (ns)	α (ns/FO)	γ (ns/pF)
A	YB	LH	113.448	-	0.082
		HL	112.385	-	0.071
AN	YBN	LH	121.419	-	0.082
		HL	112.658	-	0.071
EB	YB	LZ	1.992	-	0.190
		ZL	2.567	-	0.071
		HZ	1.496	-	0.215
		ZH	70.919	-	0.082
EB	YBN	LZ	2.516	-	0.190
		ZL	2.798	-	0.071
		HZ	2.562	-	0.215
		ZH	67.373	-	0.082
GN	YB	LZ	1.853	-	0.190
		ZL	2.127	-	0.071
		HZ	1.335	-	0.215
		ZH	93.127	-	0.082
GN	YBN	LZ	2.401	-	0.190
		ZL	2.367	-	0.071
		HZ	2.401	-	0.215
		ZH	89.655	-	0.082

S=1: Full Speed

From	To	LH/HL	tpd0' (ns)	α (ns/FO)	γ (ns/pF)
A	YB	LH	4.550	-	0.608
		HL	4.261	-	0.238
AN	YBN	LH	4.569	-	0.498
		HL	4.246	-	0.237
EB	YB	LZ	1.191	-	0.152
		ZL	4.774	-	0.149
		HZ	3.193	-	0.165
		ZH	1.221	-	0.068
EB	YBN	LZ	1.194	-	0.366
		ZL	4.773	-	0.145
		HZ	3.703	-	0.407
		ZH	0.692	-	0.098

Power Dissipation (VDD = 3.3V,Tj =25°C)

S=0:Low Speed Function

AC: 2940.4µW/MHz

DC: 311.2µW YB=VIH=3.3V, YBN=VIL=0V

1730.9µW(#2) YB=VOH≥2.8V, YBN=VOL≤0.3V

1353.8µW(#2) YB=VOL≤0.3V, YBN=VOH≥2.8V

0.0µW when Power Down Mode(GN=1) is used

S=1:Full Speed Function

AC: 48.0µW/MHz

DC: 311.2µW YB=VIH=3.3V, YBN=VIL=0V

1009.4µW(#1) YB=VOH≥2.8V, YBN=VOL≤0.3V

723.4µW(#1) YB=VOL≤0.3V, YBN=VOH≥2.8V

0.0µW when Power Down Mode(GN=1) is used

DC Parameters (VDD: core/IO = 3.3/3.3V±0.3V,Tj = 0 to 85°C)

Parameter	Value	Conditions
VDI	0.2V	-
Vt+	2.0V	-
Vt-	0.8V	-
VOH	2.8V	15kΩ to GND
VOL	0.3V	1.5kΩ to 3.6V

Note: VDI = Differential Input Sensitivity

Output Switching Parameters (VDD = 3.3V,Tj =25°C)

Output	tr0 (ns)	γr (ns/pF)	tf0 (ns)	γf (ns/pF)
YB#1	1.822	0.095	2.041	0.090
YBN#1	1.491	0.105	1.821	0.087
YB#2	79.749	0.106	77.070	0.055
YBN#2	136.166	0.001	78.704	0.085

Note: #1 = Full Speed Function

YB: RPD=15kΩ , RPU=1.5kΩ

YBN: RPD=15kΩ

#2 = Low Speed Function

YB: RPD=15kΩ

YBN: RPD=15kΩ , RPU=1.5kΩ

References

See the *USB Specification Revision 1.0* for more information on USB functionality.