MITEL SEMICONDUCTOR

VP536E

NTSC/PAL Digital Video Encoder

DS4322 - 3.2 August 1997

FEATURES

- Converts RGB data (3x8bits) to analog composite video and S-video
- Internal video timing generation
- RGB or YUV input modes
- Progressive scanning (non-interlaced fields) display mode optional
- Separate horizontal and vertical sync outputs
- 68 pin PLCC package

APPLICATIONS

- Multi-media
- Video Games
- PC's
- Graphics
- Display Adaptors
- Video Effects Processors

DESCRIPTION

The VP536E converts digital RGB data (3x8bits) into analog NTSC/PAL composite video and S-video signals. The outputs are capable of driving doubly terminated 75 ohm loads with standard video levels.

The device will also accept YUV data. Progressive scan (non-interlaced fields) video display is available in both NTSC and PAL modes.

The output pixel rate is approximately 7 times Fsc (color subcarrier frequency) for NTSC (6.6 times Fsc for PAL) which is approximately 25MHz. Input pixel rate is half this frequency; approximately 12.5MHz.

All the necessary synchronization signals are generated internally. Digital horizontal and vertical sync outputs are available for use by the host system.

The rise and fall times of sync, burst envelope and video blanking are internally controlled to be within composite video specifications.

Two 8-bit digital to analog converters (DACs) are used to convert the digital luminance and chrominance data into analog signals. An inverted composite video signal is generated by summing the complimentary current outputs of each DAC. An internally generated reference voltage provides the biasing for the DACs.

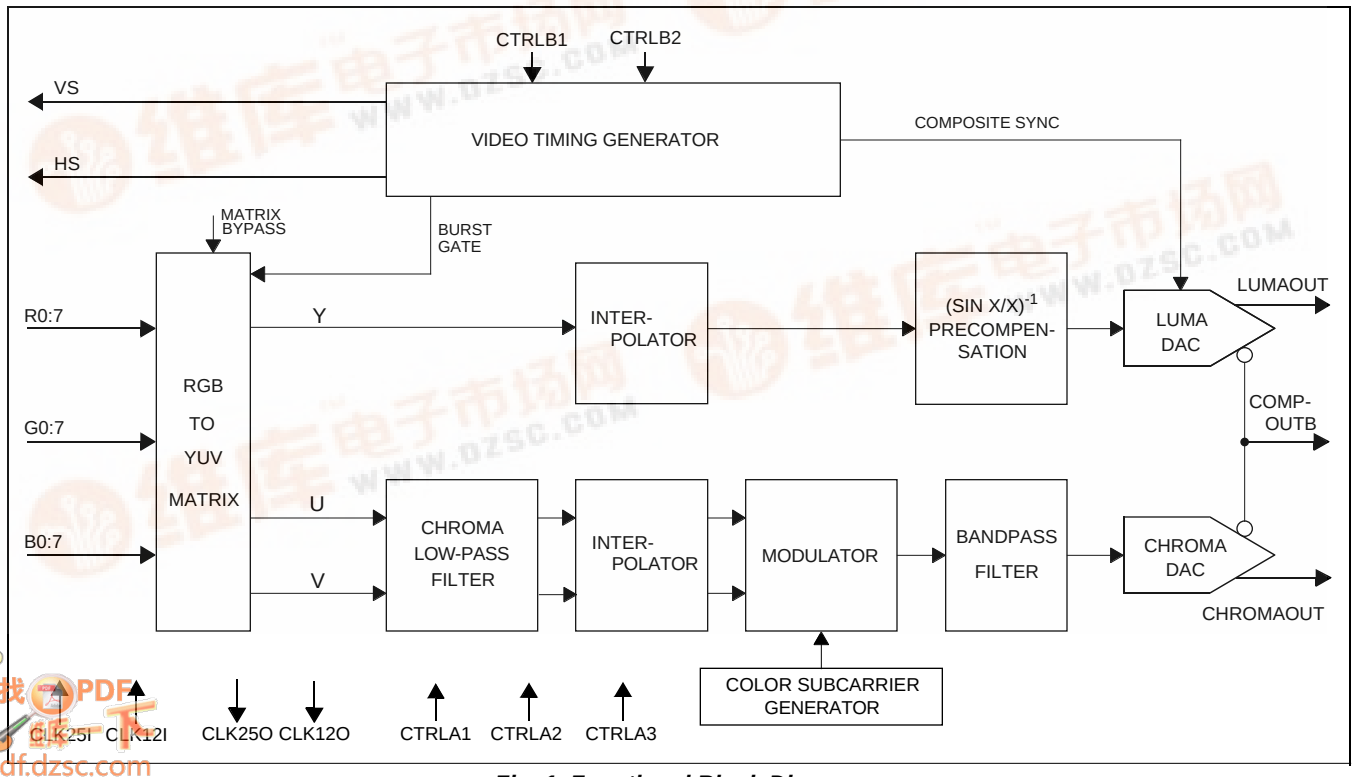


Fig. 1. Functional Block Diagram

NTSC/PAL Video Standards

Both NTSC (4-field, 525 lines) and PAL (8-field, 625 lines) video standards are supported by the VP536E. All raster synchronization, color subcarrier and burst characteristics are adapted to the standard selected. However, different input clock frequencies are necessary for each of the two video standards. For the NTSC mode of operation, input clock frequencies of 25.048948MHz. and 12.524474MHz. are required. For the PAL mode of operation, the required input clock frequencies are 29.500000MHz. and 14.750000MHz. The two input clock frequencies in each of the video standards are related by a ratio of 2.

The mode of operation is selected through the CTRLB1 and CTRLB2 pins as shown in Table 1.

Progressive Scan Display

Progressive scan (non-interlaced fields) display mode is available for semi-NTSC and semi-PAL video applications.

For NTSC, there are 263 lines in each field instead of 262.5 lines per field in a normal NTSC display. Thus, 263 lines of field 2 data are scanned as field 1 resulting in 526 lines per 'frame'.

For PAL, there are 313 lines in each field instead of 312.5 lines per field in a normal PAL display. Thus, 313 lines of field 2 data are scanned as field 1, resulting in 626 lines per 'frame'.

Progressive scanning display mode is selected through the CTRLB1 and CTRLB2 pins as shown in Table 1.

Table 1: VP536E Modes of Operation

CTRLB2	CTRLB1	Video Standard
0	0	NTSC
0	1	Progressive Scan NTSC
1	0	PAL
1	1	Progressive Scan PAL

NOTE: CTRLB1 & CTRLB2 are internally pulled low, therefore, if left unconnected, NTSC is the default mode of operation.

Video Timing

The VP536E has an internal sync generator which produces video timing signals appropriate to the mode of operation. All timing signals are derived from the two input clocks. These clocks are input on the CLK25I pin (25.048948MHz:NTSC/29.5MHz:PAL) and the CLK12I pin (12.52444MHz:NTSC/14.75MHz:PAL). The two input clock frequencies for NTSC and PAL are related by a ratio of 2.

The lower frequency corresponds to the input pixel data rate. Input pixel data is latched in on the rising edge of the CLK12I clock.

The clocks must be derived from a crystal controlled oscillator in order to avoid timing, chroma frequency and modulation errors.

The video timing generator produces the internal composite sync, blanking and burst gate as well as externally available horizontal sync (HS) and vertical sync (VS) pulse signals. The HS and VS signals are negative true pulses coincident with the sync pulses in the output video signals.

The HS signal has the same duration as a standard horizontal sync pulse but is continuous through the vertical sync interval.

Input Pixel Data Format

Input pixel data may be in one of two formats; pre-gamma corrected RGB and YUV. This format is controlled by the state of theCTRLA1, CTRLA2 and CTRLA3 pins as shown in Table 2.

The RGB input data coding is straight binary and is in the range of 0-255. In the YUV input mode, Y, U and V data is presented on the R, B and G input data buses, respectively. Y data coding is binary and is in the range of 0-247. U and V coding is in two's compliment binary. U is in the range of -102 to +102 and V is in the range of -107 to +107.

Dithering

In applications where the input RGB/YUV data has been subject to video compression, visual artefacts may occur in the video display depending on the type and quality of video compression employed.

The VP536E incorporates dithering techniques on the incoming RGB data and on the internal luminance data in order to minimize any artefacts.

Each of these dithering techniques can be enabled or disabled through the CTRLA1 and CTRLA2 pins as shown in Table 2 below.

Table 2: Input Pixel Data Format and Dithering Selection

CTRLA3	CTRLA2	CTRLA1	Input Pixel Data Format
0	0	0	RGB input dither ON, Luma dither OFF
0	0	1	RGB input dither ON, Luma dither ON
0	1	0	RGB input dither OFF, Luma dither ON
0	1	1	RGB input dither OFF, Luma dither OFF
1	0	0	YUV input, Luma dither ON
1	0	1	YUV input, Luma dither OFF
1	1	0	reserved
1	1	1	reserved

NOTE: CTRLA1 is internally pulled high, while CTRLA2 & CTRLA3 are internally pulled low; therefore if left unconnected, pre-gamma corrected RGB is the default input pixel data format with input RGB and luma dithering enabled.

Video Blanking

The VP536E automatically performs standard composite video blanking. Lines 1-17, 261-279, 523-525 inclusive, as well as the last half of line 260 and the first half of line 280 are blanked in the NTSC mode. In PAL mode, lines 1-22, 311-335, 624-625 inclusive, as well as the last half of line 623 and the first half of line 23 are blanked.

The host pixel data can be phased relative to the active video timing by counting the CLK12I clock periods from the rising edge of HS. NTSC active video starts 48 CLK12I clock cycles after the rising edge of the horizontal sync pulse output, and PAL active video starts 58 CLK12I clock periods after the rising edge of HS (HS and VS pulse edges coincide with the rising edge of the CLK12I clock).

Input pixel data is ignored during the composite blanking periods.

Color Space Matrix

The RGB color space is converted to a YUV color space, using a transformation matrix defined by the NTSC and PAL colorimetry definitions. If the input data format is YUV, this block is bypassed without affecting the overall data latency.

Interpolator

The luminance and chrominance data is separately passed through interpolating filters to produce output sampling rates double that of the incoming pixel rate. This reduces the sinx/x distortion that is inherent in the digital to analog converters and also simplifies the analog reconstruction filter requirements.

Sinx/x Distortion Precompensation

The luminance data is precompensated for the sinx/x distortion that is inherent in the digital to analog converters. Since the chrominance data is contained within a relatively narrow frequency range, it's sinx/x distortion is compensated for by increasing the gain of the chrominance DAC by a fixed amount.

Digital To Analog Converters

The VP536E contains two 8-bit digital to analog converters which produce the analog video signals. The DACs use a current steering architecture in which bit currents are routed to one of two outputs; thus each DAC has a true and complimentary output. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed. An on-chip voltage reference of 1.0V (typ.) provides the necessary biasing. However, the VP536E may be used in applications where an external 1V reference is provided, in which case the external reference should be temperature compensated and provide a low impedance output.

The full-scale output currents of the DACs is set by external resistors between the LUMAGAIN, CHROMAGAIN and GND pins. An on-chip loop amplifier stabilizes the full-scale output current against temperature and power supply variations.

By summing the complimentary current outputs of the two DACs, an inverted composite video signal is obtained. Note that this signal has a DC offset. The analog outputs of the VP536E are capable of directly driving a 37.5 ohm load, such as a doubly terminated 75 ohm co-axial cable.

DAC Gain Adjust

The gains of the luma and chroma DACs are independently adjustable. The gains are adjusted using the external gain setting resistors between the LUMAGAIN, CHROMAGAIN pins and GND.

For the correct DAC gains in the NTSC & PAL modes, the LUMAGAIN resistance should be 837ohms. The CHROMAGAIN resistance should be 520ohms for the proper corresponding chroma amplitude (including sinx/x compensation).

Luminance, Chrominance & Composite Video Outputs

The Luminance video output (LUMAOUT pin) drives a 37.5 ohm load at 1.0V, sync tip to peak white. It contains only the image's luminance content plus the composite synchronization pulses.

The chrominance video output (CHROMAOUT pin) drives a 37.5 ohm load at levels proportional in amplitude to the luma output. This output has a fixed offset current which will produce approximately a 0.5V DC bias across the 37.5 ohm load. Burst is injected with appropriate timing relative to the luma signal.

Luma, Chroma and true Composite video signals may be obtained simultaneously through the use of an external inverting video amplifier with the inverted composite video output (COMPOUTB pin).

The inverted composite video output has a fixed DC offset. Sync tip is the most positive voltage and is approximately 1.5V with a 37.5 ohm load.

The NTSC and PAL output video waveforms of the luma, chroma and inverted composite signals for 100% amplitude, 100% saturated color bars are shown in Figs. 3-8.

Extendable S-Video Bandwidth

The bandwidth of color baseband signals is typically limited in order to avoid modulation problems that develop in composite video due to the interleaving of the chrominance and luminance frequency components. The VP536E can use either traditional bandwidth limited or extended bandwidth baseband signals. For applications where the composite signal is the main source of the video display, it is recommended that bandwidth limiting be used in order to reduce "dot-crawl" effects in the display. For S-Video applications where the luma and chroma signals are separate, enabling the extended bandwidth will result in improved picture definition.

The enabling/disabling of this bandwidth extension is controlled through the TCSPK pin as shown below.

Table 3: Bandwidth Control

TCSPK	Chroma Bandwidth
0	Extended Bandwidth
1	Limited Bandwidth

NOTE: TCSPK is internally pulled LOW, therefore Extended Bandwidth is the default selection.

Master Reset

The VP536E can be initialized with the RESET pin. This is an active low signal and must be active for a minimum of 2 CLK12I clock periods in order for the VP536E to be reset.

Video Timing Reset

The VP536E also features the ability to independently reset the video timing generator without affecting the data path. The TSURST pin controls this function. Taking this pin high resets the video timing generator. If this pin is left open, it is internally pulled low.

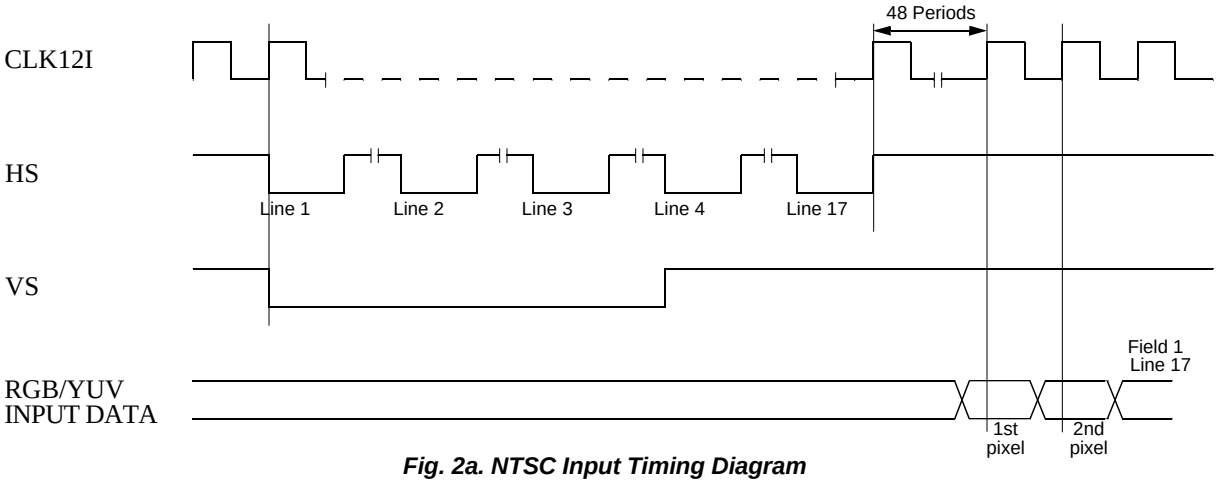


Fig. 2a. NTSC Input Timing Diagram

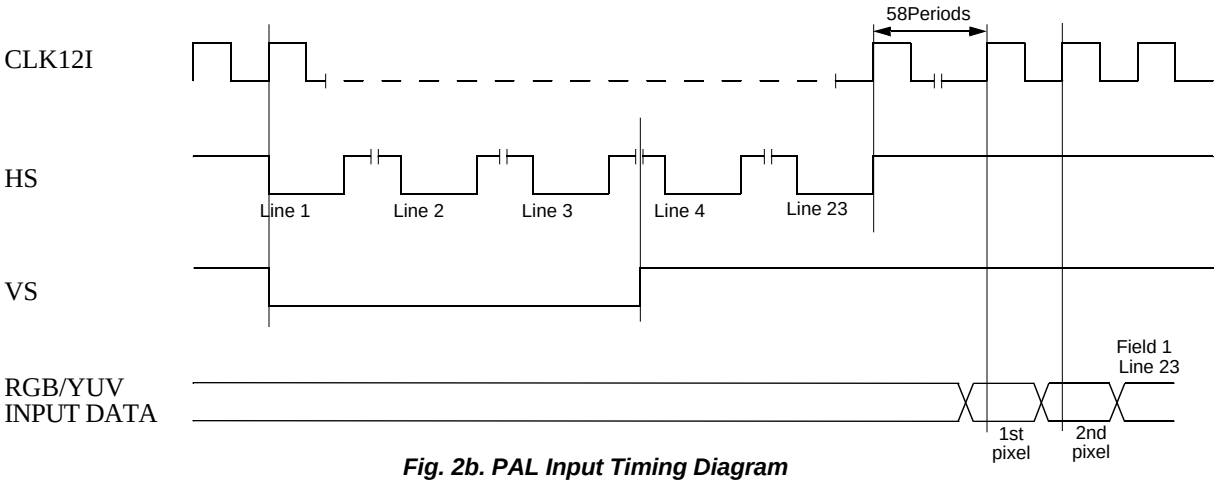


Fig. 2b. PAL Input Timing Diagram

NOTE:

1. Coincident falling edges of HS and VS denote the start of an odd field.
2. VS is low during the first 3 lines in each NTSC field and during the first $2^1/_2$ lines in each PAL field.
3. Input pixel data is ignored during composite blanking periods.

Fig. 3.
NTSC Luminance Video Output Waveform

100% saturation, 100% amplitude color bars.

LUMAGAIN resistor = 837 ohms, VREF=1.0V, 37.5 ohm load.

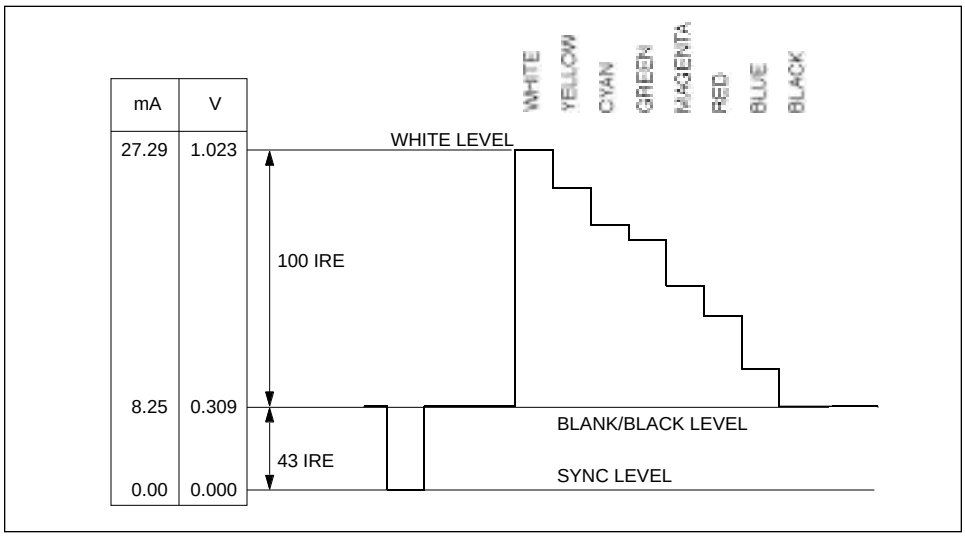


Fig. 4.
NTSC Chrominance Video Output Waveform

100% saturation, 100% amplitude color bars.

CHROMAGAIN resistor = 520 ohms, VREF=1.0V, 37.5 ohm load.

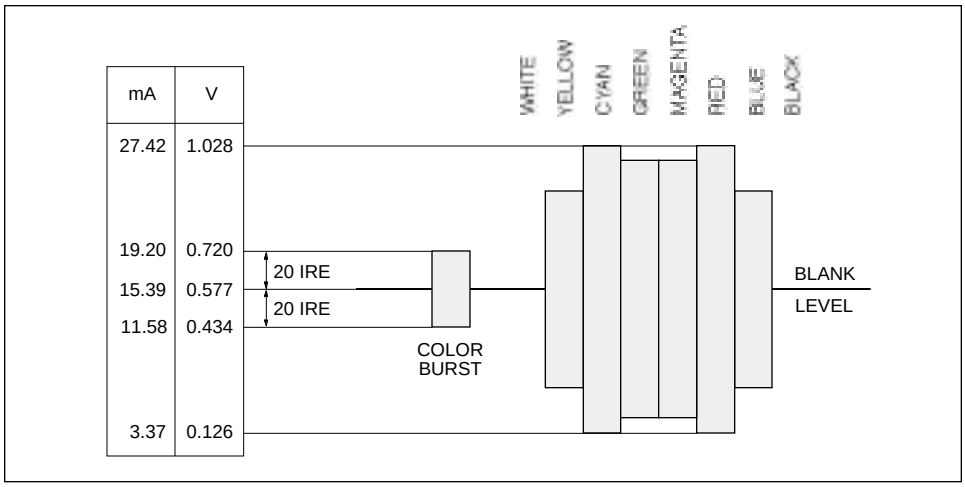


Fig. 5.
NTSC Inverted Composite Video Output Waveform

100% saturation, 100% amplitude color bars.

LUMAGAIN resistor = 837 ohms, CHROMAGAIN resistor = 520 ohms, VREF=1.0V, 37.5 ohm load

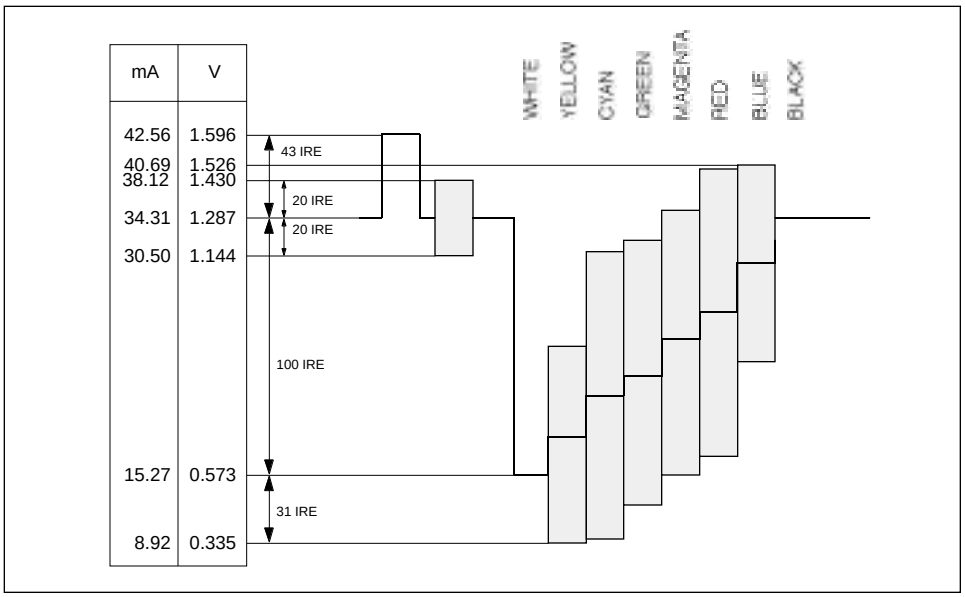


Fig. 6.
PAL Luminance Video Output Waveform

100% saturation, 100% amplitude color bars.

LUMAGAIN resistor = 837 ohms, VREF=1.0V, 37.5 ohm load.

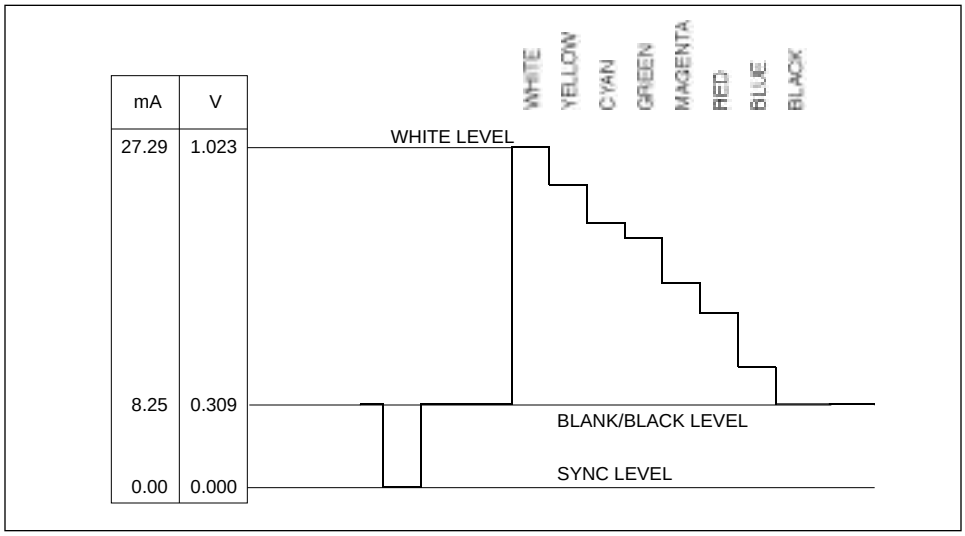


Fig. 7.
PAL Chrominance Video Output Waveform

100% saturation, 100% amplitude color bars.

CHROMAGAIN resistor = 520 ohms, VREF=1.0V, 37.5 ohm load.

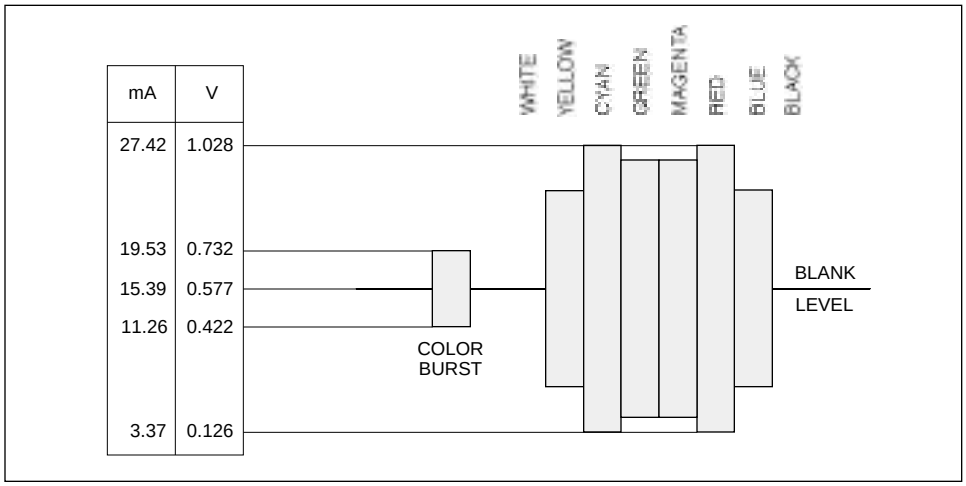
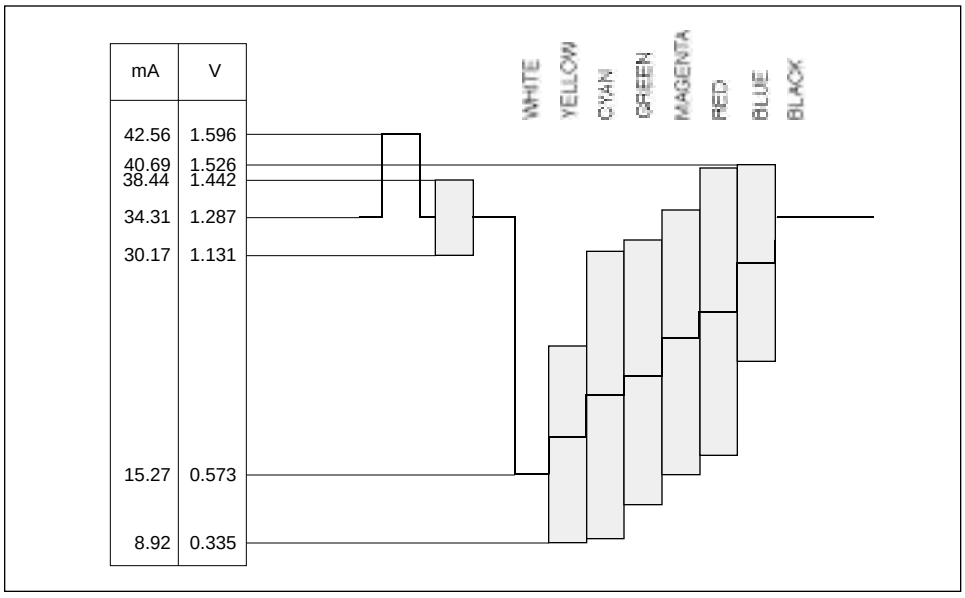


Fig. 8.
PAL Inverted Composite Video Output Waveform

100% saturation, 100% amplitude color bars.

LUMAGAIN resistor = 837 ohms, CHROMAGAIN resistor = 520 ohms, VREF=1.0V, 37.5 ohm load



Pin Descriptions

Table 4: Pin Descriptions

Pin Name	Pin No.	Description
B0-B7	2-9	8 Bit Blue data inputs. B0 is the least significant bit, corresponding to Pin 2. These pins are internally pulled low.
G0-G7	17-24	8 Bit Green data inputs. G0 is the least significant bit. These pins are internally pulled low.
R0-R6, R7	62-68, 1	8 Bit Red data inputs. R7 is the most significant bit corresponding to Pin 1. These pins are internally pulled low.
CLK25I	57	2X pixel rate clock input. The VP536E requires a clock whose frequency is twice the input pixel data rate; i.e., 25.0489484MHz. for the NTSC mode of operation; 29.500000MHz. for the PAL mode of operation.This clock must be derived from a crystal controlled oscillator in order to avoid chroma frequency, modulation and timing errors.
CLK12I	60	Pixel rate clock input. The frequency of this clock must be exactly half that of the CLK25I clock. The rising edges of these two clocks must be synchronous.
CLK25O	61	2X pixel rate clock output. The CLK25I clock is output on this pin. Note that this output clock signal is inverted with respect to the CLK25I clock.
CLK12O	51	Pixel rate clock output. The CLK12I clock is output on this pin.
HS	14	Horizontal sync pulse output. This is an active low signal output, i.e. the presence of a sync pulse is denoted by the signal being low.
VS	13	Vertical sync pulse output. This is an active low signal output.
RESET	16	VP536E master reset. This is an active low input signal and must be asserted for a minimum of 2 CLK12I clock periods in order to reset the VP536E.
CTRLA1 CTRLA2 CTRLA3	59 58 54	Input data format and dithering control. Control codes on these three input pins determine the format of the input data as described in Input Pixel Data Format on Page 2. CTRLA1 is internally pulled high, while CTRLA2 and CTRLA3 are internally pulled low; therefore if left open, the default input data format is pre-gamma corrected RGB with dithering as described on Page 2.
CTRLB1 CTRLB2	52 53	Video standard control. Control codes on these two input pins determine the video display mode as described in Table 1 on Page 2. These pins are internally pulled low, therefore if left open, the default video display mode is NTSC.
TCSPK	49	Enable/Disable extended video bandwidth. Taking this pin high limits the bandwidth of the video signal as described in Extendable S-Video Bandwidth on Page 3. This pin is internally pulled low, therefore if left open, extended bandwidth is enabled.
TSURST	50	Synchronous reset of video timing. An active high pulse on this pin resets the video timing generator without affecting the data path. On the rising edge of CLK12I following TSURST going low, Field 1, line 1 is initiated. This pin is internally pulled low.
VREF	28	Voltage reference output. This output is nominally 1.0V and should be decoupled with a 1.0µF capacitor to GND.
LUMA-COMP	30	Luma DAC compensation. A 0.1µF ceramic capacitor must be connected between this pin and it's neighboring VAA pin (pin 31).
CHROMA-COMP	38	Chroma DAC compensation. A 0.1µF ceramic capacitor must be connected between this pin and it's neighboring VAA pin (pin 37).
LUMAOUT COMPOUTB CHROMAOUT	32 34 36	Luminance, inverted composite and chrominance video signal outputs. These outputs are high impedance current source outputs. A DC path to GND must exist from each of these pins.
LUMAGAIN	29	Luminance full scale current control. A resistor connected between this pin and GND sets the magnitude of the luminance video output current. An internal loop amplifier controls a reference current flowing through this resistor so that the voltage across it is equal to the Vref voltage. This reference current has a weighting equal to 16 LSB's. Note that the IRE relationships shown in Fig. 3 are maintained, regardless of the output full scale current.

Table 4: Pin Descriptions (Continued)

Pin Name	Pin No.	Description
CHROMAGAIN	39	Chrominance full scale current control. As with the LUMAGAIN pin, a resistor between this pin and GND controls the magnitude of the chrominance video signal. An internal loop amplifier adjusts a reference current flowing through this resistor so that the voltage across it is equal to the Vref voltage. This reference current has a weighting equal to 16 LSB's.
TEST0-TEST7	41-48	These pins must be held low.
CTRLC1 CTRLC2	15 12	Test mode control. These two pins are used to configure the VP536E into various test modes. They should be held low during normal operation.
VAA	10, 25, 31, 37, 40, 55	Power. All VAA pins must be connected.
GND	11, 26, 56 27, 33, 35	Ground. All GND pins must be connected.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply voltage	VAA	4.75	5.00	5.25	V
Input clock frequency					
CLK25I (NTSC)			25.048948		MHz.
CLK12I (NTSC)			12.524474		MHz.
CLK25I (PAL)			29.500000		MHz.
CLK12I (PAL)			14.750000		MHz.
CLK25I & CLK12I rising edges must be synchronous					
Input clock frequency accuracy				25	ppm
Analog video output load			37.5		Ω
Gain resistors					
Lumagain resistor (NTSC)			837		Ω
Chromagain resistor (NTSC)			520		Ω
Lumagain resistor (PAL)			837		Ω
Chromagain resistor (PAL)			520		Ω
Ambient operating temperature		0		70	^{o}C

ABSOLUTE MAXIMUM RATINGS (Referenced to GND)

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply	VAA	-0.3		7	V
Voltage on any non-power pin		-0.3		VAA + 0.3	V
Analog video output short circuit duration			Indefinite		
Ambient operating temperature		0		70	^{o}C
Storage temperature		-40		125	^{o}C

NOTE: Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC Characteristics (see note on Page 11)

Parameter	Symbol	Min.	Typ.	Max.	Units
Resolution (each DAC)		8			Bits
Accuracy (each DAC)					
Integral linearity error	INL			+/- 1.5	LSB
Differential linearity error	DNL			+/- 1	LSB
Gray scale error				+/- 5	% gray scale
Monotonicity			Guaranteed		
Analog video output compliance	V_{AVOC}	-0.3		1.6	V
Digital Inputs					
Input high voltage	V_{IH}	3.0			V
Input low voltage	V_{IL}			0.8	V
Digital Outputs					
Output high voltage (I_{OH} = -10.0 mA)	V_{OH}	VAA - 1			V
Output low voltage (I_{OL} = 10.0 mA)	V_{OL}			0.4	V
Luminance video output current					
White level relative to black/blank level (NTSC)		18.11	19.04	19.97	mA
Black/Blank level relative to sync level (NTSC)		7.67	8.25	8.83.	mA
White level relative to black/blank level (PAL)		18.11	19.04	19.97	mA
Black/blank level relative to sync level (PAL)		7.67	8.25	8.83	mA
Chrominance video output current					
Blank level (NTSC)		14.62	15.39	16.16	mA
Peak chroma level relative to blank level (NTSC) (corresponding to 100% saturated red)		+/- 10.95	+/- 12.03	+/- 13.11	mA
Peak burst level relative to blank level (NTSC)		+/- 3.46	+/- 3.81	+/- 4.16	mA
Blank level (PAL)		14.62	15.39	16.16	mA
Peak chroma level relative to blank level (PAL) (corresponding to 100% saturated red)		+/- 10.95	+/- 12.03	+/- 13.11	mA
Peak burst level relative to blank level (PAL)		+/- 3.77	+/- 4.14	+/- 4.51	mA
Internal reference voltage	V_{REF}	0.95	1.00	1.05	V
Internal reference voltage output impedance			25		KΩ

AC Characteristics (see note on Page 11)

Parameter	Symbol	Min.	Typ.	Max.	Units
CLK12I clock delay with respect to CLK25I clock (tested with 50% duty cycle CLK12I and CLK25I clocks)	t_{dCLK}	0		18	ns
Data set-up time (wrt CLK12I clock)	t_{suDATA}	8			ns
Data hold time (wrt CLK12I clock)	t_{hDATA}	5			ns
HS/VS output delay wrt CLK12I clock	t_{dSYNC}	0		20	ns
HS low pulse width (NTSC)	$t_{wHS\text{-}NTSC}$		59		CLK12I cycles
HS low pulse width (PAL)	$t_{wHS\text{-}PAL}$		69		CLK12I cycles
VS low pulse width(NTSC)	$t_{wVS\text{-}NTSC}$		2388		CLK12I cycles
VS low pulse width (PAL)	$t_{wVS\text{-}PAL}$		2360		CLK12I cycles
Input clock pulse width high time		16			ns
Input clock pulse width low time		16			ns
Analog video output delay (wrt CLK25I clock)	t_{dAVO}		10		ns
Analog video output rise/fall time	t_{rfAVO}		8		ns
Analog video output settling time (50% to +/- 1 LSB)	t_{sAVO}		12		ns
Signal related harmonics of DAC outputs for 1MHz. direct digitally synthesized sine wave			tbd		dB
Pipeline delay (data in to analog video out)			20.5		CLK12I cycles
VAA supply current	I_{AA}		200		mA
Power supply rejection (chromacomp, lumacomp = 0.1uF, f = 1 KHz.)			40		dB

Timing Waveforms

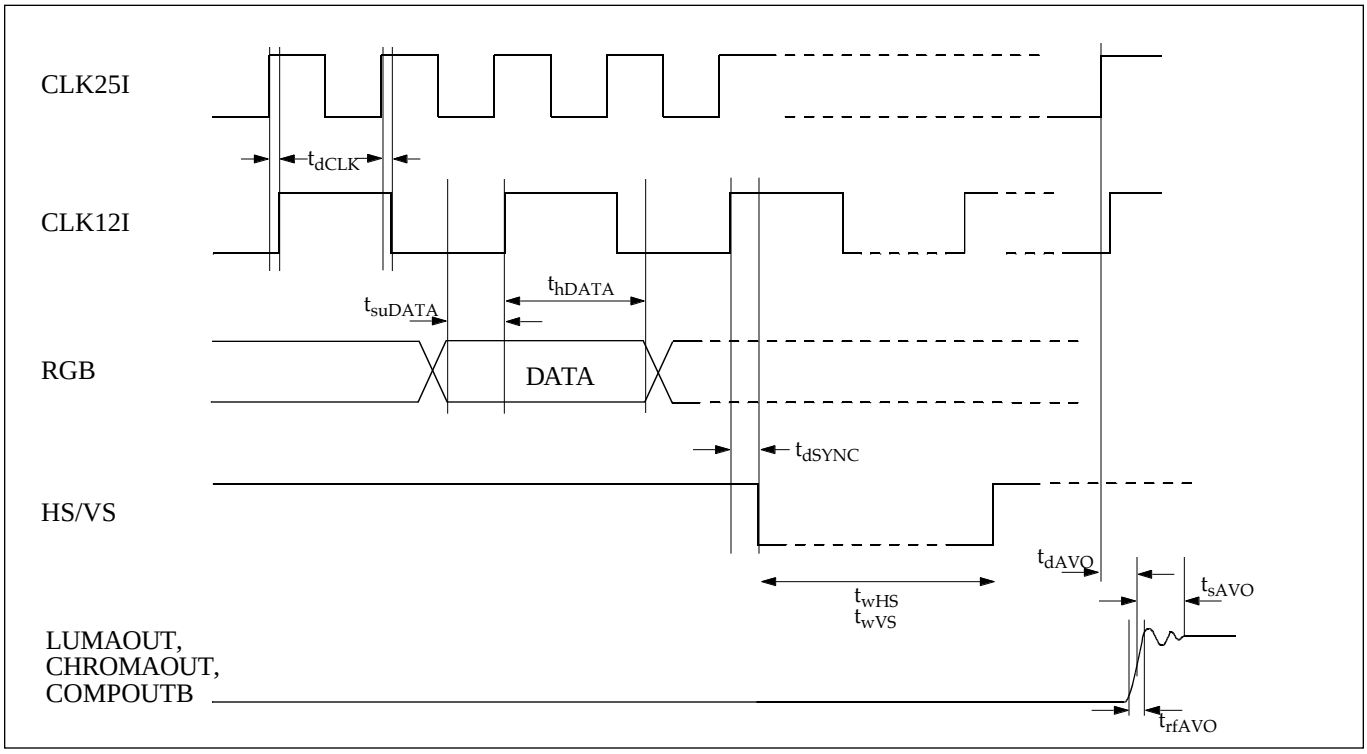


Fig. 9. Input/Output Timing Diagram

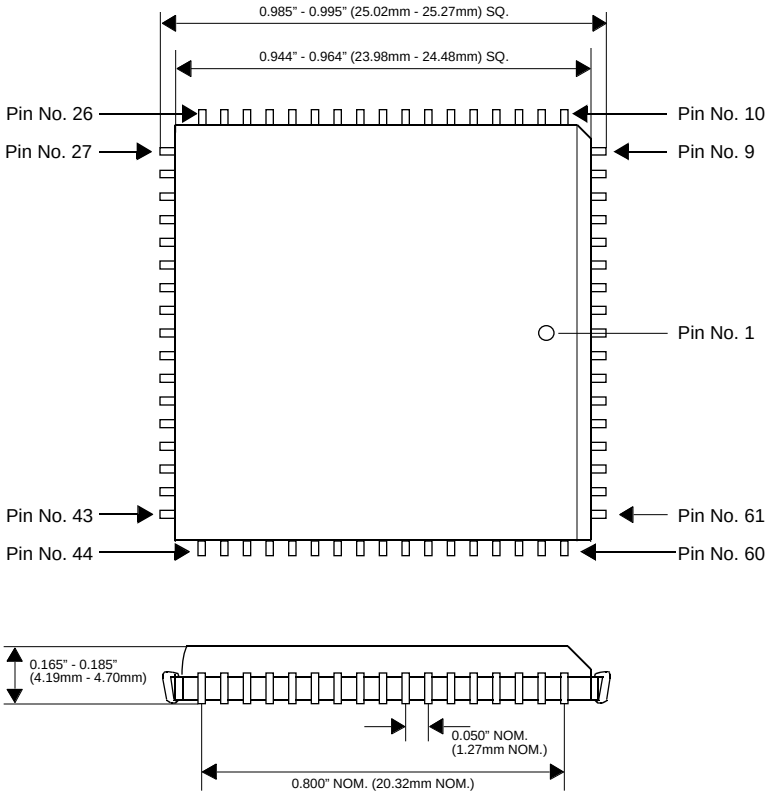
Video Characteristics (see note below)

Parameter	Symbol	Min.	Typ.	Max.	Units
Luminance bandwidth (Extended Bw mode)			4.0		MHz.
Luminance bandwidth (Reduced Bw mode)			2.5		MHz.
Chrominance bandwidth (Extended Bw mode)			1.8		MHz.
Chrominance bandwidth (Reduced Bw mode)			1.2		MHz.
Burst frequency (NTSC)			3.579545		MHz.
Burst frequency (PAL)			4.433619		MHz.
Burst cycles (NTSC)			10		Fsc cycles
Burst cycles (PAL)			10		Fsc cycles
Burst envelope rise/fall time			1.5		Fsc cycles
Analog video sync rise/fall time			90		ns
Analog video blank rise/fall time			160		ns
Differential gain			1.5		% pk-pk
Differential phase			1.0		^{o} pk-pk
Signal to Noise Ratio (white field)			60		dB
Chroma AM signal to noise ratio (100% red field)			58		dB
Chroma PM signal to noise ratio (100% red field)			56		dB
Hue accuracy				2.5	degrees
Color saturation accuracy				2.5	%
Residual subcarrier			-60		dB
Luminance/chrominance delay			20		ns

NOTE: The DC, AC and Video characteristics listed above are based on design targets and/or actual measurements on a limited number of devices. All parametric information is subject to review following further characterization.

Package Details and Pin-Out

68 Pin PLCC Package



Pin No.	Pin Name	Pin No.	Pin Name
1	R7	35	GND
2	B0	36	CHROMAOUT
3	B1	37	VAA
4	B2	38	CHROMACOMP
5	B3	39	CHROMAGAIN
6	B4	40	VAA
7	B5	41	TEST0
8	B6	42	TEST1
9	B7	43	TEST2
10	VAA	44	TEST3
11	GND	45	TEST4
12	CTRLC2	46	TEST5
13	VS	47	TEST6
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17	G0	51	CLK12O
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19	G2	53	CTRLB2
20	G3	54	CTRLA3
21	G4	55	VAA
22	G5	56	GND
23	G6	57	CLK25I
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26	GND	60	CLK12I
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