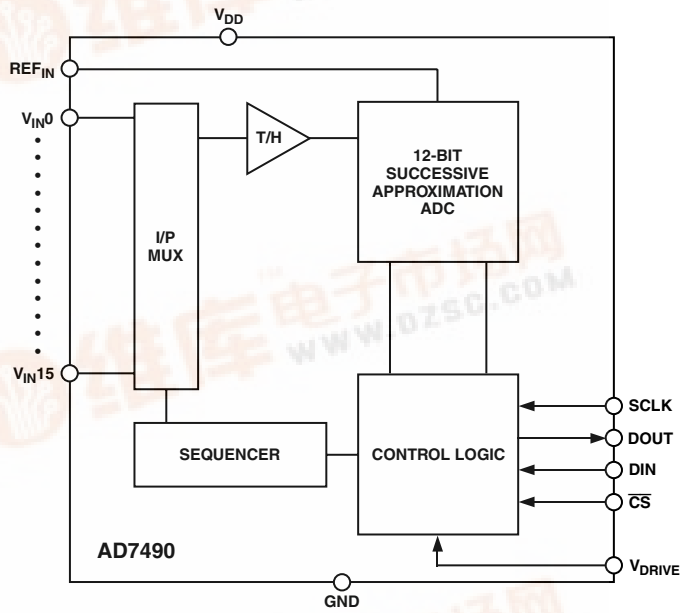
16-Channel, 1 MSPS, 12-Bit ADC with Sequencer in 28-Lead TSSOP

AD7490

FEATURES

- Fast Throughput Rate: 1 MSPS
- Specified for V_{DD} of 2.7 V to 5.25 V
- Low Power at Max Throughput Rates:
  - 5.4 mW Max at 870 kSPS with 3 V Supplies
  - 12.5 mW Max at 1 MSPS with 5 V Supplies
- Sixteen (Single-Ended) Inputs with Sequencer
- Wide Input Bandwidth:
  - 69.5 dB SNR at 50 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High-Speed Serial Interface SPI™/QSPI™/ MICROWIRE™/DSP-Compatible
- Full Shutdown Mode: 0.5 µA Max
- 28-Lead TSSOP and 32-Lead LFCSP Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7490 is a 12-bit high-speed, low power, 16-channel, successive-approximation ADC. The part operates from a single 2.7 V to 5.25 V power supply and features throughput rates up to 1 MSPS. The part contains a low noise, wide bandwidth track/hold amplifier that can handle input frequencies in excess of 1 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock signal, allowing the device to easily interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and conversion is also initiated at this point. There are no pipeline delays associated with the part.

The AD7490 uses advanced design techniques to achieve very low power dissipation at high throughput rates. For maximum throughput rates, the AD7490 consumes just 1.8 mA with 3 V supplies, and 2.5 mA with 5 V supplies.

By setting the relevant bits in the Control Register, the analog input range for the part can be selected to be a 0 to REF_{IN} input or a 0 to 2 × REF_{IN} with either straight binary or two's complement output coding. The AD7490 features sixteen single-ended analog inputs with a channel sequencer to allow a preprogrammed selection of channels to be converted sequentially.

The conversion time is determined by the SCLK frequency as this is also used as the master clock to control the conversion.

PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption
   The AD7490 offers up to 1 MSPS throughput rates. At maximum throughput with 3 V supplies the AD7490 dissipates just 5.4 mW of power.
2. Sixteen Single-Ended Inputs with Channel Sequencer
   A Sequence of channels can be selected, through which the AD7490 will cycle and convert on.
3. Single-Supply Operation with V_{DRIVE} Function
   The AD7490 operates from a single 2.7 V to 5.25 V supply. The V_{DRIVE} function allows the serial interface to connect directly to either 3 V or 5 V processor systems independent of V_{DD}.
4. Flexible Power/Serial Clock Speed Management
   The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. The part also features various shutdown modes to maximize power efficiency at lower throughput rates. Power consumption is 0.5 µA max when in full shutdown.
5. No Pipeline Delay
   The part features a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD7490–SPECIFICATIONS

(V_{DD} = V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, f_{SCLK}[1] = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	B Version[2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 50 kHz Sine Wave, f_{SCLK} = 20 MHz
Signal to Noise 1 Distortion (SINAD)[3]	69	dB min	@ 5 V, 70.5 dB typ
	68	dB min	@ 3 V, 69.5 dB typ
Signal to Noise Ratio (SNR)[3]	69.5	dB min	
Total Harmonic Distortion (THD)[3]	–74	dB max	@ 5 V, –84 dB typ
	–71	dB max	@ 3 V, –77 dB typ
Peak Harmonic or Spurious Noise (SFDR)[3]	–75	dB max	@ 5 V, –86 dB typ
	–73	dB max	@ 3 V, –80 dB typ
Intermodulation Distortion (IMD)[3]			fa = 40.1 kHz, fb = 41.5 kHz
Second Order Terms	–85	dB typ	
Third Order Terms	–85	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	50	ps typ	
Channel-to-Channel Isolation[3]	–82	dB typ	f_{IN} = 400 kHz
Full Power Bandwidth	8.2	MHz typ	@ 3 dB
	1.6	MHz typ	@ 0.1 dB
DC ACCURACY[3]			
Resolution	12	Bits	
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	–0.95/+1.5	LSB max	Guaranteed No Missed Codes to 12 Bits
0 V to $V_{REF\ IN}$ Input Range			Straight Binary Output Coding
Offset Error	±8	LSB max	±0.6 LSB typ
Offset Error Match	±0.5	LSB max	
Gain Error	±2	LSB max	
Gain Error Match	±0.6	LSB max	
0 V to 2 × $V_{REF\ IN}$ Input Range			$–V_{REF\ IN}$ to $+V_{REF\ IN}$ Biased about V_{REF} with Two's Complement Output Coding Offset
Positive Gain Error	±2	LSB max	
Positive Gain Error Match	±0.6	LSB max	
Zero Code Error	±8	LSB max	±0.6 LSB typ
Zero Code Error Match	±1	LSB max	
Negative Gain Error	±1	LSB max	
Negative Gain Error Match	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to REF_{IN}	V	RANGE Bit Set to 1
	0 to 2 × REF_{IN}	V	RANGE Bit Set to 0, V_{DD}/V_{DRIVE} = 4.75 V to 5.25 V for 0 to 2 × REF_{IN}
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT			
REF_{IN} Input Voltage	2.5	V	±1% Specified Performance
DC Leakage Current	±1	µA max	
REF_{IN} Input Impedance	36	kΩ typ	f_{SAMPLE} = 1 MSPS
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 × V_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3 × V_{DRIVE}	V max	
Input Current, I_{IN}	±1	µA max	typically 10 nA, V_{IN} 5 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[4]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} – 0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	µA max	Weak/$\overline{\text{Tri}}$ Bit Set to 0
Floating-State Output Capacitance[4]	10	pF max	Weak/$\overline{\text{Tri}}$ Bit Set to 0
Output Coding	Straight (Natural) Binary		Coding Bit Set to 1
	Two's Complement		Coding Bit Set to 0

Parameter	B Version[2]	Unit	Test Conditions/Comments
CONVERSION RATE			
Conversion Time	800	ns max	16 SCLK Cycles, SCLK = 20 MHz
Track/Hold Acquisition Time[3]	300	ns max	Sine Wave Input
	300	ns max	Full-Scale Step Input
Throughput Rate	1	MSPS max	@ 5 V (See Serial Interface section.)
POWER REQUIREMENTS			
V_{DD}	2.7/5.25	V min/max	
V_{DRIVE}	2.7/5.25	V min/max	
I_{DD}[5]			Digital I/Ps = 0 V or V_{DRIVE}
Normal Mode (Static)	600	µA typ	V_{DD} = 2.7 V to 5.25 V, SCLK On or Off
Normal Mode (Operational)	2.5	mA max	V_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz
(f_S = Max Throughput)	1.8	mA max	V_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz
Auto Standby Mode	1.55	mA typ	f_{SAMPLE} = 500 kSPS
	92	µA max	Static
Auto Shutdown Mode	960	µA typ	f_{SAMPLE} = 250 kSPS
	0.5	µA max	Static
Full Shutdown Mode	0.5	µA max	SCLK On or Off (20 nA typ)
Power Dissipation[5]			
Normal Mode (Operational)	12.5	mW max	V_{DD} = 5 V, f_{SCLK} = 20 MHz
	5.4	mW max	V_{DD} = 3 V, f_{SCLK} = 20 MHz
Auto Standby Mode (Static)	460	µW max	V_{DD} = 5 V
	276	µW max	V_{DD} = 3 V
Auto Shutdown Mode (Static)	2.5	µW max	V_{DD} = 5 V
	1.5	µW max	V_{DD} = 3 V
Full Shutdown Mode	2.5	µW max	V_{DD} = 5 V
	1.5	µW max	V_{DD} = 3 V

NOTES
[1]Specifications apply for f_{SCLK} up to 20 MHz. However, for serial interfacing requirements see Timing Specifications.
[2]Temperature Ranges (B Version): –40°C to +85°C.
[3]See Terminology section.
[4]Sample tested at 25°C to ensure compliance.
[5]See Power Versus Throughput Rate section.
Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} 3 V	5 V	Unit	Description
f_{SCLK}[2]	10	10	kHz min	
	16	20	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}	16 × t_{SCLK}		
t_{QUIET}	50	50	ns min	Minimum Quiet Time Required between Bus Relinquish and Start of Next Conversion
t_2	12	10	ns min	$\overline{CS}$ to SCLK Setup Time
t_3[3]	20	14	ns max	Delay from $\overline{CS}$ Until DOUT Three-State Disabled
t_3b[4]	30	20	ns max	Delay from $\overline{CS}$ to DOUT Valid
t_4[3]	60	40	ns max	Data Access Time after SCLK Falling Edge
t_5	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK Low Pulsewidth
t_6	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK High Pulsewidth
t_7	15	15	ns min	SCLK to DOUT Valid Hold Time
t_8[5]	15/50	15/50	ns min/max	SCLK Falling Edge to DOUT High Impedance
t_9	20	20	ns min	DIN Setup Time prior to SCLK Falling Edge
t_{10}	5	5	ns min	DIN Hold Time after SCLK Falling Edge
t_{11}	20	20	ns min	Sixteenth SCLK Falling Edge to $\overline{CS}$ High
t_{12}	1	1	µs max	Power-Up Time from Full Power-Down/ Auto Shutdown/Auto Standby Modes

NOTES

[1]Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. (See Figure 1.) The 3 V operating range spans from 2.7 V to 3.6 V. The 5 V operating range spans from 4.75 V to 5.25 V.

[2]Mark/Space ratio for the SCLK input is 40/60 to 60/40. The maximum SCLK frequency is 16 MHz with 3 V supplies, to give a throughput of 870 kSPS. Care must be taken when interfacing to account for data access time t_4, and the setup time required for the user's processor. These two times will determine the maximum SCLK frequency with which the user's system can operate. (See Serial Interface section.)

[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.4 V or 0.7 V_{DRIVE} V.

[4]t_3b represents a worst-case figure for having ADD3 available on the DOUT line, i.e., if the AD7490 went back into three-state at the end of a conversion and some other device took control of the bus between conversions, the user would have to wait a maximum time of t_3b before having ADD3 valid on DOUT line. If the DOUT line is weakly driven to ADD3 between conversions then the user would typically have to wait 17 ns at 3 V and 12 ns at 5 V after the $\overline{CS}$ falling edge before seeing ADD3 valid on DOUT.

[5]t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, t_8, quoted in the timing characteristics, is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted)

V_{DD} to GND ..... –0.3 V to +7 V
V_{DRIVE} to GND ..... –0.3 V to V_{DD} + 0.3 V
Analog Input Voltage to GND ..... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND ..... –0.3 V to +7 V
Digital Output Voltage to GND ..... –0.3 V to V_{DD} + 0.3 V
REF_{IN} to GND ..... –0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2] ..... ±10 mA
Operating Temperature Ranges
  Commercial (A Version) ..... –40°C to +85°C
  Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
LFCSP, TSSOP Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 108.2°C/W (LFCSP)
  ..... 97.9°C/W (TSSOP)
  θ_{JC} Thermal Impedance ..... 32.71°C/W (LFCSP)
  .....14°C/W (TSSOP)
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... 215°C
    Infrared (15 sec) ..... 220°C
ESD ..... 1 kV

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch up.

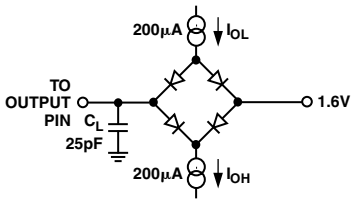


Figure 1. Load Circuit for Digital Output Timing Specifications

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Option	Package Description
AD7490BCP	–40°C to +85°C	±1	CP-32	LFCSP
AD7490BRU	–40°C to +85°C	±1	RU-28	TSSOP
EVAL-AD7490CB[2]	Evaluation Board			
EVAL-CONTROL BRD2[3]	Controller Board			

NOTES

[1]Linearity error refers to integral linearity error.

[2]This can be used as a stand-alone evaluation board or in conjunction with the Evaluation Controller Board for evaluation/ demonstration purposes.

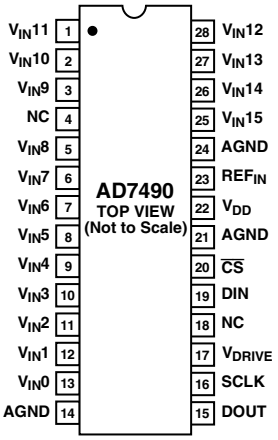
[3]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7490 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

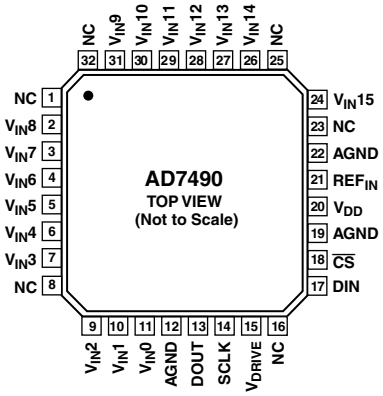
PIN CONFIGURATIONS*

28-Lead TSSOP



NC = NO CONNECT

32-Lead LFCSP



NC = NO CONNECT

EXPOSED PAD SHOULD BE TIED TO AGND

*ALL NC PINS SHOULD BE CONNECTED STRAIGHT TO AGND

PIN FUNCTION DESCRIPTIONS

Mnemonic	Function
$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7490 and also frames the serial data transfer.
REF_{IN}	Reference Input for the AD7490. An external reference must be applied to this input. The voltage range for the external reference is 2.5 V ± 1% for specified performance.
V_{DD}	Power Supply Input. The V_{DD} range for the AD7490 is from 2.7 V to 5.25 V. For the 0 to 2 × REF_{IN} range V_{DD} should be from 4.75 V to 5.25 V.
AGND	Analog Ground. Ground reference point for all circuitry on the AD7490. All analog/digital input signals and any external reference signal should be referred to this AGND voltage. All AGND pins should be connected together.
$V_{IN}0$–$V_{IN}15$	Analog Input 0 through Analog Input 15. Sixteen single-ended analog input channels that are multiplexed into the on-chip track/hold. The analog input channel to be converted is selected by using the address bits ADD3 through ADD0 of the control register. The address bits in conjunction with the SEQ and SHADOW bits allow the Sequencer Register to be programmed. The input range for all input channels can extend from 0 V to REF_{IN} or 0 V to 2 × REF_{IN} as selected via the RANGE bit in the control register. Any unused input channels should be connected to AGND to avoid noise pickup.
DIN	Data In. Logic Input. Data to be written to the AD7490's Control Register is provided on this input and is clocked into the register on the falling edge of SCLK (see Control Register section).
DOUT	Data Out. Logic Output. The conversion result from the AD7490 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream consists of four address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data which is provided MSB first. The output coding may be selected as straight binary or two's complement via the CODING bit in the control register.
SCLK	Serial Clock. Logic Input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7490's conversion process.
V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the serial interface of the AD7490 will operate.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00…000) to (00…001) from the ideal, i.e., AGND + 1 LSB.

Offset Error Match
This is the difference in offset error between any two channels.

Gain Error
This is the deviation of the last code transition (111…110) to (111…111) from the ideal (i.e., REF_{IN} − 1 LSB) after the offset error has been adjusted out.

Gain Error Match
This is the difference in Gain error between any two channels.

Zero Code Error
This applies when using the two's complement output coding option, in particular to the 2 × REF_{IN} input range with –REF_{IN} to +REF_{IN} biased about the REF_{IN} point. It is the deviation of the mid-scale transition (all 0s to all 1s) from the ideal V_{IN} voltage, i.e., REF_{IN} – 1 LSB.

Zero Code Error Match
This is the difference in Zero Code Error between any two channels.

Positive Gain Error
This applies when using the two's complement output coding option, in particular to the 2 × REF_{IN} input range with –REF_{IN} to +REF_{IN} biased about the REF_{IN} point. It is the deviation of the last code transition (011…110) to (011…111) from the ideal (i.e., +REF_{IN} − 1 LSB) after the Zero Code Error has been adjusted out.

Positive Gain Error Match
This is the difference in Positive Gain Error between any two channels.

Negative Gain Error
This applies when using the two's complement output coding option, in particular to the 2 × REF_{IN} input range with –REF_{IN} to +REF_{IN} biased about the REF_{IN} point. It is the deviation of the first code transition (100…000) to (100…001) from the ideal (i.e., –REF_{IN} + 1 LSB) after the Zero Code Error has been adjusted out.

Negative Gain Error Match
This is the difference in Negative Gain Error between any two channels.

Channel-to-Channel Isolation
Channel-to-Channel Isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 400 kHz sine wave signal to all 15 nonselected input channels and determining how much that signal is attenuated in the selected channel with a 50 kHz signal. The figure is given worse case across all 16 channels for the AD7490.

PSR (Power Supply Rejection)
Variations in power supply will affect the full scale transition, but not the converter's linearity. Power supply rejection is the maximum change in full-scale transition point due to a change in power-supply voltage from the nominal value. (See Typical Performance Characteristics.)

Track/Hold Acquisition Time
The track/hold amplifier returns into track on the 14th SCLK falling edge. Track/hold acquisition time is the minimum time required for the track and hold amplifier to remain in track mode for its output to reach and settle to within ±1 LSB of the applied input signal, given a step change to the input signal.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\ to\ (Noise + Distortion) = (6.02\ N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7490, it is defined as:

$$THD(dB) = 20 \times \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2 fa + fb), (2 fa – fb), (fa + 2 fb) and (fa – 2 fb).

The AD7490 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

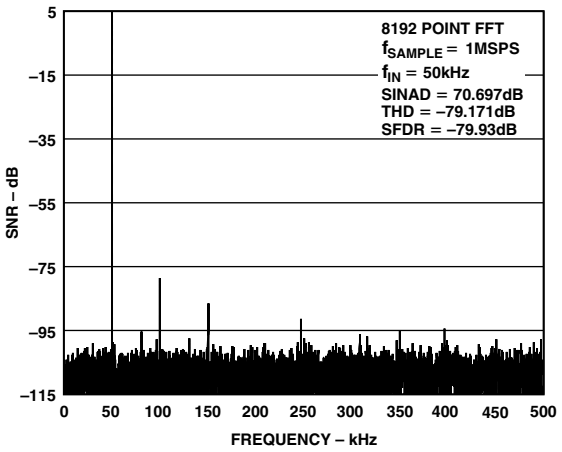
AD7490–Typical Performance Characteristics

TPC 1 shows a typical plot for the AD7490 at 1 MSPS sample rate and 50 kHz input frequency.

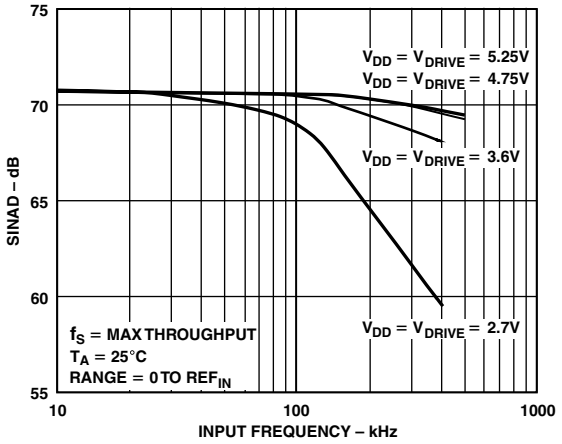
TPC 3 shows the power supply rejection ratio versus supply frequency for the AD7490. The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency f, to the power of a 200 mV p-p sine wave applied to the ADC V_{DD} supply of frequency f_S.

$$PSRR\,(dB) = 10 \times \log\left(\frac{Pf}{Pf_S}\right)$$

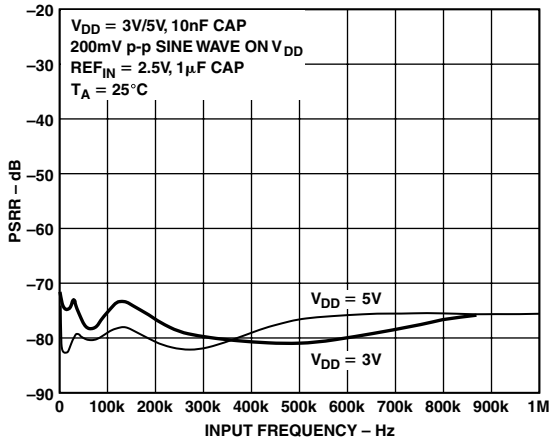
Pf is equal to the power at frequency f in ADC output; Pf_S is equal to power at frequency f_S coupled onto the ADC V_{DD} supply input. Here a 200 mV p-p sine wave is coupled onto the V_{DD} supply. 10 nF decoupling was used on the supply and a 1 µF decoupling cap on the REF_{IN} pin.



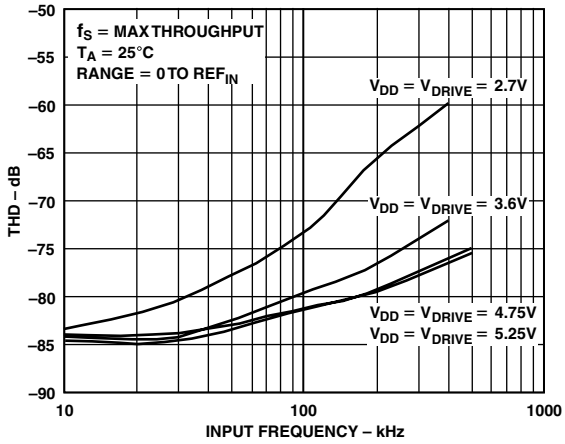
TPC 1. Dynamic Performance at 1 MSPS



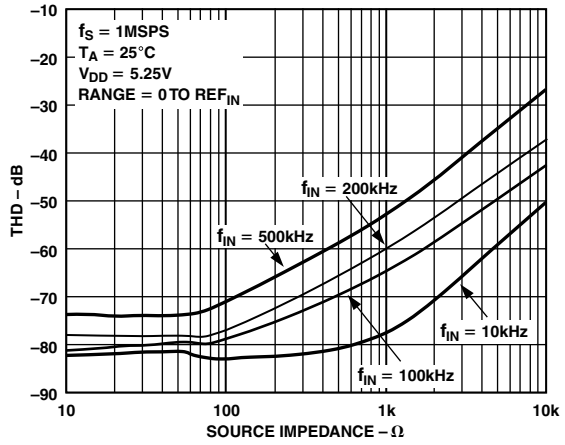
TPC 2. SINAD vs. Analog Input Frequency for Various Supply Voltages at 1 MSPS



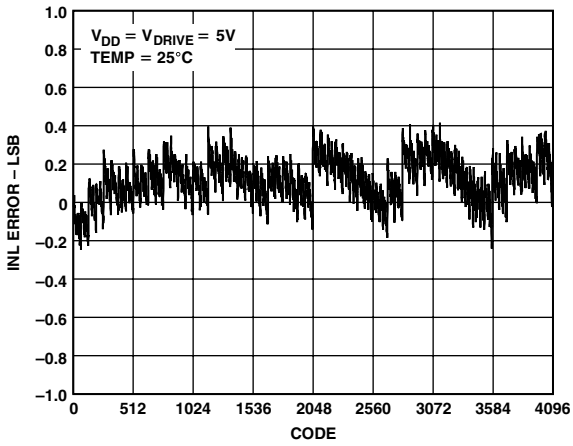
TPC 3. PSRR vs. Supply Ripple Frequency



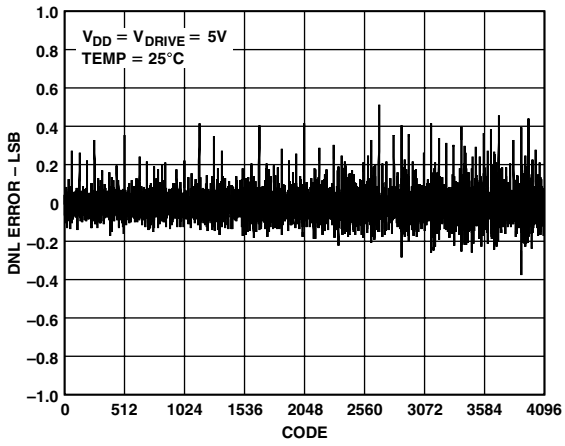
TPC 4. THD vs. Analog Input Frequency for Various Supply Voltages at 1 MSPS



TPC 5. THD vs. Source Impedance for Various Analog Input Frequencies



TPC 6. Typical INL



TPC 7. Typical DNL

CONTROL REGISTER

The Control Register on the AD7490 is a 12-bit, write-only register. Data is loaded from the DIN pin of the AD7490 on the falling edge of SCLK. The data is transferred on the DIN line at the same time as the conversion result is read from the part. The data transferred on the DIN line corresponds to the AD7490 configuration for the next conversion. This requires 16 serial clocks for every data transfer. Only the information provided on the first 12 falling clock edges (after $\overline{CS}$ falling edge) is loaded to the Control Register. MSB denotes the first bit in the data stream. The bit functions are outlined in Table I.

Table I. Control Register Bit Functions

MSB											LSB
WRITE	SEQ	ADD3	ADD2	ADD1	ADD0	PM1	PM0	SHADOW	WEAK/$\overline{TRI}$	RANGE	CODING

Bit	Name	Description
11	WRITE	The value written to this bit of the Control Register determines whether the following 11 bits will be loaded to the control register or not. If this bit is a 1 the following 11 bits will be written to the control register, if it is a 0, the remaining 11 bits are not loaded to the control register and so it remains unchanged.
10	SEQ	The SEQ bit in the control register is used in conjunction with the SHADOW bit to control the use of the sequencer function and access the SHADOW register. (See Table IV.)
9–6	ADD3–ADD0	These four address bits are loaded at the end of the present conversion sequence and select which analog input channel is to be converted on in the next serial transfer or may select the final channel in a consecutive sequence as described in Table IV. The selected input channel is decoded as shown in Table II. The address bits corresponding to the conversion result are also output on DOUT prior to the 12 bits of data, see serial interface section. The next channel to be converted on will be selected by the mux on the 14th SCLK falling edge.
5, 4	PM1, PM0	Power Management Bits. These two bits decode the mode of operation of the AD7490 as shown in Table III.
3	SHADOW	The SHADOW bit in the control register is used in conjunction with the SEQ bit to control the use of the sequencer function and access the SHADOW register. (See Table IV.)
2	WEAK/$\overline{TRI}$	This bit selects the state of the DOUT line at the end of the current serial transfer. If it is set to 1 the DOUT line will be weakly driven to the channel address bit ADD3 of the ensuing conversion. If this bit is set to 0 then DOUT will return to three-state at the end of the serial transfer. See the serial interface section for more details.
1	RANGE	This bit selects the analog input range to be used on the AD7490. If it is set to 0 then the analog input range will extend from 0 V to 2 × REF_{IN}. If it is set to 1 then the analog input range will extend from 0 V to REF_{IN} (for the next conversion). For 0 V to 2 × REF_{IN} V_{DD} = 4.75 V to 5.25 V.
0	CODING	This bit selects the type of output coding the AD7490 will use for the conversion result. If this bit is set to 0, the output coding for the part will be two's complement. If this bit is set to 1, the output coding from the part will be straight binary (for the next conversion).

Table II. Channel Selection

ADD3	ADD2	ADD1	ADD0	Analog Input Channel
0	0	0	0	$V_{IN}0$
0	0	0	1	$V_{IN}1$
0	0	1	0	$V_{IN}2$
0	0	1	1	$V_{IN}3$
0	1	0	0	$V_{IN}4$
0	1	0	1	$V_{IN}5$
0	1	1	0	$V_{IN}6$
0	1	1	1	$V_{IN}7$
1	0	0	0	$V_{IN}8$
1	0	0	1	$V_{IN}9$
1	0	1	0	$V_{IN}10$
1	0	1	1	$V_{IN}11$
1	1	0	0	$V_{IN}12$
1	1	0	1	$V_{IN}13$
1	1	1	0	$V_{IN}14$
1	1	1	1	$V_{IN}15$

Table III. Power Mode Selection

PM1	PM0	Mode
1	1	**Normal Operation** In this mode, the AD7490 remains in full power mode regardless of the status of any of the logic inputs. This mode allows the fastest possible throughput rate from the AD7490.
1	0	**Full Shutdown** In this mode, the AD7490 is in full shut-down mode with all circuitry on the AD7490, powering down. The AD7490 retains the information in the Control Register while in full shutdown. The part remains in full shutdown until these bits are changed in the Control Register.
0	1	**Auto Shutdown** In this mode, the AD7490 automatically enters shutdown mode at the end of each conversion when the control register is updated. Wake-up time from shutdown is 1 μs and the user should ensure that 1 μs have elapsed before attempting to perform a valid conversion on the part in this mode.
0	0	**Auto Standby** In this standby mode, portions of the AD7490 are powered down but the on-chip bias generator remains powered-up. This mode is similar to Auto Shutdown and allows the part to power-up within one dummy cycle, i.e., 1 μs with a 20 MHz SCLK.

For more information, see the Modes of Operation section.

SEQUENCER OPERATION

The configuration of the SEQ and SHADOW bits in the control register allows the user to select a particular mode of operation of the sequencer function. Table IV outlines the four modes of operation of the Sequencer.

Table IV. Sequence Selection

SEQ	SHADOW	Sequence Type
0	0	This configuration means the sequence function is not used. The analog input channel selected for each individual conversion is determined by the contents of the channel address bits ADD0 through ADD3 in each prior write operation. This mode of operation reflects the normal operation of a multichannel ADC, without Sequencer function being used, where each write to the AD7490 selects the next channel for conversion. (See Figure 2.)
0	1	This configuration selects the Shadow Register for programming. After the write to the Control Register, the following write operation will load the contents of the Shadow Register. This will program the sequence of channels to be converted on continuously with each successive valid $\overline{CS}$ falling edge. (See Shadow Register, Table V, and Figure 3.) The channels selected need not be consecutive.
1	0	If the SEQ and SHADOW bits are set in this way then the sequence function will not be interrupted upon completion of the WRITE operation. This allows other bits in the Control Register to be altered while in a sequence without terminating the cycle.
1	1	This configuration is used in conjunction with the channel address bits ADD3 to ADD0 to program continuous conversions on a consecutive sequence of channels from Channel 0 through to a selected final channel as determined by the channel address bits in the Control Register. (See Figure 4.)

SHADOW REGISTER

The Shadow Register on the AD7490 is a 16-bit, write-only register. Data is loaded from the DIN pin of the AD7490 on the falling edge of SCLK. The data is transferred on the DIN line at the same time as a conversion result is read from the part. This requires 16 serial falling edges for the data transfer. The information is clocked into the Shadow Register provided the SEQ and SHADOW bits were set to 0, 1 respectively in the previous write to the Control Register. MSB denotes the first bit in the data stream. Each bit represents an analog input from channel 0 through to channel 15. A sequence of channels may be selected through which the AD7490 will cycle with each consecutive $\overline{CS}$ falling edge after the write to the Shadow Register. To select a sequence of channels, the associated channel bit must be set for each analog input. The AD7490 will continuously cycle through the selected channels in ascending order, beginning with the lowest channel, until a write operation occurs (i.e., the WRITE bit is set to 1) with the SEQ and SHADOW bits configured in any way except 1, 0 (see Table IV). The bit functions are outlined in Table V.

Table V. Shadow Register Bit Functions

MSB															LSB
$V_{IN}0$	$V_{IN}1$	$V_{IN}2$	$V_{IN}3$	$V_{IN}4$	$V_{IN}5$	$V_{IN}6$	$V_{IN}7$	$V_{IN}8$	$V_{IN}9$	$V_{IN}10$	$V_{IN}11$	$V_{IN}12$	$V_{IN}13$	$V_{IN}14$	$V_{IN}15$

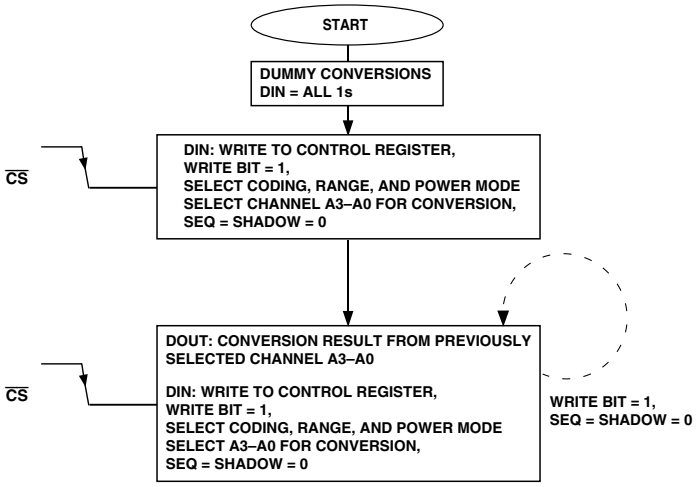


Figure 2. SEQ Bit = 0, SHADOW Bit = 0 Flowchart

Figure 2 reflects the normal operation of a multichannel ADC, where each serial transfer selects the next channel for conversion. In this mode of operation the Sequencer function is not used.

Figure 3 shows how to program the AD7490 to continuously convert on a particular sequence of channels. To exit this mode of operation and revert back to the normal mode of operation of a multichannel ADC (as outlined in Figure 2), ensure the WRITE Bit = 1 and the SEQ = SHADOW = 0 on the next serial transfer.

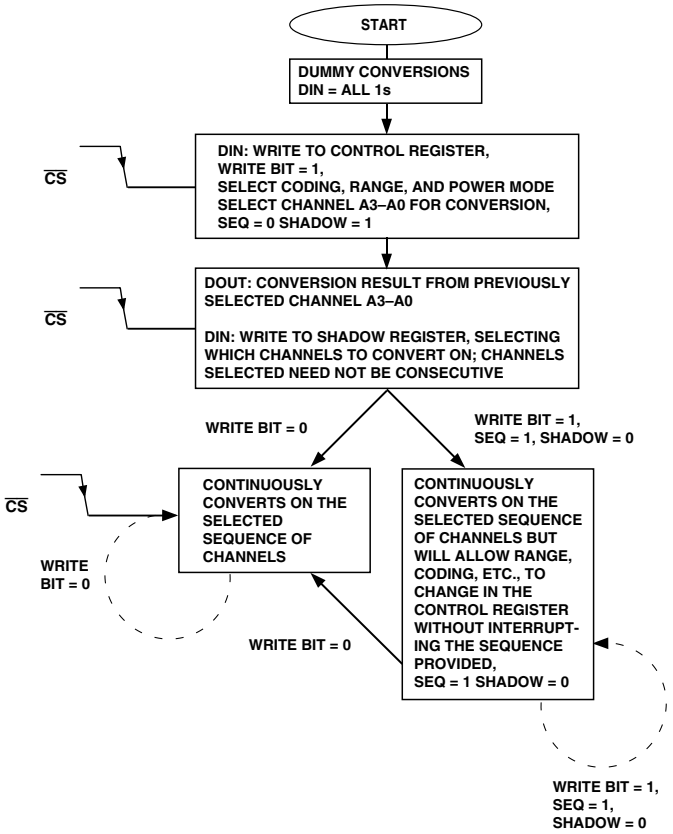


Figure 3. SEQ Bit = 0, SHADOW Bit = 1 Flowchart

Figure 4 shows how a sequence of consecutive channels can be converted on without having to program the shadow register or write to the part on each serial transfer. Again, to exit this mode of operation and revert back to the normal mode of operation of a multi-channel ADC (as outlined in Figure 2), ensure the WRITE Bit = 1 and the SEQ = SHADOW = 0 on the next serial transfer.

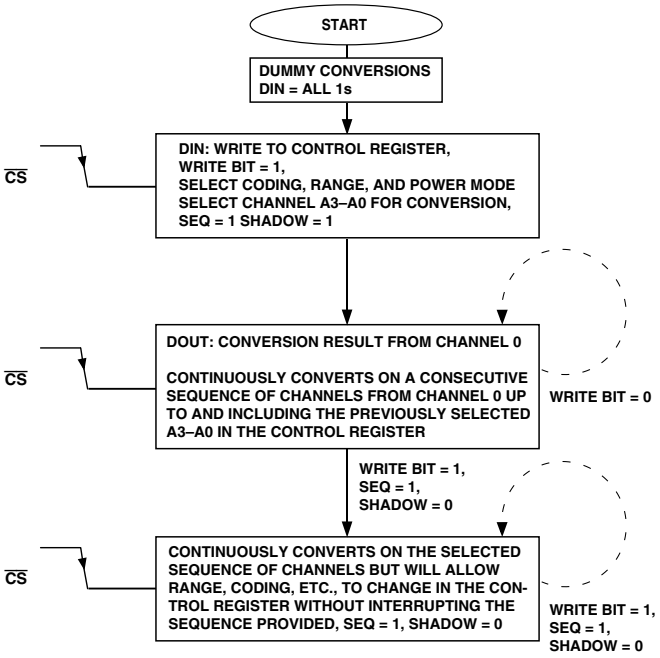


Figure 4. SEQ Bit = 1, SHADOW Bit = 1 Flowchart

CIRCUIT INFORMATION

The AD7490 is a fast, 16-channel, 12-bit, single supply, A/D converter. The parts can be operated from a 2.7 V to 5.25 V supply. When operated from a 5 V supply, the AD7490 is capable of throughput rates of up to 1 MSPS when provided with a 20 MHz clock.

The AD7490 provides the user with an on-chip track/hold, A/D converter, and a serial interface housed in either 28-lead TSSOP or 32-lead LFCSP package. The AD7490 has 16 single-ended input channels with a channel sequencer, allowing the user to select a sequence of channel through which the ADC can cycle with each consecutive $\overline{CS}$ falling edge. The serial clock input accesses data from the part, controls the transfer of data written to the ADC, and provides the clock source for the successive-approximation A/D converter. The analog input range for the AD74790 is 0 to REF_{IN} or 0 to $2 \times REF_{IN}$ depending on the status of bit 1 in the Control register. For the 0 to $2 \times REF_{IN}$ range the part must be operated from a 4.75 V to 5.25 V supply.

The AD7490 provides flexible power management options to allow the user to achieve the best power performance for a given throughput rate. These options are selected by programming the Power Management bits in the Control Register.

CONVERTER OPERATION

The AD7490 is a 12-bit successive approximation analog-to-digital converter based around a capacitive DAC. The AD7490 can convert analog input signals in the range 0 V to $V_{REF\,IN}$ or 0 V to $2 \times V_{REF\,IN}$.

Figures 5 and 6 show simplified schematics of the ADC. The ADC comprises Control Logic, SAR, and a Capacitive DAC, which are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. Figure 5 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on the selected V_{IN} channel.

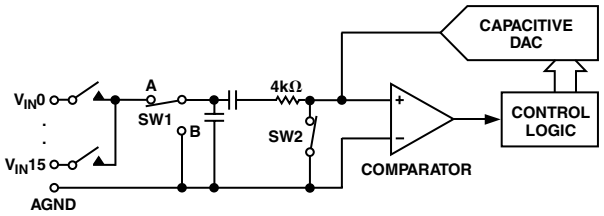


Figure 5. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 6), SW2 will open and SW1 will move to position B causing the comparator to become unbalanced. The Control Logic and the Capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced the conversion is complete. The Control Logic generates the ADC output code. Figure 8 shows the ADC transfer function.

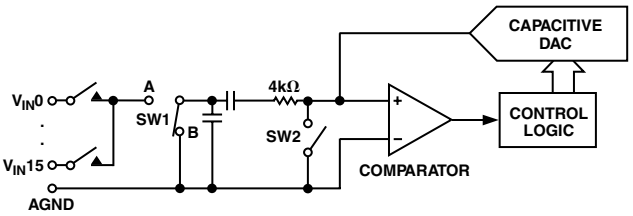


Figure 6. ADC Conversion Phase

Analog Input

Figure 7 shows an equivalent circuit of the analog input structure of the AD7490. The two diodes D1 and D2 provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200 mV. This will cause these diodes to become forward biased and start conducting current into the substrate. 10 mA is the maximum current these diodes can conduct without causing irreversible damage to the part. The capacitor C1 in Figure 7 is typically about 4 pF and can primarily be attributed to pin capacitance. The

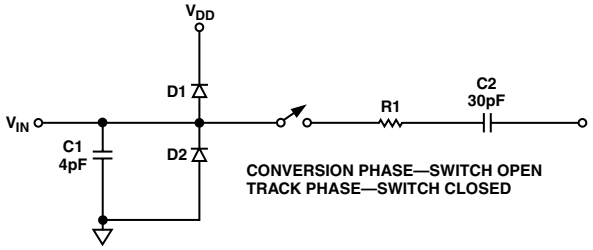


Figure 7. Equivalent Analog Input Circuit

resistor R1 is a lumped component made up of the on resistance of a switch (track and hold switch) and also includes the on resistance of the input multiplexer. The total resistance is typically about 400 Ω. The capacitor C2 is the ADC sampling capacitor and typically has a capacitance of 30 pF. For ac applications, removing high-frequency components from the analog input signal is recommended by use of an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

ADC TRANSFER FUNCTION

The output coding of the AD7490 is either straight binary or two's complement depending on the status of the LSB (RANGE bit) in the Control Register. The designed code transitions occur midway between successive LSB values (i.e., 1 LSB, 2 LSBs, etc.). The LSB size is equal to $REF_{IN}/4096$. The ideal transfer characteristic for the AD7490 when straight binary coding is selected is shown in Figure 8.

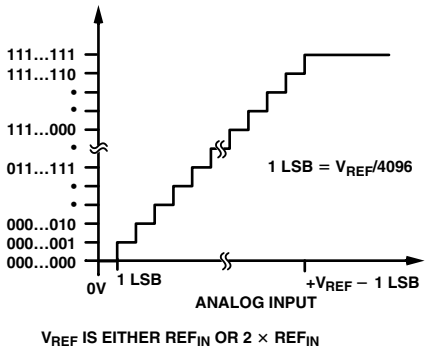


Figure 8. Straight Binary Transfer Characteristic

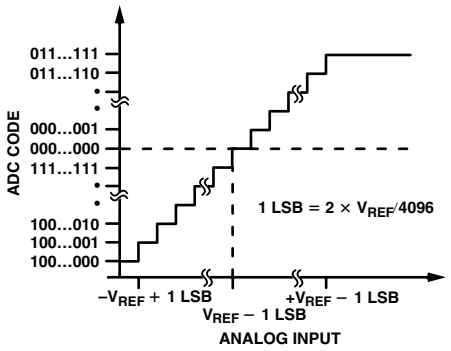


Figure 9. Two's Complement Transfer Characteristic with $REF_{IN} \pm REF_{IN}$ Input Range

Handling Bipolar Input Signals

Figure 10 shows how useful the combination of the 2 × REF_{IN} input range and the two's complement output coding scheme is for handling bipolar input signals. If the bipolar input signal is biased about REF_{IN} and two's complement output coding is selected, then REF_{IN} becomes the zero code point, $-REF_{IN}$ is negative fullscale and $+REF_{IN}$ becomes positive full scale, with a dynamic range of 2 × REF_{IN}.

TYPICAL CONNECTION DIAGRAM

Figure 11 shows a typical connection diagram for the AD7490. In this setup the AGND pin is connected to the analog ground plane of the system. In Figure 11, REF_{IN} is connected to a decoupled 2.5 V supply from a reference source, the AD780, to provide an analog input range of 0 V to 2.5 V (if RANGE bit is 1) or 0 V to 5 V (if RANGE bit is 0). Although the AD7490 is connected to a V_{DD} of 5 V, the serial interface is connected to a 3 V microprocessor. The V_{DRIVE} pin of the AD7490 is connected to the same 3 V supply of the microprocessor to allow a 3 V logic interface (see Digital Inputs section.) The conversion result is output in a 16-bit word. This 16-bit data stream consists of four address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data. For applications where

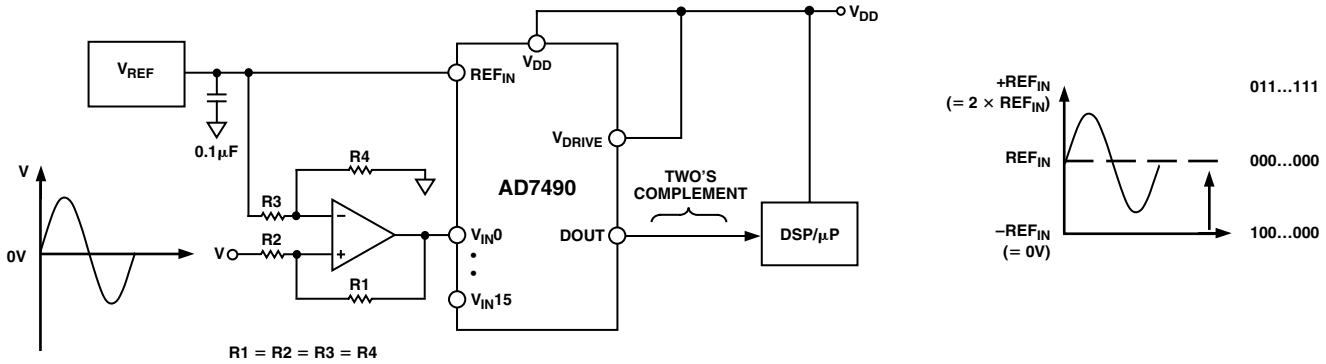


Figure 10. Handling Bipolar Signals

power consumption is of concern, the power-down modes should be used between conversions or bursts of several conversions to improve power performance. (See Modes of Operation section.)

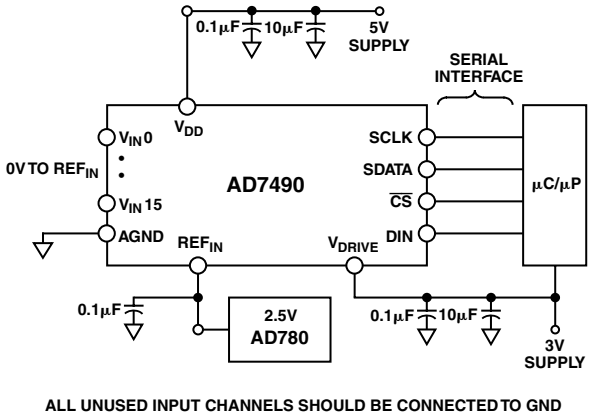


Figure 11. Typical Connection Diagram

Analog Input Section

Any one of 16 analog input channels may be selected for conversion by programming the multiplexer with the address bits ADD3–ADD0 in the control register. The channel configurations are shown in Table II. The AD7490 may also be configured to automatically cycle through a number of channels as selected. The sequencer feature is accessed via the SEQ and SHADOW bits in the control register (see Table IV). The AD7490 can be programmed to continuously convert on a selection of channels in ascending order. The Analog input channels to be converted on are selected through programming the relevant bits in the SHADOW Register (see Table V). The next serial transfer will then act on the sequence programmed by executing a conversion on the lowest channel in the selection.

The next serial transfer will result in a conversion on the next highest channel in the sequence and so on. It is not necessary to write to the control register once a sequencer operation has been initiated. The WRITE bit must be set to zero or the DIN line tied low to ensure the Control Register is not accidently overwritten, or the sequence operation interrupted. If the control register is written to at any time during the sequence then it must be ensured that the SEQ and SHADOW bits are set to 1, 0 to avoid interrupting the automatic conversion sequence. This pattern will continue until such time as the AD7490 is written to and the SEQ and SHADOW bits are configured with any bit combination except 1, 0. On completion of the sequence, the AD7490 sequencer will return to the first selected channel in the shadow register and commence the sequence again if uninterrupted.

Rather than selecting a particular sequence of channels, a number of consecutive channels beginning with channel 0 may also be programmed via the control register alone without needing to write to the SHADOW register. This is possible if the SEQ and SHADOW bits are set to 1, 1. The channels address bits ADD3 through ADD0 will then determine the final channel in the consecutive sequence. The next conversion will be on channel 0, then channel 1 and so on until the channel selected via the address bits ADD3 through ADD0 is reached. The cycle will begin again on the next serial transfer provided the WRITE Bit is set to low or, if high, that the SEQ and SHADOW Bits are set to 1, 0; then the ADC will continue its pre-programmed automatic sequence uninterrupted. Regardless of which channel selection method is used, the 16-bit word output from the AD7490 during each conversion will always contain the channel address that the conversion result corresponds to followed by the 12-bit conversion result (see Serial Interface section).

Digital Inputs

The digital inputs applied to the AD7490 are not limited by the maximum ratings which limit the analog inputs. Instead, the digital inputs applied can go to 7 V and are not restricted by the V_{DD} + 0.3 V limit as on the analog inputs.

Another advantage of SCLK, DIN and $\overline{CS}$ not being restricted by the V_{DD} + 0.3 V limit is the fact that power supply sequencing issues are avoided. If $\overline{CS}$, DIN or SCLK are applied before V_{DD} then there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V was applied prior to V_{DD}.

V_{DRIVE}

The AD7490 also has the V_{DRIVE} feature. V_{DRIVE} controls the voltage at which the serial Interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the AD7490 were operated with a V_{DD} of 5 V, and the V_{DRIVE} pin could be powered from a 3 V supply. The AD7490 has better dynamic performance with a V_{DD} of 5 V while still being able to interface to 3 V processors. Care should be taken to ensure V_{DRIVE} does not exceed V_{DD} by more than 0.3 V. (See Absolute Maximum Ratings section.)

Reference Section

An external reference source should be used to supply the 2.5 V reference to the AD7490. Errors in the reference source will result in gain errors in the AD7490 transfer function and will add the specified full scale errors on the part. A capacitor of at least 0.1 μF should be placed on the REF_{IN} pin. Suitable reference sources for the AD7490 include the AD780, REF193 and the AD1852.

If 2.5 V is applied to the REF_{IN} pin, the analog input range can either be 0 V to 2.5 V or 0 V to 5 V, depending on the RANGE bit in the Control Register.

MODES OF OPERATION

The AD7490 has a number of different Modes of operation. These modes are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements. The mode of operation of the AD7490 is controlled by the power management bits, PM1 and PM0, in the Control Register, as detailed in Table III. When power supplies are first applied to the AD7490, care should be taken to ensure the the part is placed in the required mode of operation (see Powering Up the AD7490 section.)

Normal Mode (PM1 = PM0 = 1)

This mode is intended for the fastest throughput rate performance as the user does not have to worry about any power-up times with the AD7490 remaining fully powered at all time. Figure 12 shows the general diagram of the operation of the AD7490 in this mode.

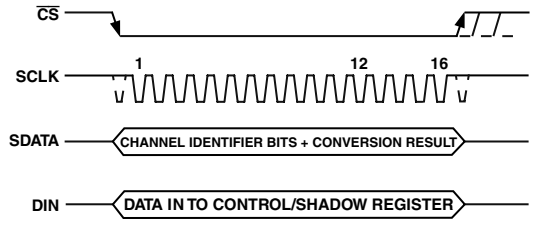


Figure 12. Normal Mode Operation

The conversion is initiated on the falling edge of $\overline{CS}$ and the track and hold will enter hold mode as described in the Serial Interface section. The data presented to the AD7490 on the DIN line during the first twelve clock cycles of the data transfer is loaded to the Control Register (provided WRITE bit is 1). If Data is to be written to the Shadow Register (SEQ = 0, SHADOW =1 on previous write), data presented on the DIN line during the first 16 SCLK cycles is loaded into the Shadow Register. The part will remain fully powered up in Normal Mode at the end of the conversion as long as PM1 and PM0 are set to 1 in the write transfer during that conversion. To ensure continued operation in Normal Mode PM1 and PM0 are both loaded with 1 on every data transfer. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. The track and hold will go back into track on the 14th SCLK falling edge. $\overline{CS}$ may then idle high until the next conversion or may idle low until sometime prior to the next conversion, (effectively idling $\overline{CS}$ low).

Once a data transfer is complete (SDATA has returned to three-state WEAK/$\overline{TRI}$ Bit = 0), another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again.

Full Shutdown (PM1 = 1, PM0 = 0)

In this mode, all internal circuitry on the AD7490 is powered down. The part retains information in the Control Register during full shutdown. The AD7490 remains in full shutdown until the power management bits in the Control Register, PM1 and PM0 are changed.

If a write to the Control Register occurs while the part is in Full Shutdown, with the power management bits changed to PM0 = PM1 = 1, Normal mode, the part will begin to power up on the $\overline{CS}$ rising edge. The track and Hold that was in hold while the part was in Full Shutdown will return to track on the 14th SCLK falling edge.

To ensure that the part is fully powered up, $t_{POWER\ UP}$ (t_{12}), should have elapsed before the next $\overline{CS}$ falling edge. Figure 13 shows the general diagram for this sequence.

Auto Shutdown (PM1 = 0, PM0 = 1)

In this mode, the AD7490 automatically enters shutdown at the end of each conversion when the control register is updated. When the part is in shutdown, the track and hold is in hold mode. Figure 14 shows the general diagram of the operation of the

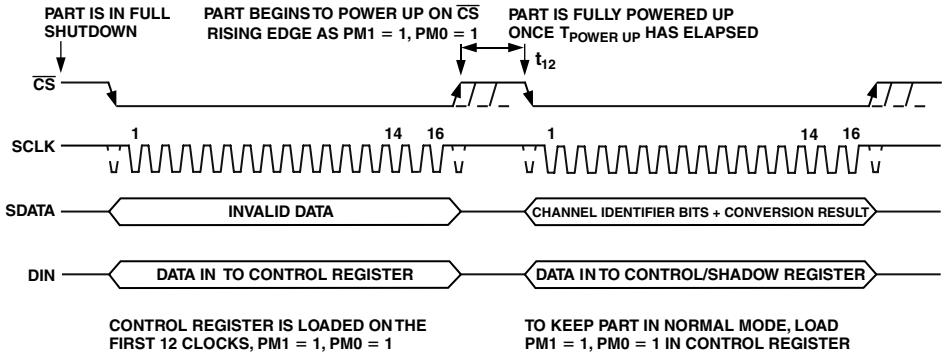


Figure 13. Full Shutdown Mode Operation

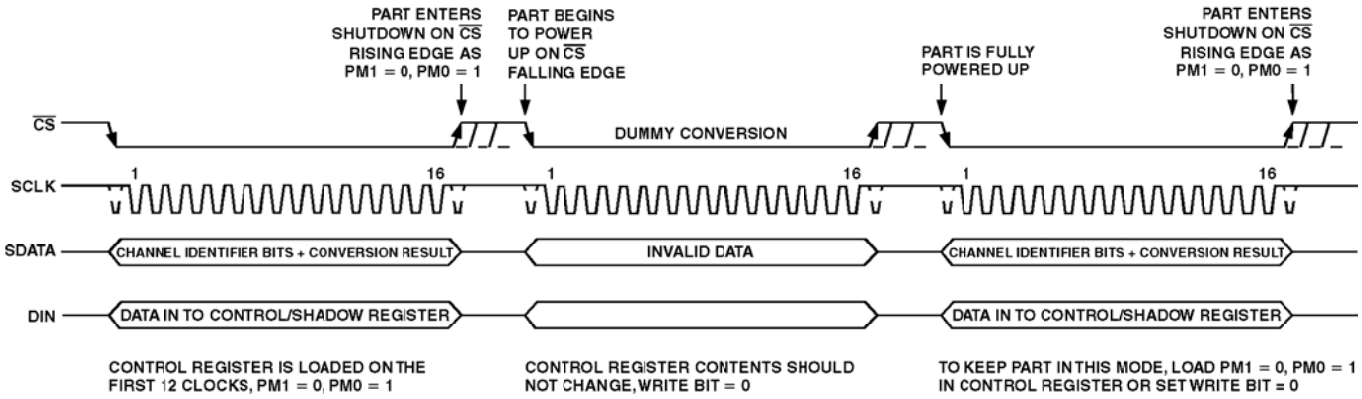


Figure 14. Auto Shutdown Mode Operation

AD7490 in this mode. In shutdown mode all internal circuitry on the AD7490 is powered down. The part retains information in the Control Register during shutdown. The AD7490 remains in shutdown until the next $\overline{CS}$ falling edge it receives. On this $\overline{CS}$ falling edge, the track and hold that was in hold while the part was in shutdown will return to track. Wake-up time from auto shutdown is 1 μs, and the user should ensure that 1 μs has elapsed before attempting a valid conversion. When running the AD7490 with a 20 MHz clock, one dummy cycle of 16 × SCLKs should be sufficient to ensure the part is fully powered up. During this dummy cycle the contents of the Control Register should remain unchanged; therefore the WRITE bit should be 0 on the DIN line. This dummy cycle effectively halves the throughput rate of the part, with every other conversion result being valid. In this mode the power consumption of the part is greatly reduced with the part entering shutdown at the end of each conversion. When the Control Register is programmed to move into auto shutdown it does so at the end of the conversion. The user can move the ADC in and out of the low power state by controlling the $\overline{CS}$ signal.

Auto Standby (PM1 = PM0 = 0)

In this mode, the AD7490 automatically enters standby mode at the end of each conversion when the control register is updated. Figure 15 shows the general diagram of the operation of the AD7490 in this mode. When the part is in standby, portions of the AD7490 are power-down but the on-chip bias generator remains powered up. The part retains information in the Control Register during standby. The AD7490 remains in standby until it receives the next $\overline{CS}$ falling edge. On this $\overline{CS}$ falling edge the track and hold that was in hold while the part was in standby will return to track. Wake-up time from standby is 1 μs, the user should ensure that 1 μs has elapsed before attempting a valid conversion on the part in this mode. When running the AD7490 with a 20 MHz clock one dummy cycle of 16 × SCLKs should be sufficient to ensure the part is fully powered up. During this dummy cycle the contents of the Control Register should remain unchanged, therefore the WRITE bit should be set to 0 on the DIN line. This dummy cycle effectively halves the throughput rate of the part with every other conversion result being valid. In this mode the power consumption of the part is greatly reduced with the part entering standby at the end of each conversion. When the Control Register is programmed to move into Auto Standby it does so at the end of the conversion. The user can move the ADC in and out of the low power state by controlling the $\overline{CS}$ signal.

Powering Up the AD7490

When supplies are first applied to the AD7490, the ADC may power up in any of the operating modes of the part. To ensure the part is placed into the required operating mode the user should perform a dummy cycle operation as outlined in Figure 16.

The three dummy conversion operations outlined in Figure 16 must be performed to place the part into either of the auto modes. The first two conversions of this dummy cycle operation are performed with the DIN line tied HIGH, and for the third conversion of the dummy cycle operation, the user should write the desired control register configuration to the AD7490 in order to place the part into the required Auto Mode. On the third $\overline{CS}$ rising edge after the

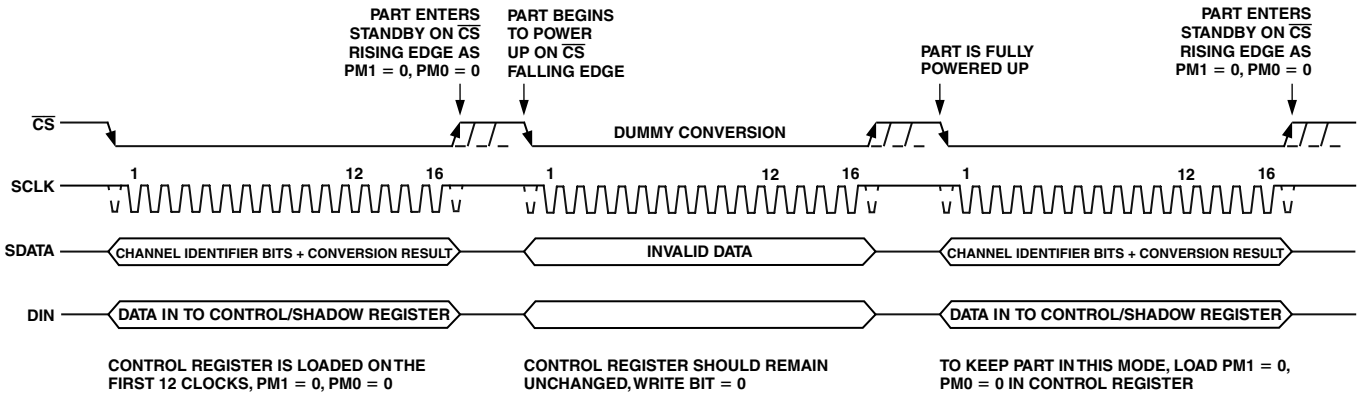


Figure 15. Auto Standby Mode Operation

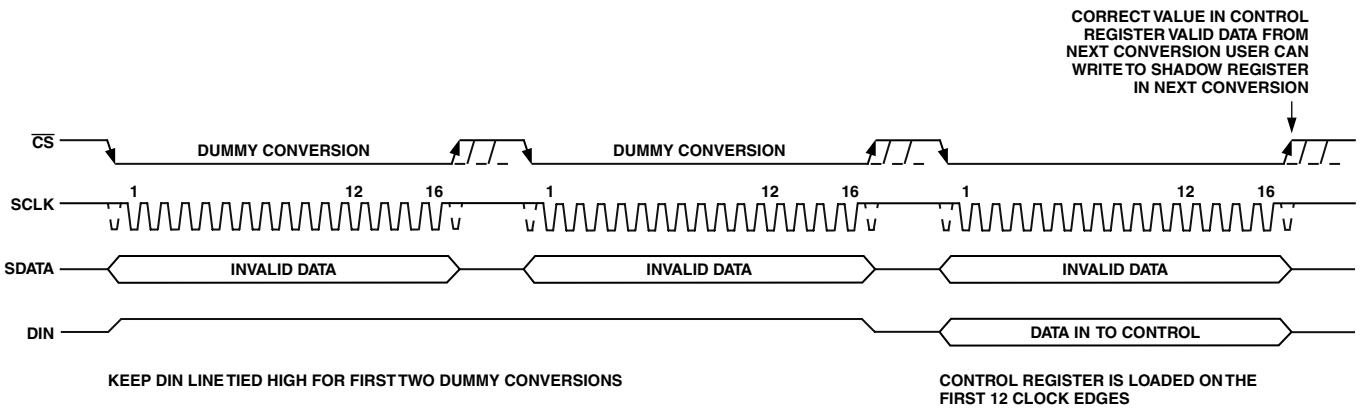


Figure 16. Placing into the Required Operating Mode after Supplies are Applied

supplies are applied, the Control Register will contain the correct information and valid data will result from the next conversion.

Therefore, to ensure the part is placed into the correct operating mode, when supplies are first applied to the AD7490, the user must first issue two serial write operations with the DIN line tied high, and on the third conversion cycle the user can then write to the control register to place to part into any of the operating modes. The user should not write to the Shadow Register until the fourth conversion cycle after the supplies are applied to the ADC, in order to guarantee the Control Register contains the correct data.

If the user wishes to place the part into either Normal Mode or Full Shutdown Mode, the second dummy cycle with DIN tied high can be omitted from the three dummy conversion operation outlined in Figure 16.

SERIAL INTERFACE

Figure 17 shows the detailed timing diagram for serial interfacing to the AD7490. The serial clock provides the conversion clock and also controls the transfer of information to and from the AD7490 during each conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track and hold into hold mode, takes the bus out of three-state and the analog input is sampled at this point. The conversion is also initiated at this point and will require 16 SCLK cycles to complete. The track and hold will go back into track on the 14th SCLK falling edge as shown in Figure 17 at point B, except when the write is to the SHADOW register, in which case the track and hold will not return to track until the rising edge of $\overline{CS}$, i.e., point C in Figure 18. On the 16th SCLK falling edge the DOUT line will go back into three-state (assuming the WEAK/$\overline{TRI}$ Bit is set to 0). Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7490. The 12 bits of data are preceded by the four channel address bits ADD3 to ADD0, identifying which channel the conversion result corresponds to. $\overline{CS}$ going low provides address bit ADD3 to be read in by the microprocessor or DSP. The remaining address bits and data bits are then clocked out by subsequent SCLK falling edges beginning with the second address bit ADD2, thus the first SCLK falling edge on the serial clock has address bit ADD3 provided and also clocks out address bit ADD2. The final bit in the data transfer is valid on the 16th falling edge, having being clocked out on the previous (15th) falling edge.

Writing of information to the Control Register takes place on the first 12 falling edges of SCLK in a data transfer, assuming the MSB, i.e., the WRITE Bit, has been set to 1. If the Control Register is programmed to use the Shadow Register, writing of information to the Shadow Register will take place on all 16 SCLK falling edges in the next serial transfer (see Figure 18). The shadow register will be updated upon the rising edge of $\overline{CS}$ and the track and hold will begin to track the first channel selected in the sequence.

If the WEAK/$\overline{TRI}$ Bit in the Control Register is set to 1, rather than returning to true three-state upon the 16th SCLK falling edge, the DOUT line will instead be pulled weakly to the logic level corresponding to ADD3 of the next serial transfer. This is done to ensure that the MSB of the next serial transfer is setup in time for the first SCLK falling edge after the $\overline{CS}$ falling edge. If the WEAK/$\overline{TRI}$ Bit is set to 0 and the DOUT line has been in true three-state between conversions, then depending on the particular DSP or microcontroller interfacing to the AD7490, address bit ADD3 may not be set up in time for the DSP/micro to clock it in successfully. In this case ADD3 would only be driven from the falling edge of $\overline{CS}$ and must then be clocked in by the DSP on the following falling edge of SCLK. However, if the WEAK/$\overline{TRI}$ Bit had been set to 1, then although DOUT is driven with address bit ADD3 since the last conversion, it is nevertheless so weakly driven

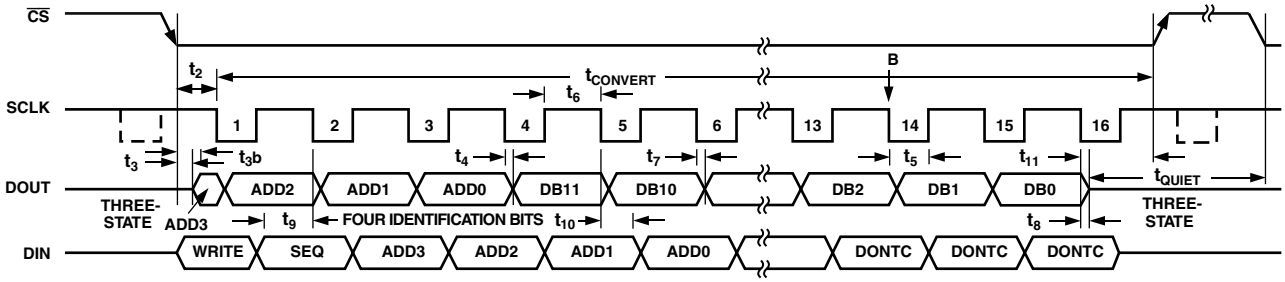


Figure 17. Serial Interface Timing Diagram

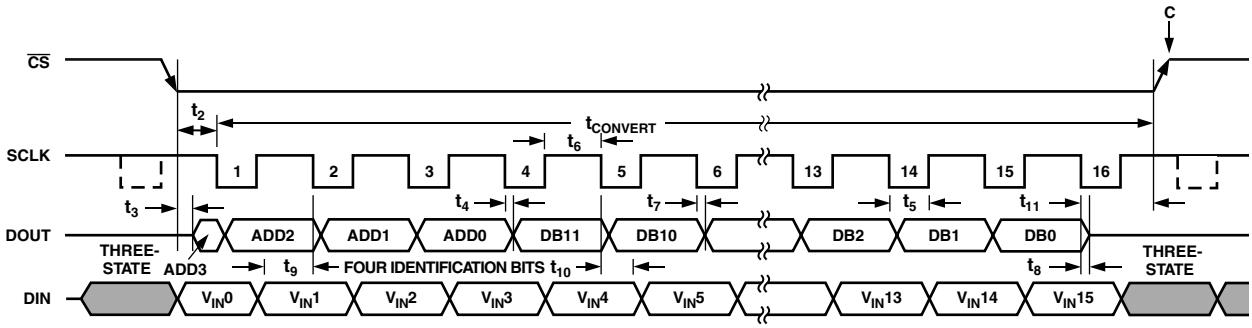


Figure 18. Writing to Shadow Register Timing Diagram

that another device may still take control of the bus. It will not lead to a bus contention and all 16 channels may be identified. However, if this does happen and another device takes control of the bus, it is not guaranteed that DOUT will be fully driven to ADD3 again in time for the read operation when control of the bus is taken back.

This is especially useful if using an automatic sequence mode to identify to which channel each result corresponds. Obviously, if only the first eight channels are in use, then address bit ADD3 does not need to be decoded and whether it is successfully clocked in as a 1 or 0 will not matter as long as it is still counted by the DSP/micro as the MSB of the 16-bit serial transfer.

POWER VERSUS THROUGHPUT RATE

By operating the AD7490 in Auto Shutdown or Auto Standby mode, the average power consumption of the ADC decreases at lower throughput rates. Figure 19 shows how as the throughput rate is reduced, the part remains in its shut-down state longer and the average power consumption over time drops accordingly.

For example if the AD7490 is operated in a continuous sampling mode, with a throughput rate of 100 kSPS and an SCLK of 20 MHz (V_{DD} = 5 V), with PM1 = 0 and PM0 = 1, i.e., the device is in Auto Shutdown mode, then the power consumption is calculated as follows:

The maximum power dissipation during normal operation is 12.5 mW (V_{DD} = 5 V). If the power up time from Auto Shutdown is one dummy cycle, i.e., 1 µs, and the remaining conversion time is another cycle, i.e., 1 µs, then the AD7490 can be said to dissipate 12.5 mW for 2 µs during each conversion cycle. For the remainder of the conversion cycle, 8 µs, the part remains in Shutdown mode. The AD7490 can be said to dissipate 2.5 µW for the remaining 8 µs of the conversion cycle. If the throughput rate is 100 kSPS, the cycle time is 10 µs and the average power dissipated during each cycle is

$$\frac{2}{10} \times 12.5\ mW + \frac{8}{10} \times 2.5\ \mu W = 2.502\ mW$$

When operating the AD7490 in Auto Standby mode, PM1 = PM0 = 0 at 5 V, 100 kSPS, the AD7490 power dissipation is calculated as follows:

The maximum power dissipation is 12.5 mW at 5 V during normal operation. Again the power up time from Auto Standby is one dummy cycle, 1 µs and the remaining conversion time is another dummy cycle, 1 µs. The AD7490 dissipates 12.5 mW for 2 µs during each conversion cycle. For the remainder of the conversion cycle, 8 µs, the part remains in Standby mode, dissipating 460 µW for 8 µs. If the throughput rate is 100 kSPS, the cycle time is 10 µs and the average power dissipated during each conversion cycle is

$$\frac{2}{10} \times 12.5\ mW + \frac{8}{10} \times 460\ \mu W = 2.868\ mW$$

Figure 19 shows the power versus throughput rate when using both the Auto Shutdown mode and Auto Standby mode with 5 V supplies. At the lower throughput rates power consumption for the Auto Shutdown mode is lower than that for the Auto Standby mode, with the AD7490 dissipating less power when in Shutdown compared to Standby. However, as the throughput rate is increased the part spends less time in power-down states, hence difference in power dissipated is negligible between modes. For 3 V supplies the power consumption of the AD7490 decreases, similar power calculations can be done at 3 V.

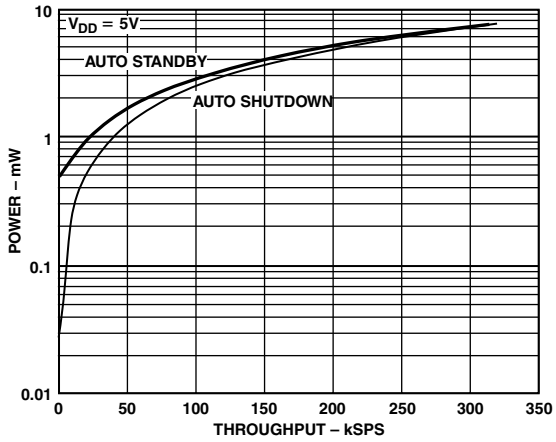


Figure 19. Typical Power vs. Throughput Rate in Auto Shutdown and Auto Standby Mode

MICROPROCESSOR INTERFACING

The serial interface on the AD7490 allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7490 with some of the more common microcontroller and DSP serial interface protocols.

AD7490 to TMS320C541

The serial interface on the TMS320C541 uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7490. The $\overline{CS}$ input allows easy interfacing between the TMS320C541 and the AD7490 without any glue logic required. The serial port of the TMS320C541 is set up to operate in burst mode with internal CLKX0 (TX serial clock on serial port 0) and FSX0 (TX frame sync from serial port 0). The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1, and TXM = 1. The connection diagram is shown in Figure 20. It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the TMS320C541 will provide equidistant sampling. The V_{DRIVE} pin of the AD7490 takes the same supply voltage as that of the TMS320C541. This allows the ADC to operate at a higher voltage than the serial interface, i.e., TMS320C541, if necessary.

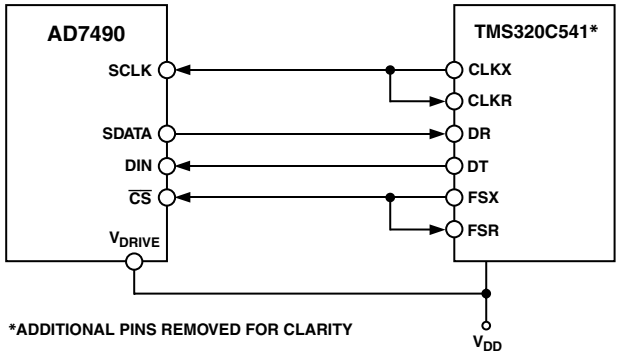


Figure 20. Interfacing to the TMS320C541

AD7490 to ADSP-21xx

The ADSP-21xx family of DSPs are interfaced directly to the AD7490 without any glue logic required. The V_{DRIVE} pin of the AD7490 takes the same supply voltage as that of the ADSP-218x. This allows the ADC to operate at a higher voltage than the serial interface, i.e., ADSP-218x, if necessary.

The SPORT0 control register should be set up as follows:

TFSW =	RFSW = 1, Alternate Framing
INVRFS =	INVTFS = 1, Active Low Frame Signal
DTYPE =	00, Right Justify Data
SLEN =	1111, 16-Bit Data words
ISCLK =	1, Internal Serial Clock
TFSR =	RFSR = 1, Frame every word
IRFS =	0
ITFS =	1

The connection diagram is shown in Figure 21. The ADSP-218x has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in Alternate Framing Mode and the SPORT control register is set up as described. The Frame synchronization signal generated on the TFS is tied to $\overline{CS}$ and as with all signal processing applications equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and under certain conditions, equidistant sampling may not be achieved.

The Timer register etc. are loaded with a value that will provide an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and hence the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given, (i.e., AX0 = TX0), the state of the SCLK is checked. The DSP will wait until the SCLK has gone High, Low and High before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, then the data may be transmitted or it may wait until the next clock edge.

For example, if the ADSP-2189 with a 20 MHz crystal has an overall master clock frequency of 40 MHz, then the master cycle time would be 25 ns. If the SCLKDIV register is loaded with the value 3, a SCLK of 5 MHz is obtained, and eight master clock periods will elapse for every 1 SCLK period. Depending on the throughput rate selected, if the timer registers are loaded with the value 803, 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. This situation will result in non-equidistant sampling as the transmit instruction is occurring on a SCLK edge. If the number of SCLKs between interrupts is a figure of N, then equidistant sampling will be implemented by the DSP.

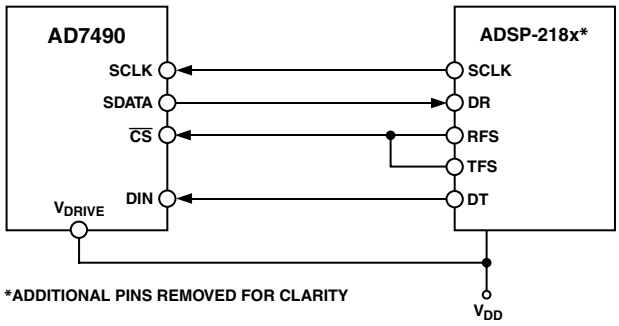


Figure 21. Interfacing to the ADSP-218x

AD7490 to DSP563xx

The connection diagram in Figure 22 shows how the AD7490 can be connected to the ESSI (Synchronous Serial Interface) of the DSP563xx family of DSPs from Motorola. Each ESSI (2 on board) is operated in Synchronous Mode (SYN bit in CRB = 1) with internally generated 1-bit clock period frame sync for both Tx and Rx (bits FSL1 = 0 and FSL0 = 0 in CRB). Normal operation of the ESSI is selected by making MOD = 0 in the CRB. Set the word length to 16 by setting bits WL1 =1 and WL0 = 0 in CRA. The FSP bit in the CRB should be set to 1 so the frame sync is negative. It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the DSP563xx will provide equidistant sampling.

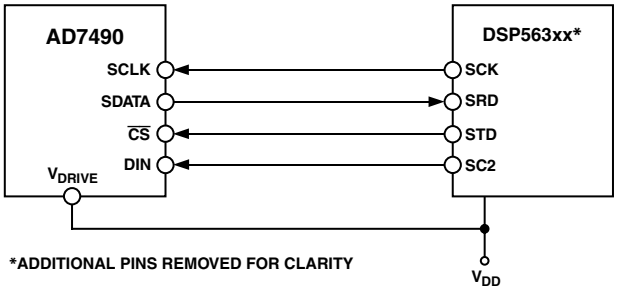


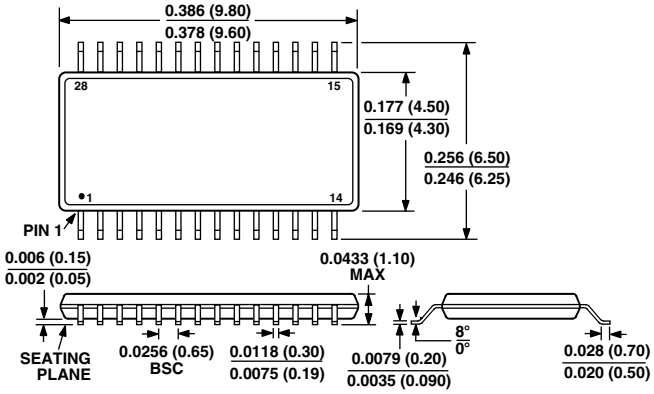
Figure 22. Interfacing to the DSP563xx

In the example shown in Figure 22, the serial clock is taken from the ESSI so the SCK0 pin must be set as an output, SCKD = 1. The V_{DRIVE} pin of the AD7490 takes the same supply voltage as that of the DSP563xx. This allows the ADC to operate at a higher voltage than the serial interface, i.e., DSP563xx, if necessary.

OUTLINE DIMENSIONS

Dimensions shown in inches and millimeters (mm).

28-Lead Thin Shrink Small Outline (TSSOP)
(RU-28)



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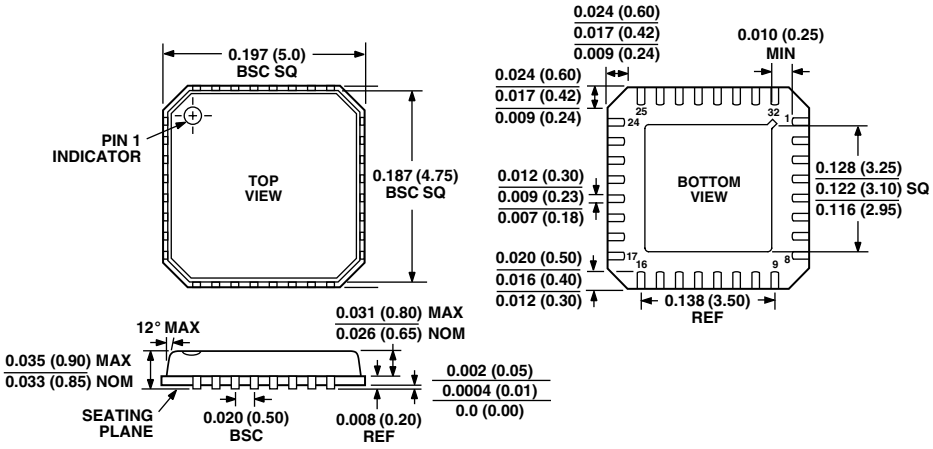
32-Lead LFCSP
(CP-32)



NOTES
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

2. DIMENSIONS MEET JEDEC MO-220-VHHD-2

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