

**CS4952**

## **NTSC/PAL Digital Video Encoder**

The following information is based on the technical datasheet:

CS4952 DS223PP2 OCT '97

Please contact Cirrus Logic : Crystal Semiconductor Products Division for further information.

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PI223PP1 JAN '98



## CS4952 Features

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### *NTSC/PAL Digital Video Encoder*

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#### Features

- Simultaneous composite and S-video output
- Supports RS170A and CCIR601 composite output timing
- Multi-standard support for NTSC-M, PAL (B, D, G, H, I, M, N, Combination N)
- Optional progressive scan @ MPEG2 field rates
- CCIR656 input mode supporting EAV/SAV codes and CCIR601 Master/Slave input modes
- Stable color subcarrier for MPEG2 systems
- NTSC closed caption encoder with interrupt
- Supports Macrovision copy protection in CS4953 version
- Host interface configurable for parallel or I<sup>2</sup>C compatible operation
- General purpose input and output pins
- Individual DAC power-down capability
- On-chip voltage reference generator
- On-chip color bar generator
- +5 volt only, CMOS, low power modes, tri-state DACs

#### Description

The CS4952/3 provides full conversion from YCbCr or YUV digital video formats into NTSC & PAL Composite and Y/C (S-video) analog video. Input formats can be 27 MHz 8-bit YUV, 8-bit YCbCr, or CCIR656 with support for

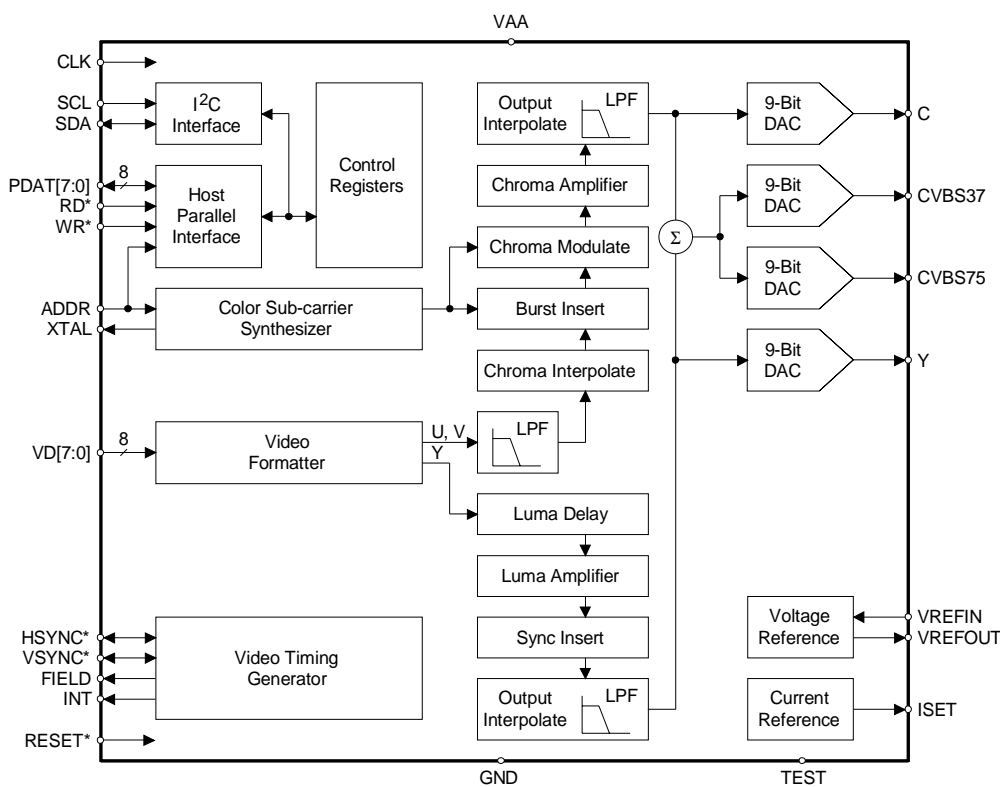


# CS4952 Description

EAV/SAV codes. Output video can be formatted to be compatible with NTSC-M, or PAL B,D,G,H,I,M,N, and Combination N systems. Also supported is NTSC line 21 and line 284 closed captioning encoding.

Four 9-bit DACs provide two channels for an S-Video output port and two composite video outputs. 2x oversampling reduces the output filter requirements and guarantees no DAC related modulation components within the specified bandwidth of any of the supported video standards.

Parallel or high speed I<sup>2</sup>C compatible control interfaces are provided for flexibility in system design. The parallel interface doubles as a general purpose I/O port when the CS4952/3 is in I<sup>2</sup>C mode to help conserve valuable board area.





## CS4952 Overview

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### Overview

The CS4952/3 is a complete multi-standard digital video encoder implemented in current 5-volt only CMOS technology. CCIR601 or CCIR656 compliant digital video input can be converted into NTSC-M, PAL B, PAL D, PAL G, PAL H, PAL I, PAL M, PAL N, or PAL N Argentina-compatible analog video. The CS4952/3 is designed to connect to MPEG1 and MPEG2 digital video decompressors without glue logic.

Two 9-bit DAC outputs provide high quality S-Video analog output while two other 9-bit DACs simultaneously generate composite analog video. The CS4952/3 will accept 8-bit YCbCr or 8-bit YUV input data.

The CS4952/3 is completely configured and controlled via an 8-bit host interface port or an I<sup>2</sup>C compatible serial interface. This host port provides access and control of all CS4952/3 options and features like closed caption insertion, interrupts, etc.

In order to lower the end user set-top overall system costs, the CS4952/3 provides an internal voltage reference which eliminates the requirement for an external discrete 3-pin voltage reference.

### FAQs

- 1) How to bring the CS4952 in standby mode?  
A: In order to bring the part in standby mode, you have to power down all the DACs (through register settings) and then turn off the clock.  
The total current consumption is then 2 mA, which gives a total power consumption of 10 mW.  
The CS4952 retains its previous configuration. It does not need to be reprogrammed.
- 2) What is the difference between powering down DACs and disabling DACs?  
A: When the DACs are disabled, there is no current flow from the output, but there is still a current flow through the DAC. For a low power operation, the DACs can be shut down via the power down registers. In this mode, turn-on through the control register will not be instantaneous.



## CS4952 Ordering Information

- 3) How to get the best performance out of the CS4952?
- A: Three points should be considered to achieve the best performance possible: Layout, clock, ISET.

Proper mixed-signal layout techniques should be used, such as, short supply traces, low ESR decoupling capacities, and split analog and digital power and ground.

Care should be taken to have the best possible 27 MHz clock. It should be free of jitter as much as possible, because color burst accuracy and stability are limited by the 27 MHz clock.

The ISET resistor determines the DAC output current per bit. The selection of that resistor is important to get good DAC performance. It should not vary over temperature and should be precise. Typically a metal film resistor with 1% accuracy should be used.

### Ordering Information

- CS4952/3-CL 44 pin PLCC
- CS4952/3-CQ 44 pin TQFP

For further information on Crystal products, please visit our website "www.crystal.com" or call our literature department (800) 888-5016 ext. 3594 or (512) 912-3594 for data sheets and application notes.

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