CIRRUS LOGIC®

CS5521/22/23/24/28

2-, 4-, or 8-Channel, 16/24-Bit Buffered ΔΣ Multi-Range ADC

The following information is based on the technical data sheet:

CS5521/23 DS317PP2 MAR '99

CS5522/24/28 DS265PP3 MAR '99

Please contact Cirrus Logic for further information.

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PRODUCT INFORMATION

PI317PP3 APR '99

Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at: **www.cirrus.com**

For further information on Cirrus Logic products, please visit our website “www.cirrus.com” or call our literature department (800) 888-5016 ext. 3594 or (512) 912-3594 for data sheets and application notes.

2-, 4-, or 8-Channel, 16/24-Bit ΔΣ Multi-Range ADC

Features

- Delta-Sigma A/D Converter
  - Linearity Error: 0.0007%FS
  - Noise Free Resolution: Up to 18-bits
- Bipolar/Unipolar Input Ranges
  - 25 mV, 55 mV, 100 mV, 1 V, 2.5 V and 5 V
- Chopper Stabilized Instrumentation Amplifier
- On-Chip Charge Pump Drive Circuitry
- Differential Multiplexer
- Conversion Data FIFO
- Programmable/Auto Channel Sequencer
- 2-Bit Output Latch
- Simple three-wire serial interface
  - SPI™ and Microwire™ Compatible
  - Schmitt Trigger on Serial Clock (SCLK)
- Output Settles in One Conversion Cycle
- 50/60 Hz ±3 Hz Simultaneous Rejection
- Buffered V_{REF} with +5 V Input Capability
- System and Self-Calibration with R/W Registers per Channel
- Single +5 V Analog Supply
  +3.0 V or +5 V Digital Supply
- Low Power Mode Consumption: 5.5 mW

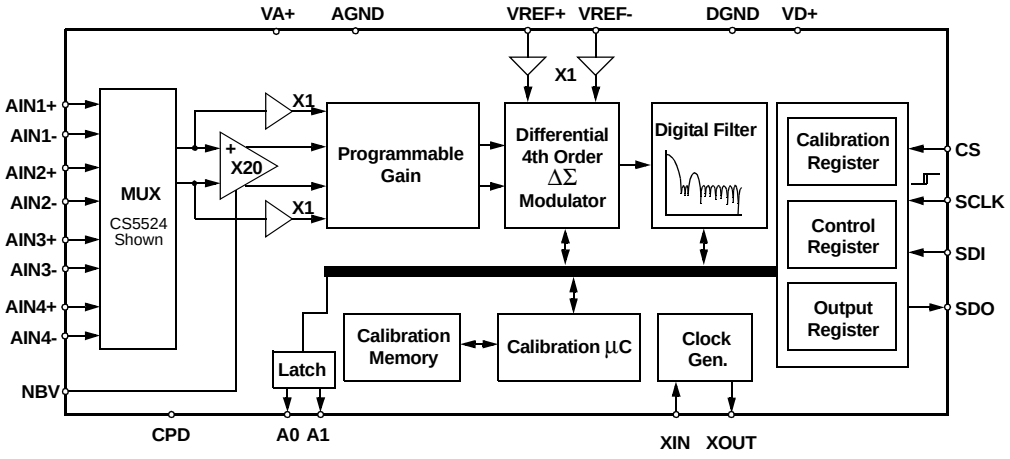
Description

The 16-bit CS5521/23 and the 24-bit CS5522/24/28 are highly integrated ΔΣ A/D converters which include an instrumentation amplifier, a PGA (programmable gain amplifier), a multi-channel multiplexer, digital filters, and self and system calibration circuitry.

The chips are designed to provide their own negative supply which enables their on-chip instrumentation amplifiers to measure bipolar ground-referenced signals ≤±100 mV. By directly supplying NBV with -2.5 V and with VA+ at 5 V, ±2.5 V signals (with respect to ground) can be measured.

The digital filters provide programmable output update rates of 1.88 Hz, 3.76 Hz, 7.51 Hz, 15 Hz, 30 Hz, 61.6 Hz, 84.5 Hz, and 101.1 Hz when operating from a 32-kHz crystal. The CS5521/22/23/24/28 are capable of producing output update rates up to 303 Hz with a 100-kHz clock. The filters are designed to settle to full accuracy for the selected output update rate within one conversion cycle. When operated at word rates of 15 Hz or less, the digital filters reject both 50 and 60 Hz line interference ±3 Hz simultaneously.

Low power, single conversion settling time, programmable output rates, and the ability to handle negative input signals make these single supply products ideal solutions for isolated and non-isolated applications.



Overview

The CS5521/23 and CS5522/24/28 are 16-bit and 24-bit converters which include a chopper-stabilized instrumentation amplifier input, and an on-chip programmable gain amplifier. They are optimized for measuring low-level unipolar or bipolar signals in process control and medical applications.

The CS5521/22/23/24/28 also include a fourth order delta-sigma modulator, a calibration micro-controller, eight digital filters used to select between eight output update rates, a 2-bit analog latch, a multiplexer, and a serial port.

The CS5521/22/23/24/28 include a CPD (Charge Pump Drive) output which provides a negative bias voltage to the on-chip instrumentation amplifier when used with a combination of external diodes and capacitors. This makes the converters ideal for thermocouple temperature measurements because the biasing scheme enables the CS5521/22/23/24/28 to measure negative voltages with respect to ground without the need for a negative supply.

FAQs

1) What determines the input span of the converter?

A: The CS5521/22/23/24/28 provide six default input ranges. With a 2.5V reference the default ranges are 25 mV, 55 mV, 100 mV, 1 V, 2.5 V, and 5 V. The reference voltage can also be used to modify the input range. For example, if the reference voltage is reduced by 50 percent, the default input ranges scale by one half. For example, if VREF = 2.5 V, then Vin = is 0 V to 5 V. If VREF = 1.25 V, then Vin = 0 V to 1.25 V, and if VREF = 5 V, then Vin = 0V to 5 V.

2) Can calibration be used to modify the default input ranges?

A: Yes, calibration can be used to modify the default input ranges. The converters offer system gain calibration which can be used to set the full scale input. With system gain calibration, each range can be exceeded by approximately ±50 percent. Further note the ADCs also offer system offset calibration. System offset calibration is used to set the zero point of the ADC's transfer function. The converter can typically trim ±50 percent of the full scale input span.

3) Is calibration required to use the converter?

A: No, calibration is not required to use the converter. If the signal to be measured is within the ADC's nominally selected input range (25mV, 55mV, 100mV, 1.0V, 2.5V, 5V), the converter can perform conversions without the need for calibrations. Keep in mind that errors in the system remain present when calibration is not performed, however, this may be acceptable if the errors are insignificant to the measurement or if the errors are removed by some other means, such as software. Another side point is that if a factory calibration is performed using system calibration, the contents of the calibration registers can be read by the system's processor and stored in EEPROM. These same calibration coefficients can then be down loaded into the calibrations registers of the ADCs when power is re-applied to the system.

4) How often do I need to recalibrate?

A: A good rule of thumb is to recalibrate the converter (or system) with every ten degrees of ambient temperature change.

5) How does the instrumentation amplifier's chopping frequency affect the converter's input impedance and input current?

A: The CS5521/22/23/24/28 provide extremely low input current and extremely high input impedance. The input impedance of the converter is a dynamic impedance and depends on whether or not the instrumentation amplifier is engaged. For the lower ranges (25 mV, 55 mV, 100 mV), the instrumentation amplifier is engaged. Since the input current in the low ranges at room temperature is around 100pA and the default input range is 100mV, a typical input impedance for the 100 mV range is 1000 MΩ (100mV/100pA). For the higher ranges (1 V, 2.5 V, and 5 V), the instrumentation amplifier is bypassed and coarse/fine charge buffers are activated. The input current to these buffers is tens of nanoamps. For the 2.5 V input range, a typical input impedance is 250 MΩ (2.5 V/10 nA).

6) How many conversion cycles does it take for the converter to settle a full scale step input?

A: The CS5521/22/23/24/25/26/28/29 as well as the CS5504/05/06/07/08/09 family of converters are designed to settle in one conversion cycle. This makes the converters ideally suited for various input level multiplexer applications as the converters can be switched from channel to channel with every conversion while maintaining resolution and accuracy.

7) How does the output word rate affect the ADC's bandwidth?

A: The usable input bandwidth is 1/2 the selected output word rate. For example, with a 15 Hz output word rate selected, the available input signal bandwidth is 7.5 Hz.

8) How does the multiplexer affect the ADC's throughput?

A: The CS5521/22/23/24/28 provide two, four and eight channel input multiplexors. The ADCs' throughputs are divided equally by the number of channels each converter has. For example, lets assume an end user has designed a system that uses a CS5524 in the continuous conversion mode and the user is sequentially stepping through its four channels. With an output word rate of 15 Hz, each channel would yield an effective through put of 15/4, or approximately 3.75 Hz per channel.

9) What is recommended if I need more or less bandwidth than is provided by the on-chip digital filter?

A: The CS5521/22/23/24/28 permit a user to use an external clock between 30 kHz and 100 kHz. By using a lower/higher rate clock, the output word rates as well as the filter corner frequencies scale linearly with the XIN clock rate. For example, by using a 3× clock, the 15 Hz default rate scales to approximately 45 Hz and the input bandwidth increases to approximately 23 Hz.

10) Can the charge pump be used to source current for an external load?

A: Yes, the charge pump can be used to source approximately 450 µA. Applications Note 146 further details systems requiring such current.

11) If the charge pump is engaged, how do I ensure that the converter and its external components are intrinsically safe?

A: Intrinsic safety prohibits the use of electrolytic (or bipolar) capacitors thus limiting the use of certain size capacitors. Although a 10 µF capacitor is recommended for the charge pump, four 0.47 µF ceramic capacitors in parallel can be used.

12) What is the recommended power supply start-up sequence for the ADCs?

A: It is a recommended practice that the analog supply be established before the digital supply. If separate digital and analog supplies are used, it is further recommended that a diode be placed between them (the cathode of the diode should point to the analog supply).

13) What is the recommended software start-up sequence for the ADCs?

A: Assuming a user is using a 32.768kHz crystal for the ADCs and is interfacing them to a micro-controller, the recommended start-up sequence is: 1) put a 500 ms delay in the software code to allow time for the oscillator to start, 2) reset the ADC's serial port with the reset serial port initialization routine (i.e. fifteen 0xFF hexadecimal commands, followed by one 0xFE hexadecimal command), 3) then reset the ADC by setting the RS (Reset System) bit in the configuration register. The user needs to remember to return the RS bit back to zero as the ADC will remain in reset until the bit is cleared.

14) How can I get the best noise performance from the ADCs?

A: The ADC's noise performance is set for a given output word rate and gain range. To minimize the noise's effect on code toggle, use the bipolar mode or increase the reference voltage, as each of these increase the size of an LSB. Also, calibrate the ADCs with the lowest output word rate setting as this minimizes noisy calibrations and use the lowest output word rate as noise performance is best with slower throughputs.

15) What advantages do the channel-sequencer and data conversion FIFO offer?

A: The channel-sequencer permits a user to pre-sequence future conversions. Up to 16 conversion sequences can be programed and converted. Once converted, the data conversion FIFO is used to store the conversions until the are read by a processor at a later time.

16) What benefit does an evaluation board offer?

A: The CDB5521/22/23/24/28 evaluation board saves time and money over prototyping. The preassembled board comes equipped with an 80C51 micro-controller and a 9-pin cable to link the evaluation board to a PC-compatible computer. The evaluation system also includes software which provides easy access to the internal registers of the converter and displays the converter's time domain, frequency domain and noise histogram performance.

Ordering Information

Model Number	Bits	Channels	Linearity Error (Max)	Temperature Range	Package
CS5521-AP	16	2	±0.003%	-40°C to +85°C	20-pin 0.3" Skinny Plastic DIP
CS5521-AS	16	2	±0.003%	-40°C to +85°C	20-pin 0.2" Plastic SSOP
CS5522-AP	24	2	±0.0015%	-40°C to +85°C	20-pin 0.3" Skinny Plastic DIP
CS5522-AS	24	2	±0.0015%	-40°C to +85°C	20-pin 0.2" Plastic SSOP
CS5523-AP	16	4	±0.003%	-40°C to +85°C	24-pin 0.3" Skinny Plastic DIP
CS5523-AS	16	4	±0.003%	-40°C to +85°C	24-pin 0.2" Plastic SSOP
CS5524-AP	24	4	±0.0015%	-40°C to +85°C	24-pin 0.3" Skinny Plastic DIP
CS5524-AS	24	4	±0.0015%	-40°C to +85°C	24-pin 0.2" Plastic SSOP
CS5528-AP	24	8	±0.0015%	-40°C to +85°C	24-pin 0.3" Skinny Plastic DIP
CS5528-AS	24	8	±0.0015%	-40°C to +85°C	24-pin 0.2" Plastic SSOP

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