Application Note

LXT970 TO CS8952 REPLACEMENT GUIDE

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Introduction

This document in conjunction with the CS8952 data sheet will guide the designer in replacing the Level One LXT970 with Cirrus Logic's Crystal LAN CS8952. Since both chips have a standard MII interface, the majority of the work is simply in routing the same signals to the different pin out of the CS8952.

The assumptions used throughout this note are:

1) The CS8952 will be used in full auto negotiation mode, advertising 10/100Mb and Full/Half duplex.
2) A minimum of software configuration is desired.
3) The MAC will use the change of port status interrupt (MDINT on the LXT970, MII_INT on the CS8952) to minimize polling.
4) Phy Address 1.

The following table illustrates the pin to pin mapping and any needed pull up or pull down resistors. Certain configuration pins have no one to one mapping. In this case the pins necessary to match the LXT970 configuration are listed with their needed pull up or pull down resistor value. Power and ground pins are not listed.

The LXT970 specifies 55 ohm series resistors on the MII interface. The CS8952 uses 33 ohm series resistors.

The magnetics requirements for the CS8952 and the LXT970 are the same; a 1:1 turns ratio for both transmit and receive. Changing magnetics should not be necessary. However, the designer should evaluate the magnetics for suitability in their specific design. Please see the CS8952 datasheet for crystal requirements.

LXT970			CS8952		
PIN #	**Name**	**Routing**	**Equiv PIN #**	**Name**	**Routing**
1	CRS	to MAC	49	CRS/Phyaddr[2]	to MAC, 10K pulldown
2	FDS/MDINT	Used as MDINT, connected to Mac, implies bit 17.1 is set	26	MII_IRQ	to MAC, 4.7K pullup
3	TRSTE	to MAC	14	RX_EN	to MAC
4	MF4	MII ADDR[4] low (implies CFG1 Low, FDE don't care)			
5	MF3	MII ADDR[3] low (Scrambler enabled)			

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PIN #	**Name**	**Routing**	**Equiv PIN #**	**Name**	**Routing**
6	MF2	MII ADDR[2]/ low (4B, nibble mode)			
7	MF1	MII ADDR[1] low (DTE mode)			
8	MF0	MII ADDR[0]/ 3.5V (autoneg enabled)			
	Notes for MF pins	MF[4:0] tied to 10/100 autneg, MII address 1, scrambler enabled, DTE mode, full duplex 10/100 advertised, equivalent settings are used for the CS8952 control pins			
10	TEST	Low	24,25	TEST0, TEST1	low
11	XO (crystal out)	N/C	97	XTAL_25O	N/C
12	XI (crystal in)	25/2.5 MHz Clock input	96	XTAL_25I	25 MHz Clock input
13	FDE (full duplex enable)	N/C	57,58	AutoNeg Control	N/C
14	CFG0 (Configuration pin 0)	low	NONE		
15	MDDIS (MDIO DISABLE)	high (all presets permanent)	NONE		
16	RESET	to MAC	15	RESET	to MAC
17	FIBOP (fiber out positive)	N/C	5	TX_NRZ+	N/C
18	FIBON (fiber out negative)	N/C	6	TX_NRZ-	N/C
20	TREF	tied to center tap of output transformer	NONE		
21	TPOP	transformer	80	TX+	transformer
23	TPON	transformer	81	TX-	transformer
25	RBIAS	22K 1% to ground	86	RES	4.99K 1% to ground
27	FIBIP	N/C	7	RX_NRZ+	N/C
28	FIBIN	N/C	6	RX_NRZ-	N/C
29	TPIP	transformer	91	RX+	transformer
30	TPIN	transformer	92	RX-	transformer
33	CFG1 (configuration pin 1)	low	NONE		
34	PWRDN	to MAC	64	PWRDN	to MAC
38	LEDS	LED	67	SPEED_100	LED (high efficiency)
39	LEDC	LED	73	LED5 (collision)	LED
40	LEDL	LED	71	LED3 (link OK)	LED
41	LEDT	LED	69	LED1 (tx active)	LED
42	LEDR	LED	70	LED2 (rx active)	LED
44	MDIO	to MAC	27	MDIO	to MAC
45	MDC	2.5MHz Clock	28	MDC	2.5MHz Clock
46	RXD4	to MAC	37	RX_ERR/RXD[4]/ PHY_ADDR[4]	to MAC, 10K pulldown
47	RXD3	to MAC	29	RXD[3]PHY_ADDR[3]/ PHY_ADDR[3]	to MAC, 10K pulldown
48	RXD2	to MAC	30	RXD[2]	to MAC
49	RXD1	to MAC	31	RXD[1]/ PHY_ADDR[1]	to MAC, 10K pulldown
50	RXD0	to MAC	32	RXD[0]	to MAC

LXT970			CS8952		
PIN #	**Name**	**Routing**	**Equiv PIN #**	**Name**	**Routing**
51	RX_DV	to MAC	33	RXDV/MII_DRV	to MAC
54	RX_CLK	to MAC	36	RX_CLK	to MAC
55	RX_ERR	to MAC	37	RX_ERR/RXD[4]/ PHY_ADDR[4]	to MAC, 10K pulldown
56	TX_ERR	to MAC	38	TX_ERR/TXD[4]	to MAC
57	TX_CLK	to MAC	42	TX_CLK	to MAC
58	TX_EN	to MAC	43	TX_EN	to MAC
59	TXD0	to MAC	44	TXD[0]	to MAC
60	TXD1	to MAC	45	TXD[1]	to MAC
61	TXD2	to MAC	46	TXD[2]	to MAC
62	TXD3	to MAC	47	TXD[3]	to MAC
63	TXD4	to MAC	38	TX_ERR/TXD[4]	to MAC
64	COL	to MAC	48	COL/PHYADD[0]	to MAC, 10K pullup