Application Note

USING THE CS7620/22 WITH CCDs

INTRODUCTION

This application gives an overview of how to use the CS7620/22 with different CCDs. Each short example explains the different modes and signals involved.

Example #1 : CS7620 in Master Mode:

To select this mode, the user must set the BYPASS_PLL pin LOW and select the proper internal timing mode in the timing mode register (See CS7620 Register Configuration). The CS7620 will provide vertical and horizontal outputs to the vertical driver/CCD. It only requires external clock, EXPOSE and POWER DOWN signals. When PWR_DN is high, all of the CS7620 powers down except for the DAC outputs (which may be powered down through register controls). The EXPOSE signal should go high at the beginning of exposure and low at the beginning of read out. The LINE_ENA and CLAMP are not used in Master Mode and should be tied low. The use of two vertical drivers is suggested in the Sony ICX205AK datasheet. Note that the two internal DACs can be used for any bias used for the CCD.

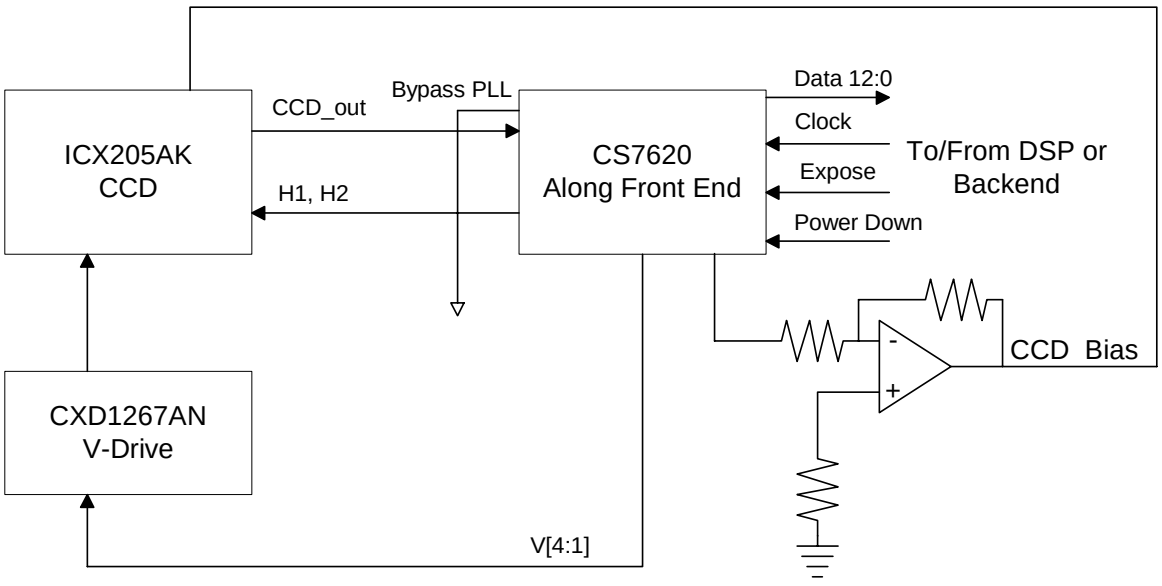

Figure 1. Master Mode

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Example #2 : CS7620 in Slave Mode:

In this example, the Sony Timing Generator/Vertical Driver is used to generate all the timing information. In this configuration, the CS7620 is in Slave Mode, therefore it requires all the timing information from an external source. The user must set the BYPASS_PLL pin HIGH and provide the following signals: EXPOSE, POWER DOWN, CLAMP, CLK_FT and CLK_DT. The EXPOSE signal is redefined as a non-readout signal. This is used so that the back end processor can account for the chip latency. The POWER DOWN pin may be use to save power. CLAMP should be high when over the DARK reference pixels. CLK_FT and CLK_DT are respectively used to sample the Feedthrough level and the pixel (data) level (See Figure 2).

CK_FT and CK_DT:

The XTAL_IN and LINE_ENA pins are redefined as the CK_FT and CK_DT signals, which sample the feedthrough and data levels, respectively. The timing for CK_FT and CK_DT is shown in Figure 3. Note that these clocks are non-overlapping.

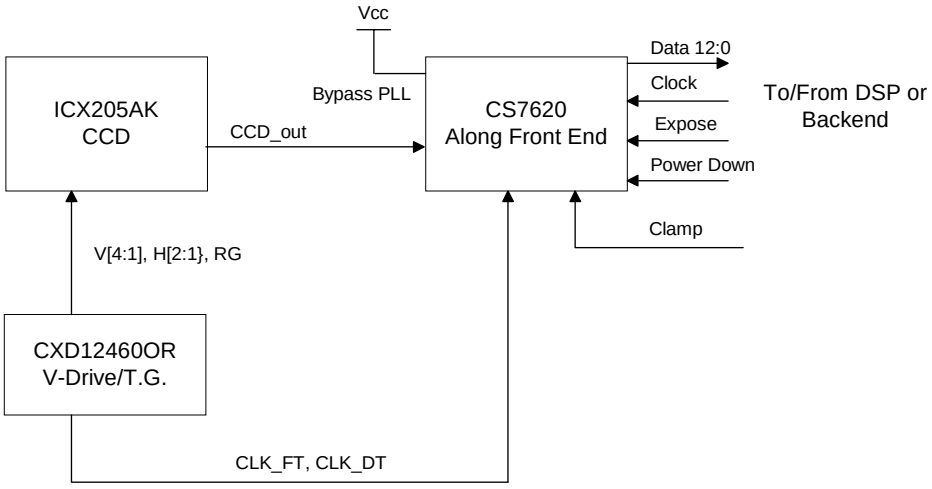


Figure 2. Slave Mode

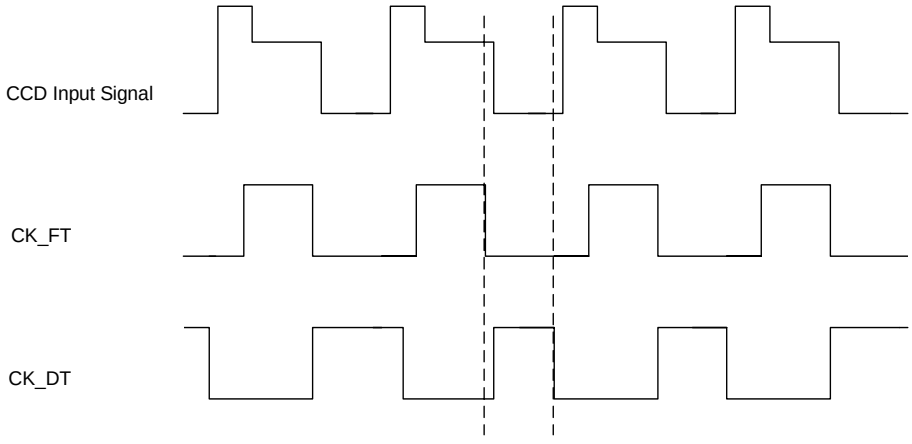


Figure 3. Clock Timing

Example #3 : CS7620 in Partial Master Mode:

To select this mode, the user must set the BYPASS_PLL pin LOW and the select external timing mode in the timing mode register. The CS7620 is the master of the pixel rate timing, but the line and frame timing is controlled elsewhere. In this mode, the user must control four signals: PWR_DN, EXPOSE, LINE_ENA, and CLAMP. The master PWR_DN signal may be used to conserve power during non-readout time. The EXPOSE pin is redefined as a non-readout time signal. This is used so that the back end processor can account for the chip latency (See Figure 4).

The LINE_ENA signal should be high during the vertical shift and load times, and CLAMP should be high when over the dark reference pixels. The suggested timing for these signals is shown in Figure 5. Note that the chip should be powered up at least 500 us before the beginning of readout. The CLAMP signal may also be high during the dark pixel lines at the beginning of the frame.

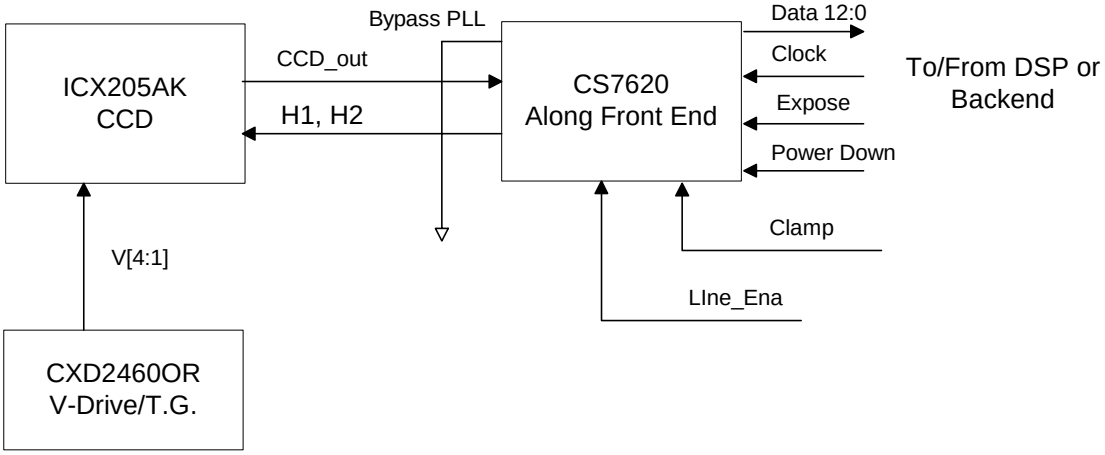


Figure 4. Partial Master Mode

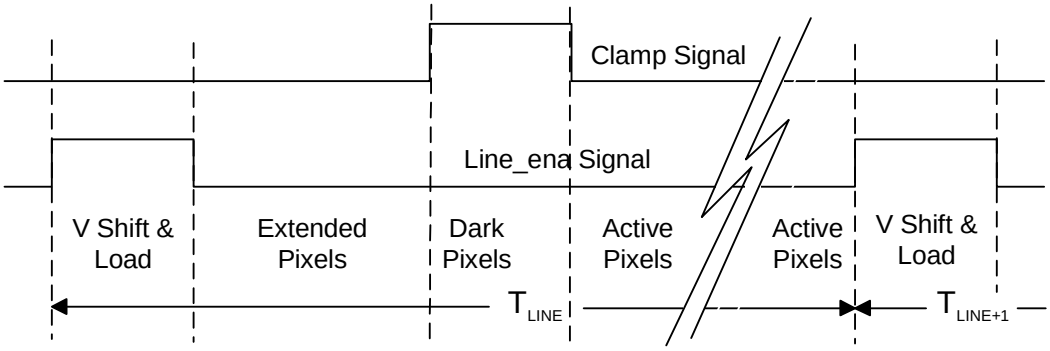


Figure 5. Clamp and Line Enable

NOTE: In partial master mode, we have full programmability over the four horizontal signals (H1-H4) and the RG signal. This means that the rise and fall time of each signal can be individually programmed. Each adjustment made on the rise and fall time has a step of one-eighth of the pixel clock. Through reg. 2C, H1-H4 and RG delay can be fine tuned to ensure optimum sampling time with a resolution of 1.5 ns.

CS7620 Register Configuration:

To use the CS7620 with the Sony imager a handful of registers need to be modified.

Set tim_modes in Operation Control 1 register (address 06h) for Sony imager:

Master Mode

tim_modes [2:0] set to 011 for low resolution timing
tim_modes [2:0] set to 100 for high resolution timing
H clocks programmed through reg. 29h-2Ch

Slave Mode

tim_modes [2:0] set to 111 - bypass pll high

Partial Slave Mode

tim_modes [2:0] set to 111 - bypass pll low, H clocks programmed through reg. 29h-2Ch.

The amount of exposure measured in line lengths can be controlled through reg. 23h-24h. The n_extra[10:0] allows for increased exposure time while in low resolution mode. The H clocks must also be programmed for the sony CCD (Reg. 29h-2Ch).

Example #4 : CS7622:

In this example, the Sony Timing Generator/Vertical Driver is used to generate all the timing information. The CS7622 is ALWAYS Slave to the timing generator, therefore it requires all the timing information from an external source (See Figure 6).

The presence of black pixels in the CCD output is indicated by the CLAMP pulse, which must be fed to the CS7622. The input clocks CLK_FT and CLK_DT are used to set up the sampling times and also to generate the digital clock. These clocks need to be running when processing pixels from the CCD, accessing the registers or performing calibration. The timing of these clocks is important to ensure optimum settling times and sampling the correct value. CLK_FT and CLK_DT need to be non-overlapping pulses made as wide as possible to give long settling times. The falling edge of CK_FT should be close to the end of feedthrough while the falling edge of CK_DT should be close to the end of the data section of the CCD signal. See figure 7, connection diagram, for more details on how to interface the CS7622.

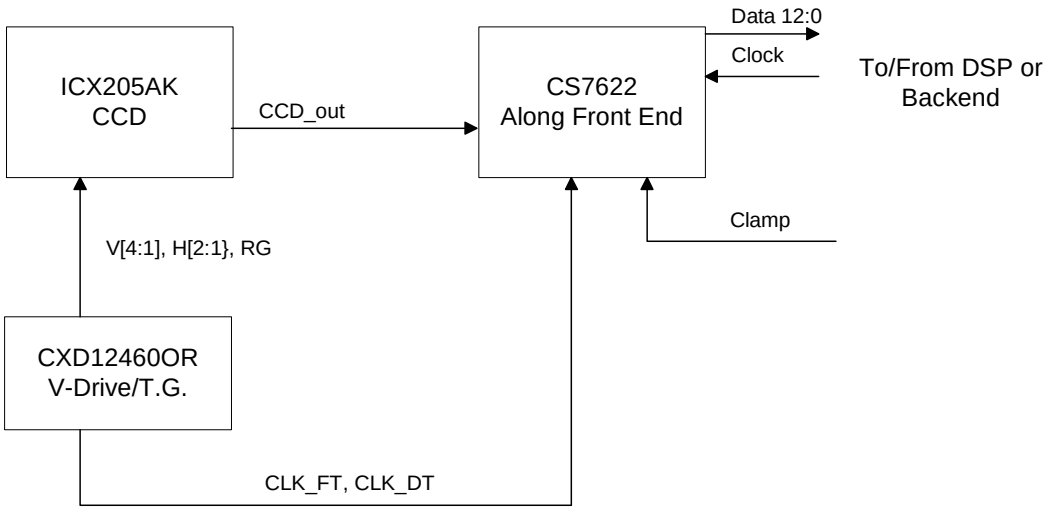


Figure 6. CS7622 (Always Slave)

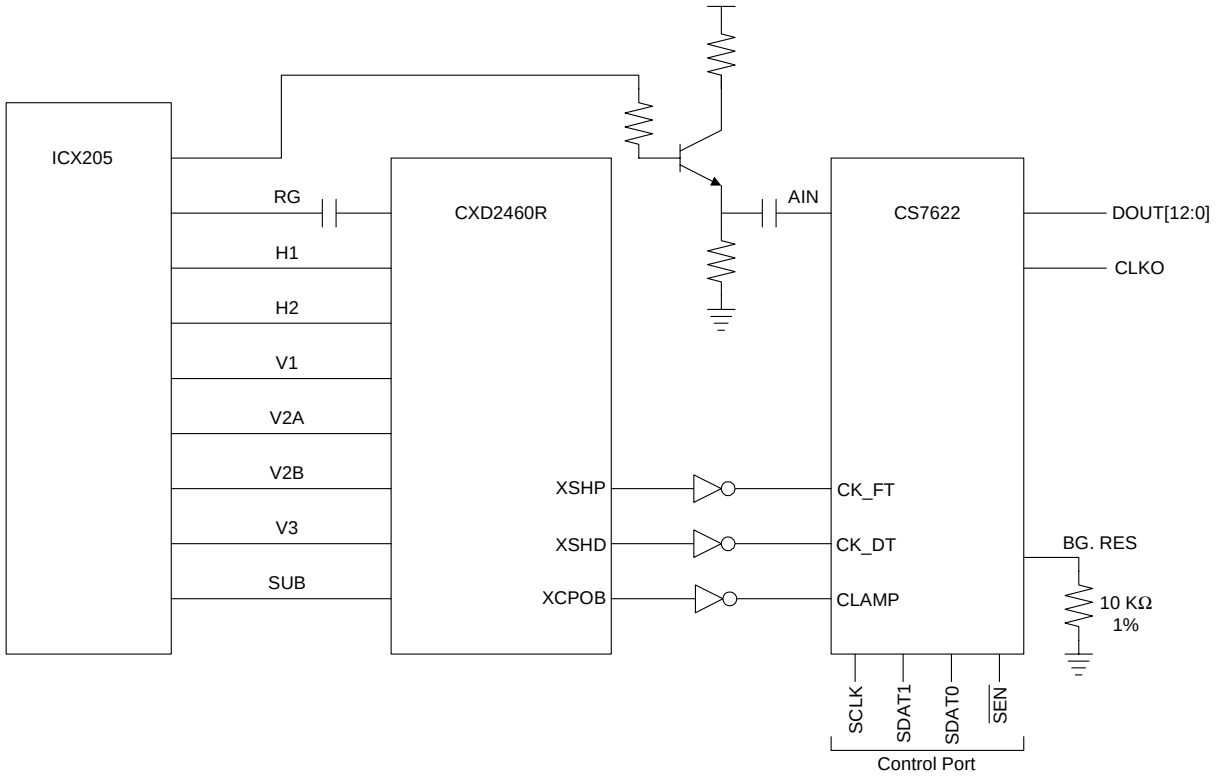


Figure 7. Connection Diagram

Non-Overlap clock generator circuit:

This circuit will allow you to generate a non-overlap clock.

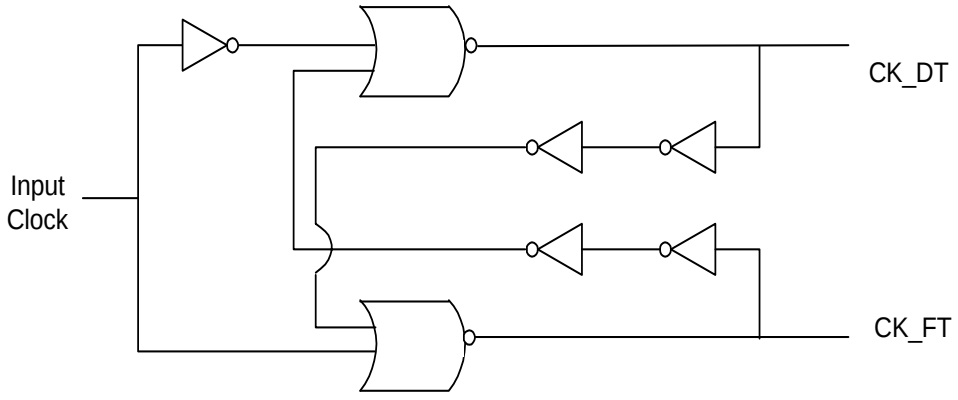
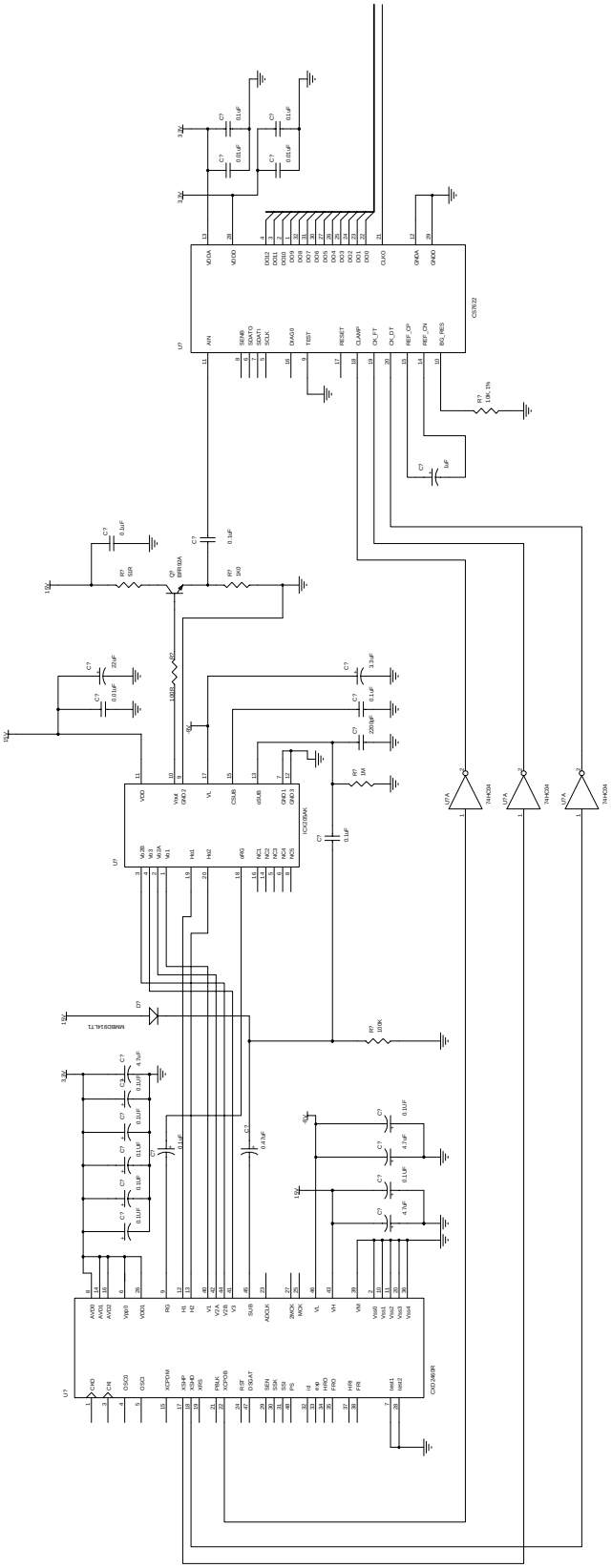


Figure 8. Non-Overlap Clock Generator

* Refer to CS7622 Datasheet for timing information.



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